Fail-Safe IC with High-Side Driver and Relay Driver

Description

The function of microcontrollers in safety critical applications (e.g. anti-lock systems) needs to be monitored permanently. Usually this task is accomplished by an independent watchdog timer. The monolithic IC U6813B – designed in bipolar technology and qualified according to the needs of the automotive industry – includes such a watchdog timer and provides additional features for added value. With the help of integrated driver stages it is easy to control safety related functions of a relay and of an N-channel power MOSFET in high side applications. In the case of a microcontroller malfunction or supply voltage anomalies the U6813B provides positive and negative reset and enable output signals. This flexibility guarantees a broad range of applications. The U6813B is based on the experience of the Atmel Wireless & Microcontrollers Failsafe ICs U6808B and U6809B.

Features

- Digital self-supervising watchdog with hysteresis
- One 150-mA output driver for relay
- One high-side driver for n-channel power FET
- Positive and negative enable output
- Positive and negative reset output
- Over-/ under-voltage detection
- Relay and power-FET outputs protected against standard transients and 55-V load dump

Block Diagram

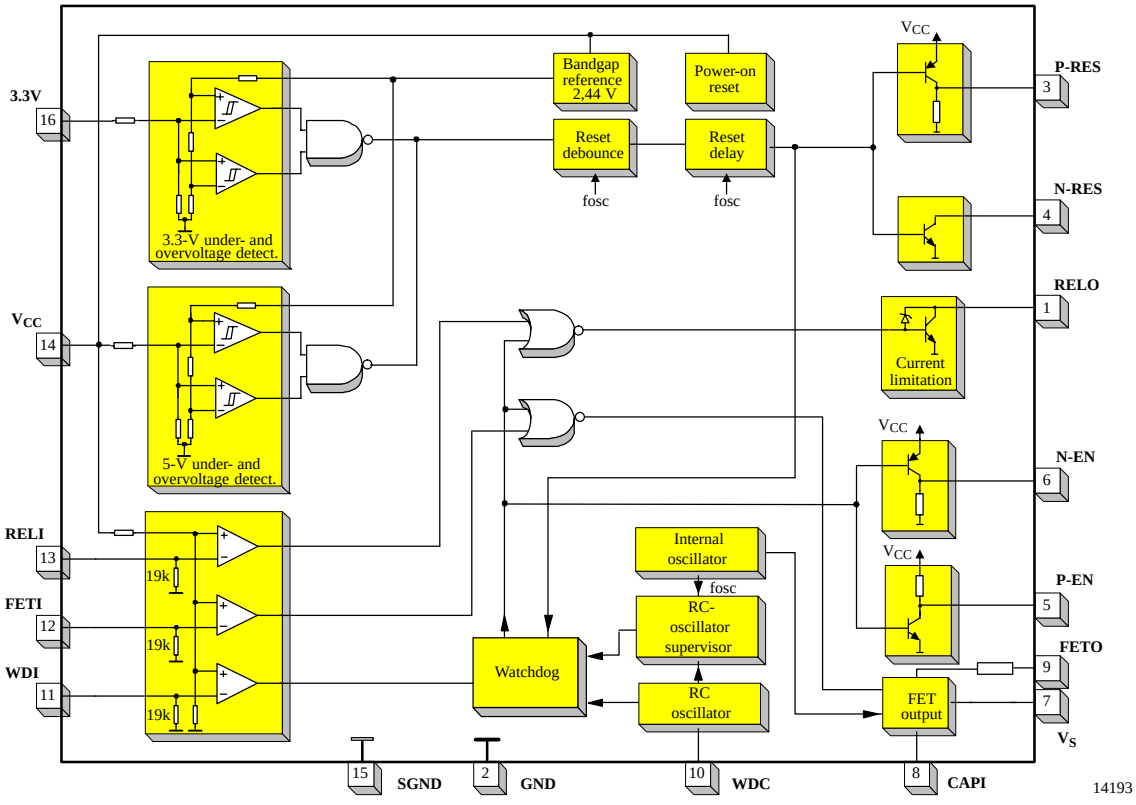


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U6813B	SO16	

Pin Description

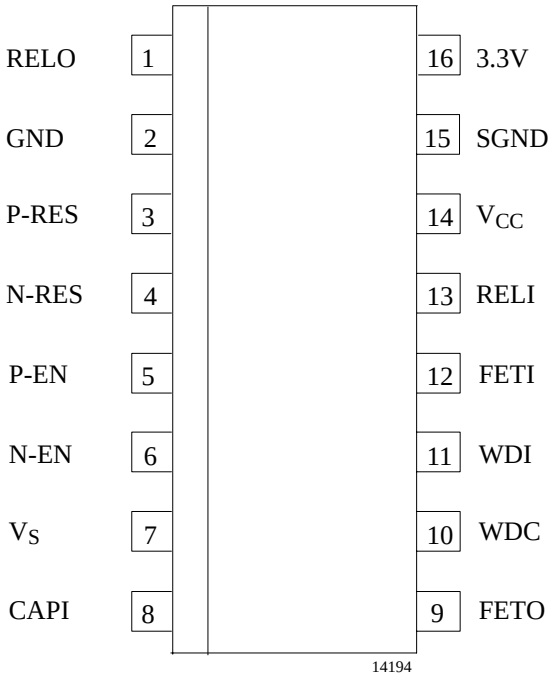


Figure 2. Pinning

Table 1 Pin types and functions

Pin	Name	Type	Function	Logic
1	RELO	Open-collector output driver	Failsafe relay driver	Driver on: L
2	GND	Supply	General ground	
3	P-RES	Digital output	Positive reset signal	Reset: H
4	N-RES	Digital output	Negative reset signal	Reset: L
5	P-EN	Digital output	Positive enable signal	Enable: H
6	N-EN	Digital output	Negative enable signal	Enable: L
7	V_S	Battery supply	Voltage for charge pump	
8	CAPI	Analog input	Input bootstrap capacitor	
9	FETO	Power FET output	High voltage for n-channel FET	
10	WDC	Analog input	Ext. RC for watchdog timer	
11	WDI	Digital input	Watchdog trigger signal	Pulse sequence
12	FETI	Digital input	Activation of power FET	FET on: H
13	RELI	Digital input	Activation of relay driver	Driver on: H
14	V_{CC}	Supply	5-V supply	
15	SGND	Supply	Sense ground, reference for V_{CC} and 3.3V	
16	3.3V	Analog input	3.3-V supply	

Fail-Safe Functions

A good fail-safe IC has to maintain its monitoring function even if there is a fault condition at one of the pins (e.g. short circuit) ensuring that a microcontroller system would not go into a ”critical status”. A system would get into critical status for example if it would not be able to switch off the relay or disable the power MOSFET or could not to give a signal to the mC via ENABLE- and RESET- outputs in the case of a fault condition. The U6813B is designed to handle those fault conditions according to the following table for a maximum of system safety.

Table 2 Truth table

VCC	3.3V	WDI	RELI	FETI	RELO	FETO	N–RES	P–RES	P–EN	N–EN
ok	ok	ok	H	x	on	x	H	L	H	L
ok	ok	ok	L (d)	x	off	x	H	L	H	L
ok	ok	ok	x	H	x	on	H	L	H	L
ok	ok	ok	x	L (d)	x	off	H	L	H	L
ok	ok	wrong	x	x	off	off	H	L	L	H
x	wrong	x	x	x	off	off	L	H	L	H
wrong	x	x	x	x	off	off	L	H	L	H

d = default state at open input
N–EN disable: high
P–EN disable: low

Application Circuit

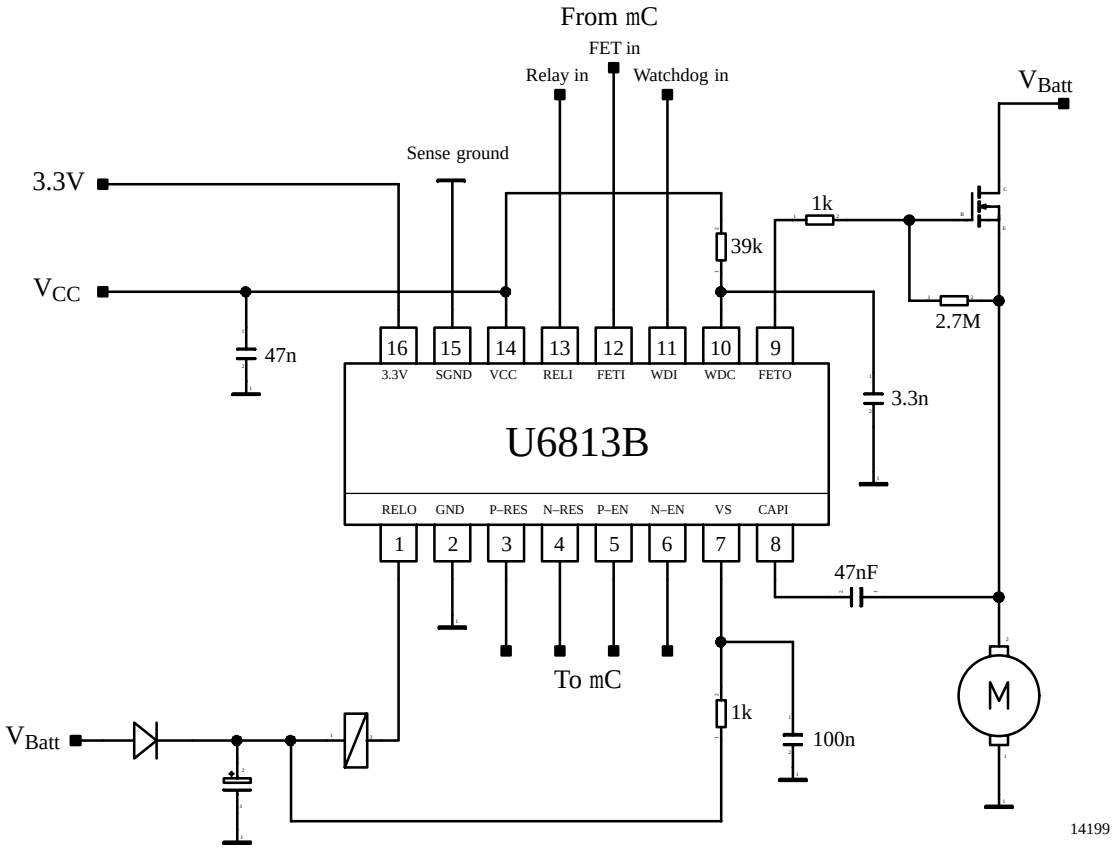


Figure 3. Application circuit

Description of the Watchdog

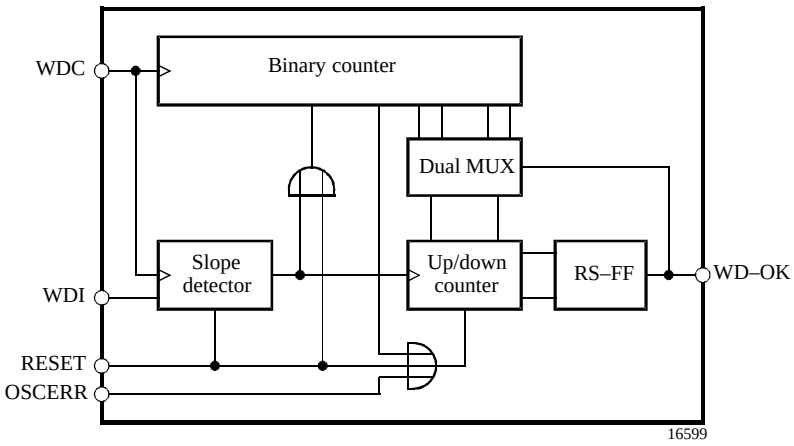


Figure 4. Watchdog block diagram

Abstract

The microcontroller is monitored by a digital window watchdog which accepts an incomming trigger signal of a constant frequency for correct operation. The frequency of the trigger signal can be varied in a broad range as the watchdog‘s time window is determined by external R/C components.

The following description refers to the block diagram (Fig. 4)

WDI Input (Pin 11)

The microcontroller has to provide a trigger signal with the frequency f_{WDI} which is fed to the WDI input. A positive edge of f_{WDI} detected by a slope detector resets the binary counter and clocks the up/down counter additionally.The latter one counts only from 0 to 3 or reverse. Each correct trigger increments the up/down counter by 1, each wrong trigger decrements it by 1. As soon as the counter reaches status 3 the RS flip-flop is set; see Fig. 4 (WD state diagram). A missing incoming trigger signal is detected after 250 clocks of the internal watchdog frequency f_{RC} (see WD OK output) and resets the up/down counter directly.

WDC Input (Pin 10)

With an external R/C circuitry the IC generates a time base (frequency f_{WDC}) independent from the microcontroller. The watchdog‘s time window refers to a frequency of

$f_{WDC} = 100 \square f_{WDI}$

OSCERR Input

A smart watchdog has to ensure that internal problems with its own time base are detected and do not lead to an undesired status of the complete system. If the RC oscillator stops oscillating a signal is fed to the OSCERR input after a timeout delay. It resets the up/down counter and disables the WD-OK output.

Without this reset function the watchdog would freeze its current status when f_{RC} stops.

RESET Input

During power-on and under-/ overvoltage detection a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

WD-OK Output

After the up/down counter is incremented to status 3 (see Fig. 6, WD State Diagram) the RS flip-flop is set and the WD-OK output becomes logic ”1”. As WD-OK is directly connected to the enable pins, the open-collector output P-EN provides also logic ”1” while a logic ”0” is available at N-EN output. If on the other hand the up/down counter is decremented to ”0” the RS flip-flop is reset, the WD-OK output and the P-EN output are logic ”0” and N-EN output is logic ”1”. The WD-OK output also controls a dual MUX stage which shifts the time window by one clock after a successful trigger thus forming a hysteresis to provide stable conditions for the evaluation of the trigger signal ”good or false”. The WD-OK signal is also reset in the case the watchdog counter is not reset after 250 clocks (missing trigger signal)

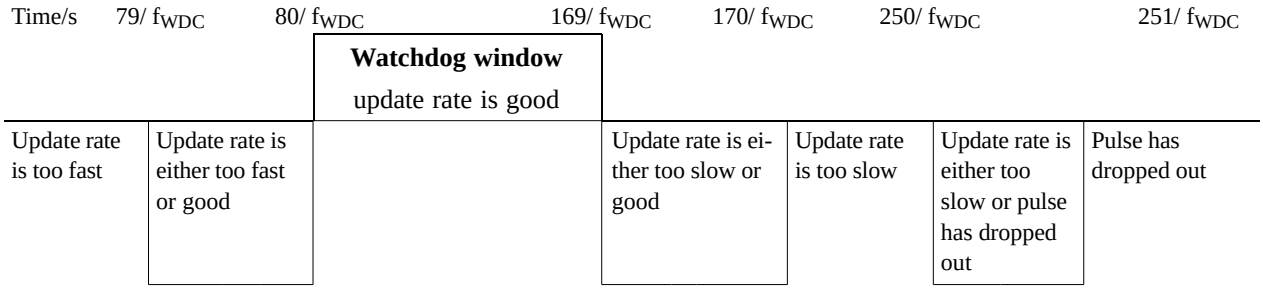


Figure 5. Watchdog timing diagram with tolerances

Watchdog State Diagram

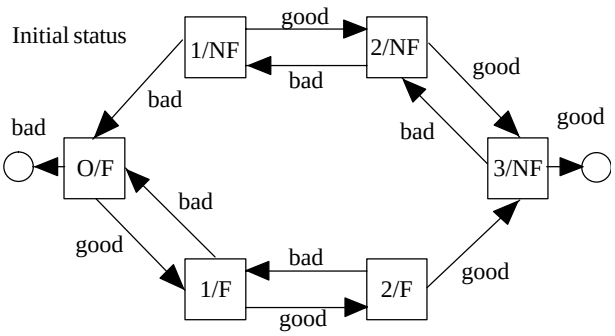


Figure 6. Watchdog state diagram

Explanation

In each block, the first character represents the state of the counter. The second notation indicates the fault status of the counter. A fault status is indicated by an ”F” and a no fault status is indicated by an ”NF”. When the watchdog is powered up initially, the counter starts out at the 0/F block (initial state). ”Good” indicates that a pulse has been received whose width resides within the timing window. ”Bad” indicates that a pulse has been received whose width is either too short or too long.

Watchdog-Window Calculation

Example with recommended values

C_{osc} = 3.3 nF (should be preferably 10%, NPO)

R_{osc}= 39 kW (may be 5%, R_{osc} <100 kW due to leakage current and humidity)

RC Oscillator

t_{WDC} (s) = 10^{-3} ◻ [C_{osc} (nF) ◻ [(0.00078 ◻ R_{osc} (kW)) + 0.0005]]

f_{WDC} (Hz) = 1 / (t_{WDC})

Watchdog WDI

f_{WDI} (Hz) =0.01 ◻ f_{WDC}

t_{WDC} = 100 ms –> f_{WDC} = 10 kHz

f_{WDI} = 100 Hz –> t_{WDI} = 10 ms

WDI pulse width for fault detection after 3 pulses:

Upper watchdog window

Minimum: 169/ f_{WDC} = 16.9 ms –> f_{WDC} / 169 = 59.1 Hz
Maximum: 170/ f_{WDC} = 17.0 ms –> f_{WDC} / 170 = 58.8 Hz

Lower watchdog window

Minimum: 79/ f_{WDC} = 7.9 ms –> f_{WDC} / 79 = 126.6 Hz
Maximum: 80/ f_{WDC} = 8.0 ms –> f_{WDC} / 80 = 125.0 Hz

WDI dropouts for immediate fault detection:

Minimum: 250/ f_{WDC} = 25 ms
Maximum: 251/ f_{WDC} = 25.1 ms

Remarks to Reset Relay

The duration of the over- or undervoltage pulses determines the enable- and reset outputs. A pulse duration shorter than the debounce time has no effect on the outputs. A pulse longer than the debounce time results in the first reset delay. If a pulse appears during this delay, a 2nd delay time is triggered. Therefore the total reset delay time can be longer than specified in the data sheet.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply-voltage range	V_S	– 0.2 to 18	V
Power dissipation V_S = 5 V; T_{amb} = –40°C V_S = 5 V; T_{amb} = 125°C	P_{tot} P_{tot}	250 150	mW mW
Thermal resistance	R_{thja}	110	K/W
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	–40 to 125	°C
Storage temperature range	T_{stg}	–55 to 155	°C

Electrical Characteristics

V_{CC} = 5 V, T_{amb} = –40 to + 125°C; reference pin is GND or SGND (over- and under-voltage detection);
f_{intern} = 200 kHz □ 50% , f_{WDC} = 10 kHz □ 10%; f_{WDI} = 100 Hz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**Pin 14**					
Operation -voltage range		V_{CC}	4.5		5.5	V
Operation-voltage range of RESET outputs		V_{CC}	1.2		18.0	V
Current consumption						
	Relay off T_{amb} = – 40°C @ 5.25 V T_{amb} = 125°C @ 5.25 V	 I_{CC} I_{CC}			 15 10	 mA mA
Digital input WDI	**Pin 11**					
Detection low		V_{WDI}	–0.2		0.3□V_{CC}	V
Detection high		V_{WDI}	0.7□V_{CC}		V_{CC} + 0.2 V	V
Internal pull-down resistor		R_{INT11}	10		40	kΩ
Input current low	Input voltage = 0 V	I_{WDI}	–5		5	µA
Input current high	Input voltage = 5 V	I_{WDI}	100		550	µA
Digital input RELI	**Pin 13**					
Detection low		V_{RELI}	–0.2		0.3 V_{CC}	V
Detection high		V_{RELI}	0.7□V_{CC}		V_{CC} + 0.2 V	V
Internal pull-down resistor		R_{INT13}	10		40	kΩ
Input current low	Input voltage = 0 V	I_{RELI}	–5		5	µA
Input current high	Input voltage = 5 V	I_{RELI}	100		550	µA
Digital input FETI	**Pin 12**					
Detection low		V_{FETI}	–0.2		0.3 V_{CC}	V
Detection high		V_{FETI}	0.7□V_{CC}		V_{CC} + 0.2 V	V
Internal pull-down resistor		R_{INT12}	10		40	kΩ
Input current low	Input voltage = 0 V	I_{FETI}	–5		5	µA
Input current high	Input voltage = 5 V	I_{FETI}	100		550	µA

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Digital output N-RES (open collector)		**Pin 4**				
Saturation voltage low	$I_{reset} \leq 3$ mA	V_{SAT4}			0.5	V
Leakage current	@5V, high state	I_{LEAK4}			0.5	µA
Reset debounce time (switch to low)	Over– or undervoltage	t_{DEB4}	120	320	500	µs
Reset delay (switch back to high)	Over– or undervoltage	t_{DEL4}		50		ms
Digital output P-RES (internal pull-down resistor)		**Pin 3**				
Saturation voltage high	$I_{reset} \leq 0.3$ mA	V_{SAT3}	V_{CC}– 0.5 V		V_{CC}	V
Leakage current	@0 V, low state	I_{LEAK3}			0.5	µA
Internal pull-down resistor	@5 V	R_{INT3}	25		100	kΩ
Reset debounce time (switch to low)	Over– or undervoltage	t_{DEB3}	120	320	500	µs
Reset delay (switch back to high)	Over– or undervoltage	t_{DEL3}		50		ms
Digital output N-EN (with open collector and internal pull-down resistor)		**Pin 6**				
Saturation voltage high	I ≤ 1 mA	V_{SAT6}	V_{CC}– 0.5V		V_{CC}	V
Leakage current	@ 0 V, low state	I_{LEAK6}			0.5	µA
Internal pull down resistor	@ 5 V	R_{INT6}	25		100	kΩ
Enable debounce time (switch to low)	Over– or undervoltage	t_{DEB6}	120	320	500	µs
Enable delay (switch back to high)	Over– or undervoltage	t_{DEL6}		85		ms
Digital output P-EN (internal pull-up resistor)		**Pin 5**				
Saturation voltage high	I ≤ 3 mA	V_{SAT5}			0.5	V
Leakage current	@ 5 V, high state	I_{LEAK5}			0.5	µA
Internal pull-up resistor	@ 0 V	R_{INT5}	12.5		50	kΩ
Enable debounce time (switch to high)	Over– or undervoltage	t_{DEB5}	120	320	500	µs
Enable delay (switch back to low)	Over– or undervoltage	t_{DEL5}		85		ms
Relay driver (RELO)		**Pin 1**				
Saturation voltage	I ≤150 mA	V_{SAT1}	0.1		0.5	V
Current limitation		I_{LIM}	150		300	mA
Clamping voltage		V_{CL}	26		30	V
Turn-off energy			30			mJ
Leakage current	V_{Batt} = 16 V V_{Batt} = 26 V @25°C	I_{LEAK1} I_{LEAK1}	—— ——		20 200	µA µA

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power-FET output FETO *) (max. load capacitor at FET gate 470 pF) **Pin 9**						
Output voltage		V_{OUT9}	V_S + 10 V		V_S + 15 V	V
Operation range		V_S	9		20	V
Overvoltage shut down		V_S	20		24	V
Clamping voltage		V_{CL}	26		30	V
On/off frequency		f			200	Hz
Max. current	FETO	I_{FETO}	10			µA
Max. clamping current		I_{FETO}	5			mA
Leakage current	@FETI = low	I_{LEAK9}			100	µA
Reset and V_{CC} control **Pin 14**						
Lower reset level	Reference SGND	V_{CC}	4.5		4.75	V
Upper reset level	Reference SGND	V_{CC}	5.25		5.5	V
Hysteresis		V_{HYST14}	25		100	mV
Reset debounce time		t_{DEB}	120	320	500	µs
Reset delay		t_{DEL}	20	50	80	ms
Reset and 3.3V control **Pin 16**						
Lower reset level	Reference SGND	$V_{3.3V}$	2.97		3.13	V
Upper reset level	Reference SGND	$V_{3.3V}$	3.47		3.63	V
Hysteresis		V_{HYST16}	15		70	mV
Reset debounce time		t_{DEB16}	120	320	500	µs
Reset delay		t_{DEL16}	20	50	80	ms
RC oscillator WDC **Pin 10**						
Oscillator frequency	R_{OSC} = 39 kΩ C_{OSC} = 3.3 nF	f_{WDC}	9	10	11	kHz
Watchdog timing						
Power-on-reset prolongation time		t_{POR}	34.3		103.1	ms
Detection time for RC-oscillator fault	V_{CR} = const.	$t_{RCerror}$	81.9		246	ms
Time interval for over/under-voltage detection		$t_{D,OUV}$	0.16		0.64	ms
Reaction time of reset output on over/under voltage		$t_{R,OUV}$	0.187		0.72	ms
Nominal frequency for WDI	$f_{RC} = 100 \square f_{WDI}$	f_{WDI}	10		500	Hz
Nominal frequency for WDC	$f_{WDI} = 1/100 \square f_{WDC}$	f_{WDC}	1		50	kHz
Minimum pulse duration for a securely WDI input-pulse detection		$t_{P,WDI}$	182			µs

*) Charge-pump frequency 100 to 300 kHz

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Frequency range for a correct WDI signal		f_{WDI}	64.7		112.5	Hz
Number of incorrect WDI trigger counts for locking the outputs		n_{lock}		3		
Number of correct WDI trigger counts for releasing the outputs		$n_{release}$		3		
Detection time for a stucked WDI signal	V_{WDI} = const.	$t_{WDIerror}$	24.5		25.5	ms
Watchdog timing relative to f_{WDC}						
Minimum pulse duration for a securely WDI input-pulse detection				2		cycles
Frequency range for a correct WDI signal			80		170	cycles
Hysteresis range at the WDI ok margins				1		cycle
Detection time for a stucked WDI signal (WDI dropout)	V_{WDI} = const.		250		251	cycles

Protection against transient voltages according to ISO TR 7637–1 level 4 (except pulse 5)

Pulse	Voltage	Source Resistance *	Rise Time	Duration	Amount
1	– 110 V	10 W	100 V/s	2 ms	15.000
2	+ 110 V	10 W	100 V/s	0.05 ms	15.000
3a	– 160 V	50 W	30 V/ns	0.1 ms	1 h
3b	+ 150 V	50 W	20 V/ns	0.1 ms	1 h
5	55 V	2 W	10 V/ms	250 ms	20

* in the case of the relay driver, the coil resistance of R_{min} = 150 Ω has to be added to the source resistance.

Timing Diagrams

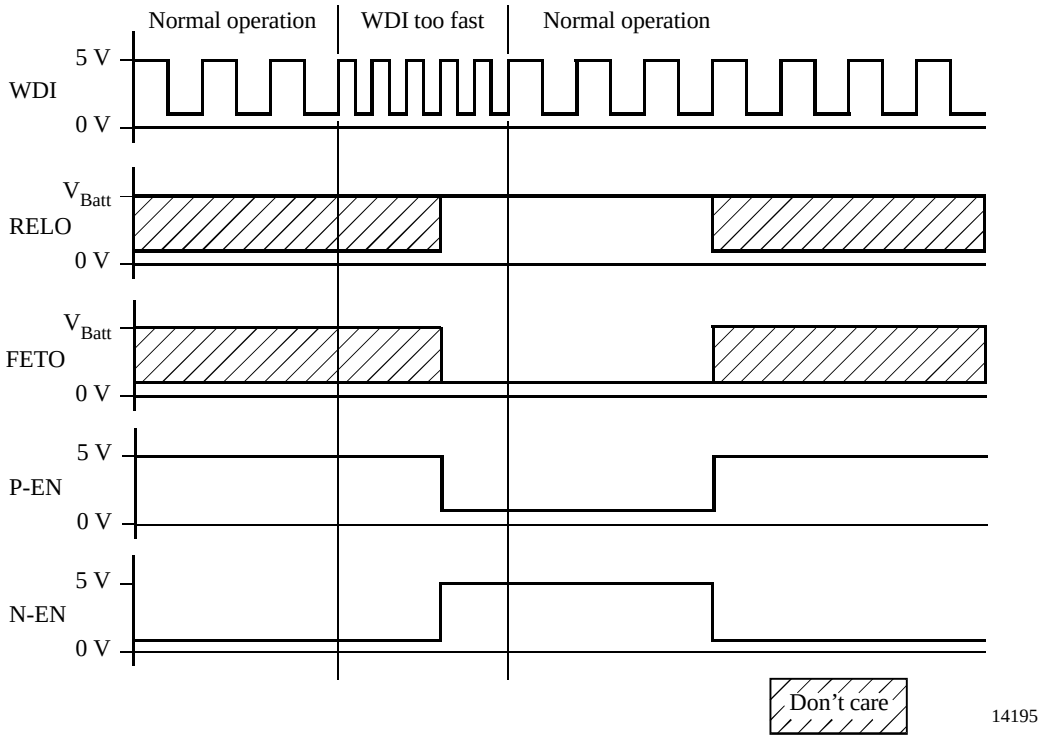


Figure 7. Watchdog in too-fast condition

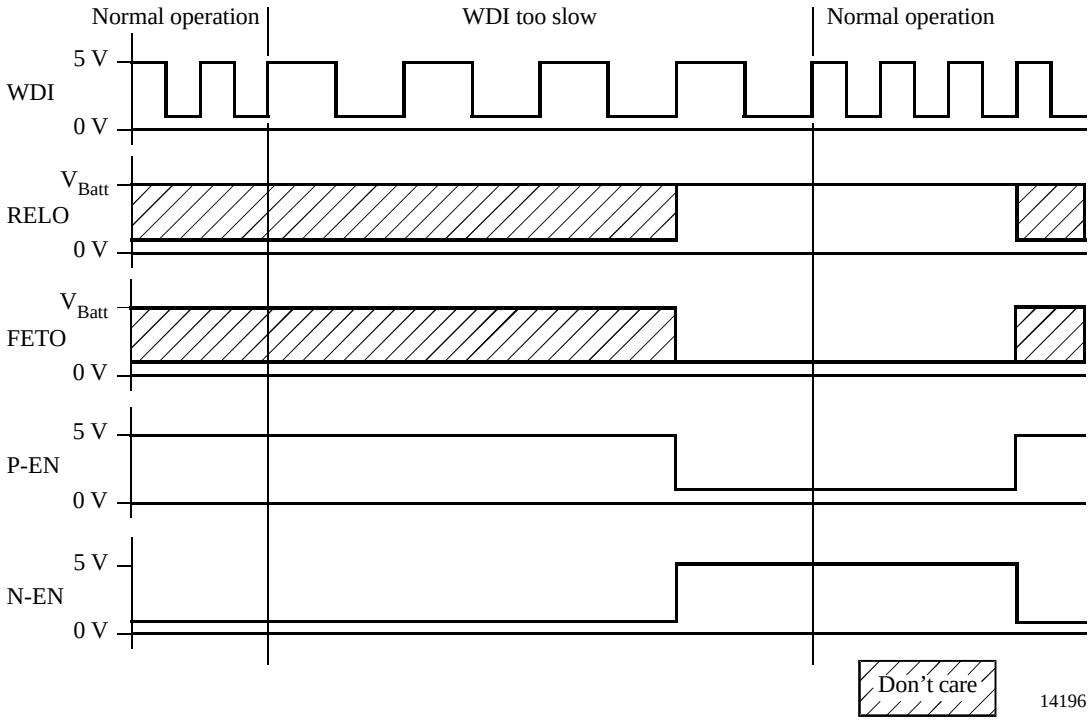


Figure 8. Watchdog in too-slow condition

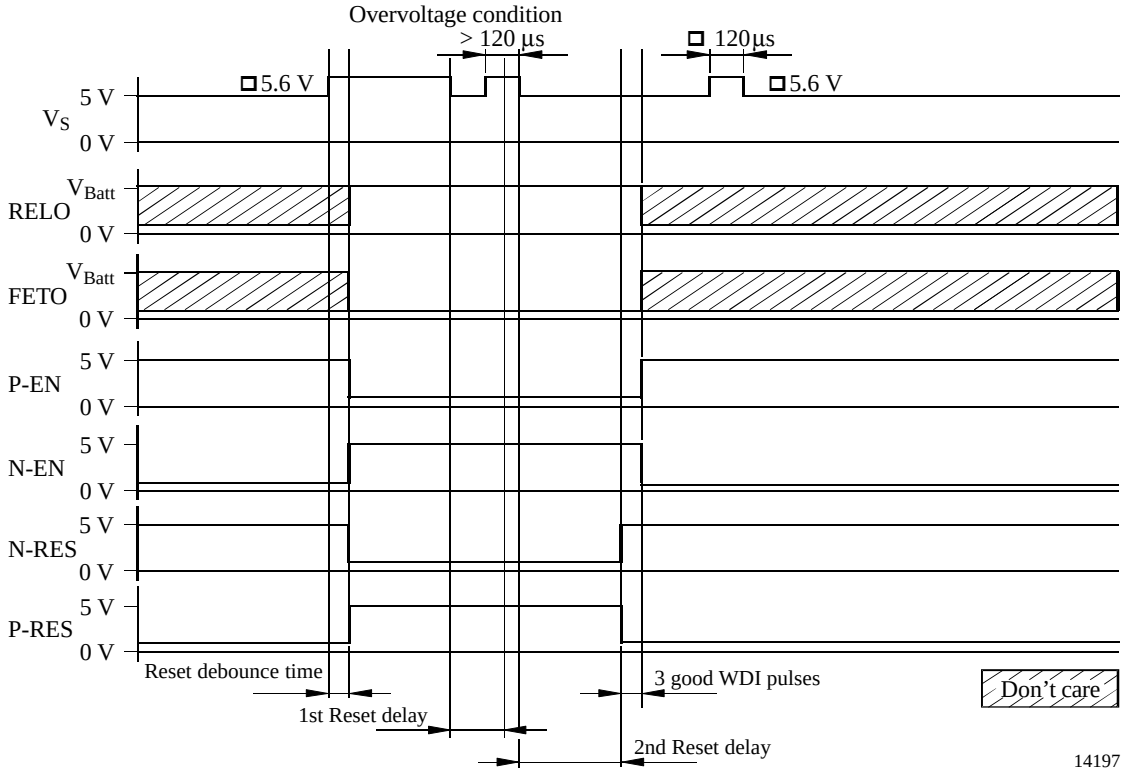


Figure 9. Overvoltage condition

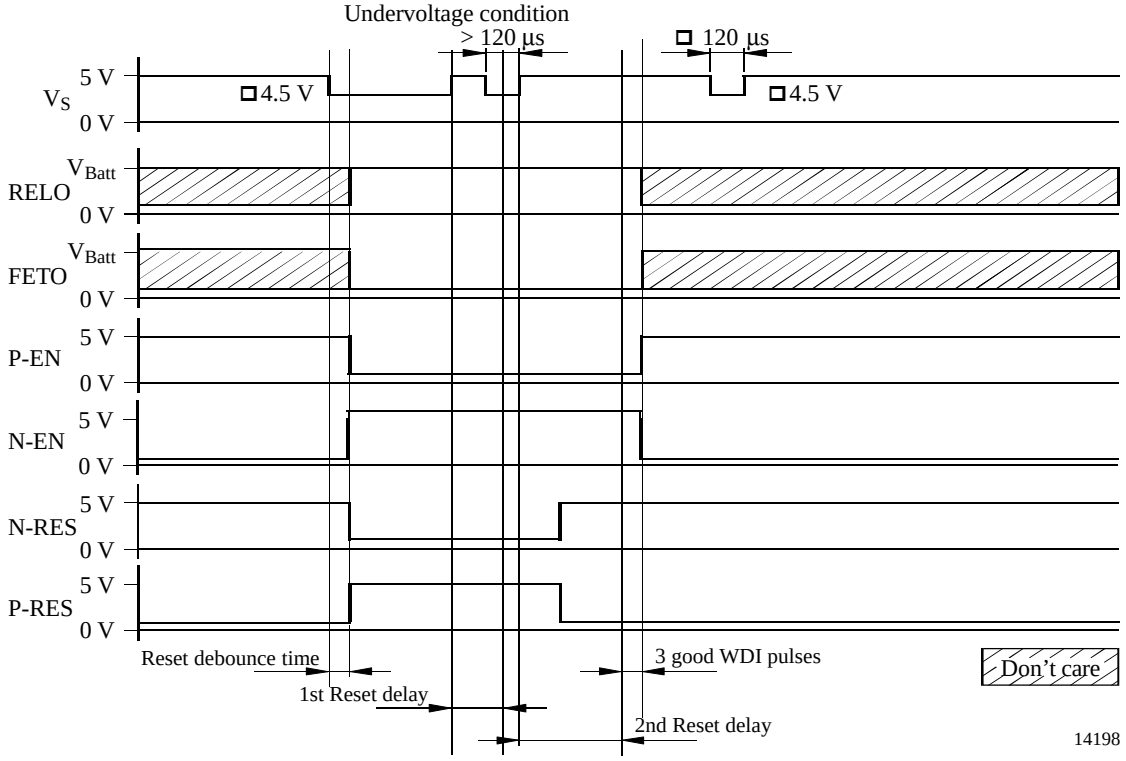
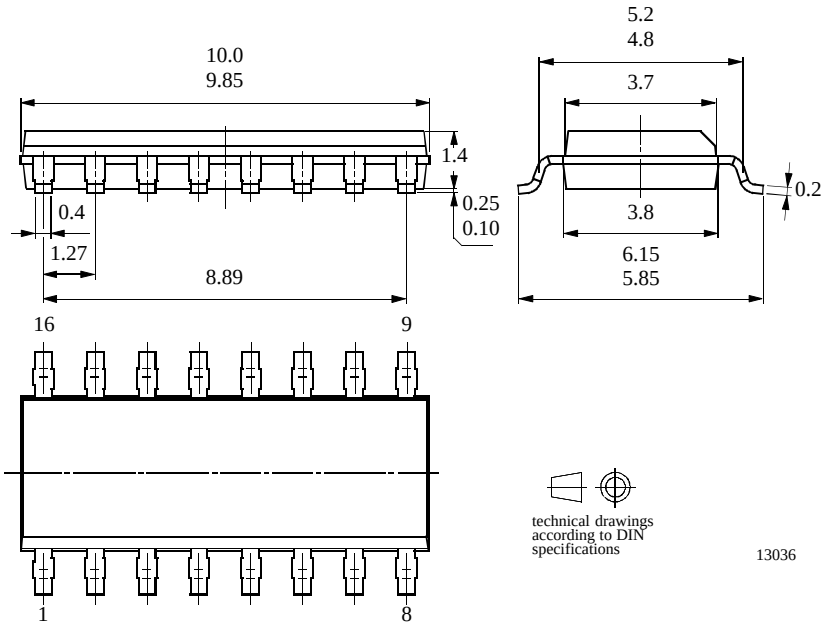


Figure 10. Undervoltage condition

Package Information

Package SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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