AKD4552
Evaluation board Rev.A for AK4552

GENERAL DESCRIPTION

AKD4552 is an evaluation board for the digital audio 24bit A/D and D/A converter, AK4552. The AKD4552 can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards directly. The AKD4552 has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it's easy to evaluate the D/A section. The AKD4552 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4552 --- Evaluation board for AK4552

FUNCTION

- **Compatible with 2 types of interface**
  - **Direct interface with AKM's A/D & D/A converter evaluation boards**
  - **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**

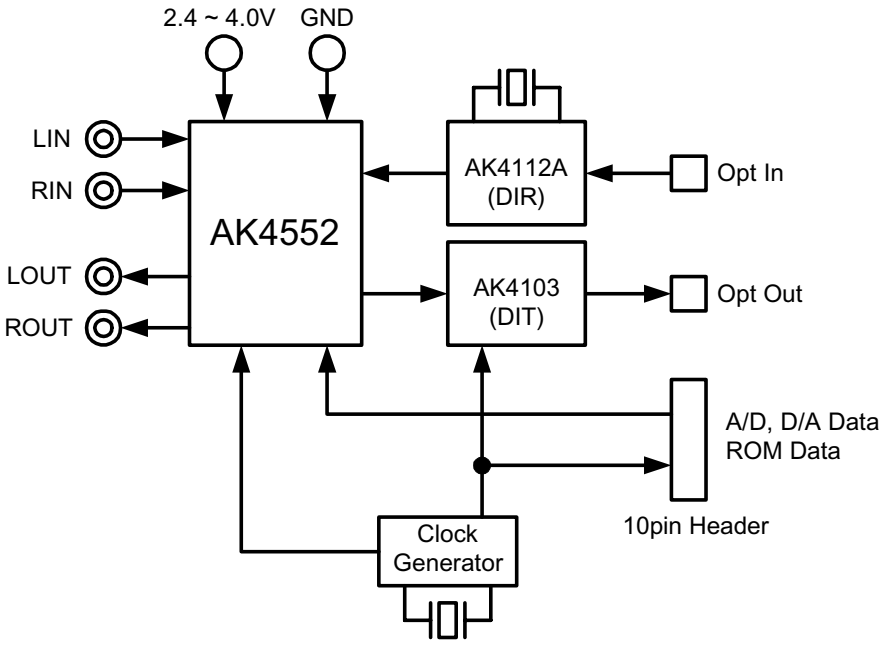


Figure 1. AKD4552 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Analog Input Circuit

External analog signal fed through the BNC connector is terminated by a resistor of 560 ohms. The resistor value should be properly selected in order to meet the output impedance of the signal source.

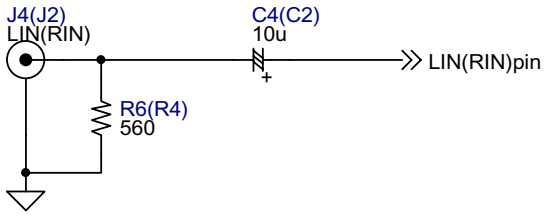


Figure 2. Input buffer circuit on board

* AKM assumes no responsibility for the trouble when using the circuit examples.

■ Analog Output Circuit

The AK4552 includes a combination of switched-capacitor filter (SCF) and continuous-time filter (CTF), so any external filters are not required.

■ Operation sequence

1) Set up the power supply lines.

[VA]	(orange)	= 2.4 ~ 4.0V	: for VA of AK4552 (typ. 3.0V)
[D2V]	(orange)	= 2.4 ~ 4.0V	: for D2V of 74LVC541 (typ. 3.0V)
[VCC]	(red)	= 3.6 ~ 5.0V	: for logic
[AGND]	(black)	= 0V	: for analog ground (including VSS of AK4552)
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.
D2V and VA must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4552 should be reset once bringing SW1 (PDN) “L” upon power-up.

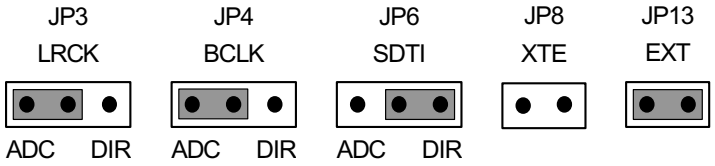
■ Evaluation mode

Applicable Evaluation Mode

(1) Evaluation of A/D using DIT (Optical Link)
(2) Evaluation of D/A using DIR (Optical Link)
(3) Evaluation of loopback mode (default)
(4) Evaluation of D/A using ideal sine wave generated by ROM data
(5) Evaluation of D/A using A/D converted data
(6) Evaluation of A/D using D/A converted data
(7) All interface signals including master clock are fed externally.

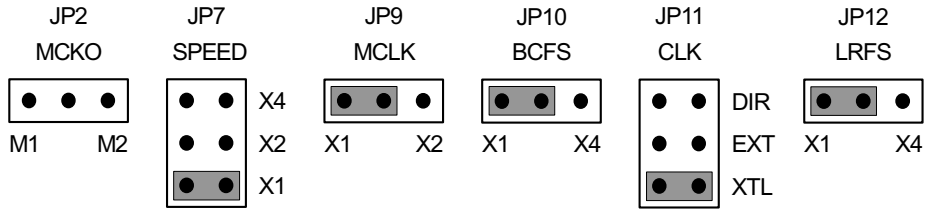
(1) Evaluation of A/D using DIT (Optical Link)

PORT2 (DIT) and X2 (X'tal) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. Nothing should be connected to PORT1 (DIR), PORT3 (ROM). In case of using external clock through a BNC connector (J5), select EXT on JP11 (CLK) and short JP8 (XTE) and open JP13 (EXT). AK4112A should be powered down.

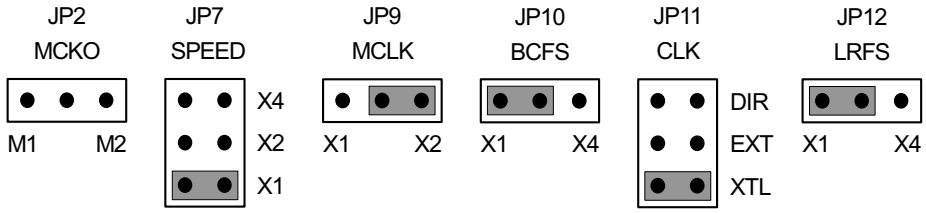


• Clock example

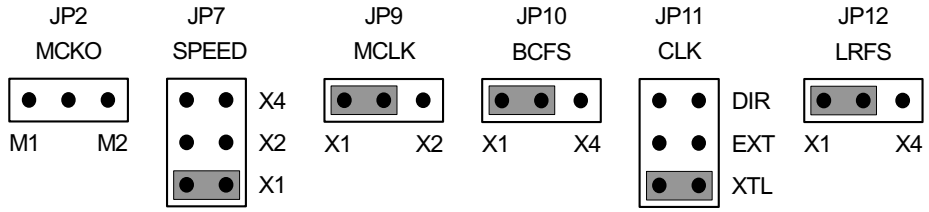
1-1) Normal speed of ADC (MCLK=256fs)
Master clock frequency example of X2 : X2 = 8.192MHz, 11.2896MHz, 12.288MHz



1-2) Normal speed of ADC (MCLK=512fs)
Master clock frequency example of X2 : X2 = 16.384MHz, 22.5792MHz, 24.576MHz

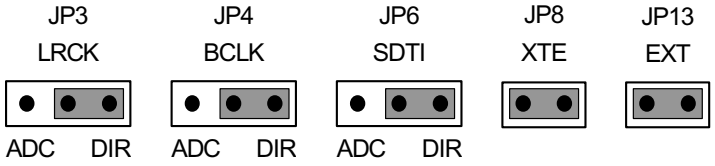


1-3) Double speed of ADC (MCLK=256fs)
Master clock frequency example of X2 : X2 = 16.384MHz, 22.5792MHz, 24.576MHz



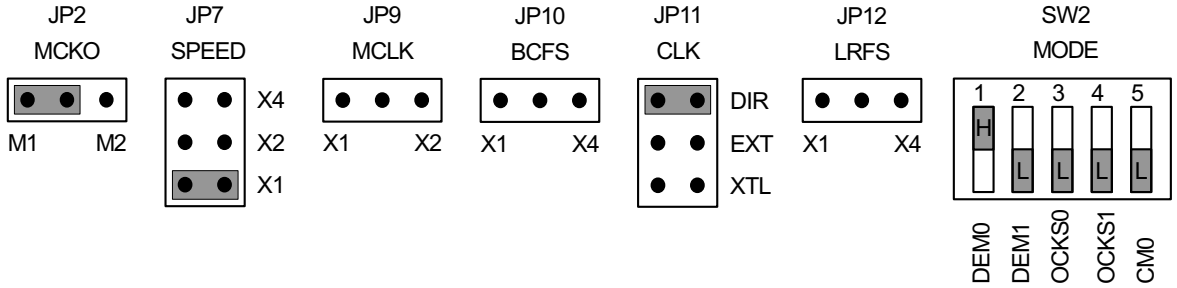
(2) Evaluation of D/A using DIR (Optical Link)

PORT1 (DIR) is used. DIR generates MCLK, BCLK, LRCK and SDATA from the received data through optical connector (TORX176). Used for the evaluation using CD test disk. Nothing should be connected to PORT3 (ROM). Set up "H" (AK4112A : PLL mode) for SW2-5 (CM0).

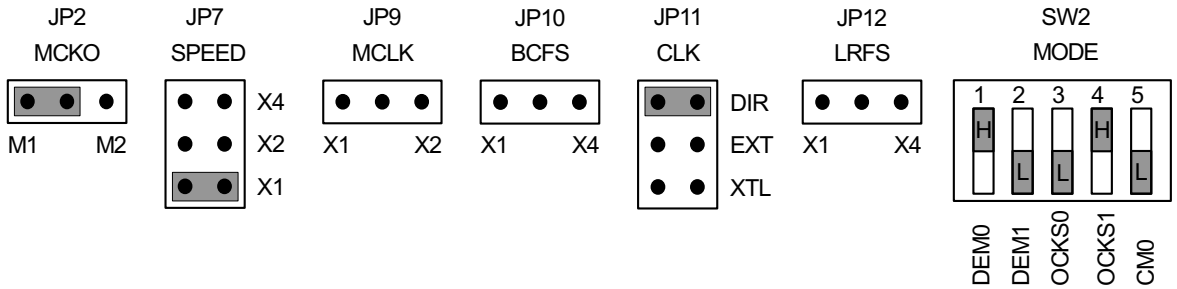


• Clock example

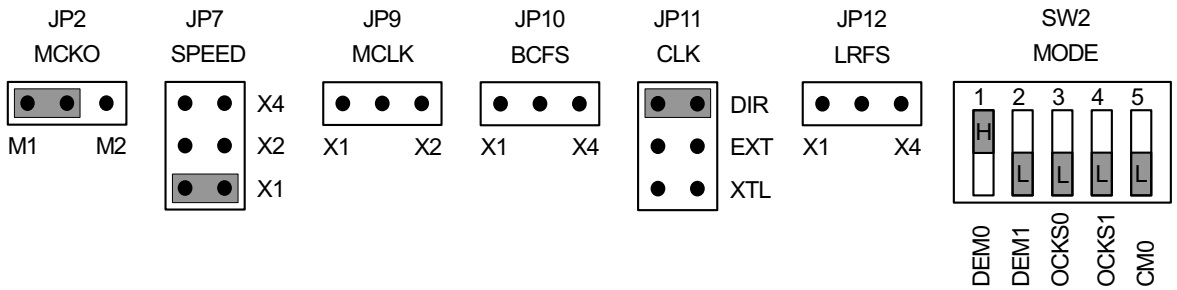
2-1) Normal speed of DAC (MCLK=256fs)
Input fs example for PORT1 : fs = 32kHz, 44.1kHz, 48kHz



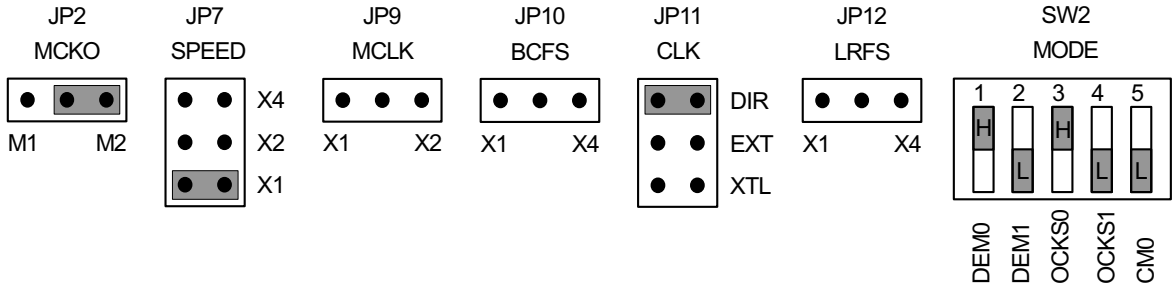
2-2) Normal speed of DAC (MCLK=512fs)
Input fs example for PORT1 : fs = 32kHz, 44.1kHz, 48kHz



2-3) Double speed of DAC (MCLK=256fs)
Input fs example for PORT1 : fs = 64kHz, 88.2kHz, 96kHz

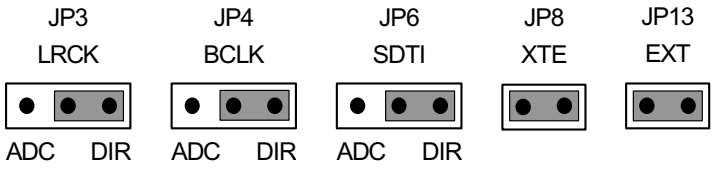


2-4) 1/2 decimation of DAC (MCLK=128fs)
Input fs example for PORT1 : fs = 64kHz, 88.2kHz, 96kHz



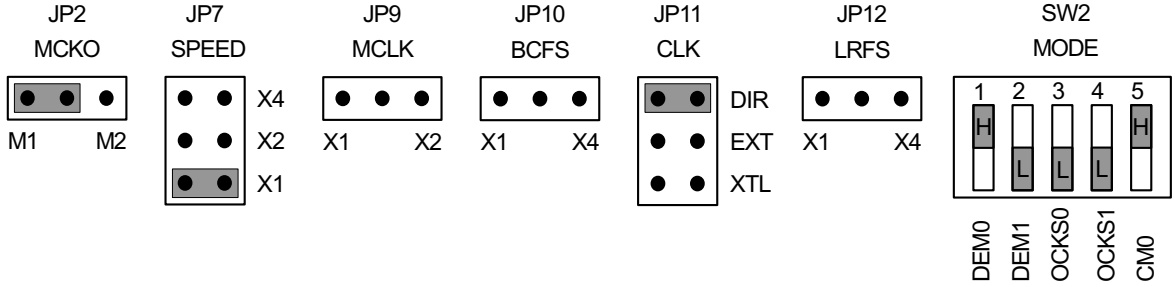
(3) Evaluation of loopback mode (default)

Using U4 (AK4112A) and X1 (X'tal). Nothing should be connected to PORT1 (DIR), PORT3 (ROM). Set up "H" (AK4112A : X'tal mode) for SW2-5 (CM0).

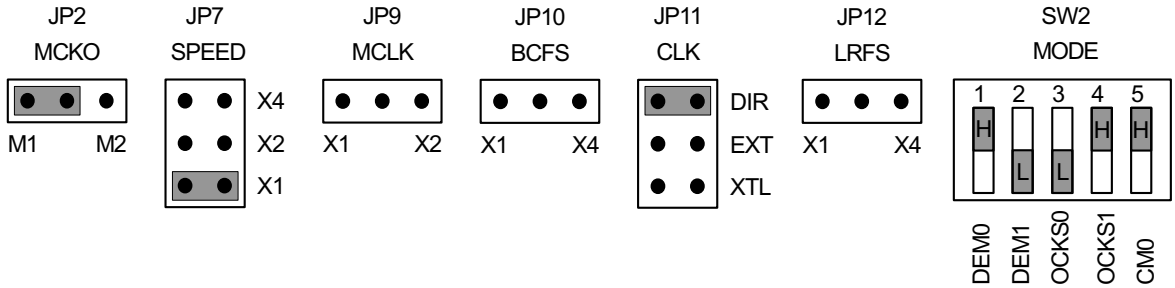


- Clock example

3-1) Normal speed (MCLK=256fs)
Master clock frequency example of X1 : X1 = 8.192MHz, 11.2896MHz, 12.288MHz

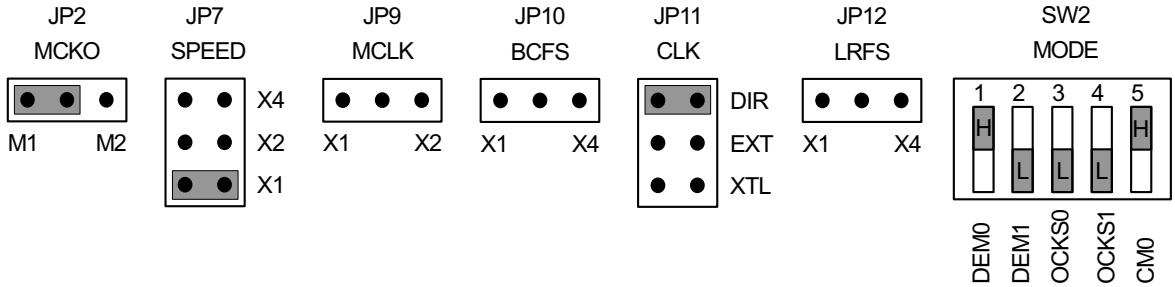


3-2) Normal speed (MCLK=512fs)
Master clock frequency example of X1 : X1 = 16.384MHz, 22.5792MHz, 24.576MHz



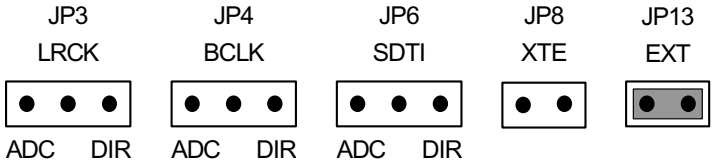
3-3) Double speed (MCLK=256fs)

Master clock frequency example of X1 : X1 = 16.384MHz, 22.5792MHz, 24.576MHz



(4) Evaluation of D/A using ideal sine wave generated by ROM data

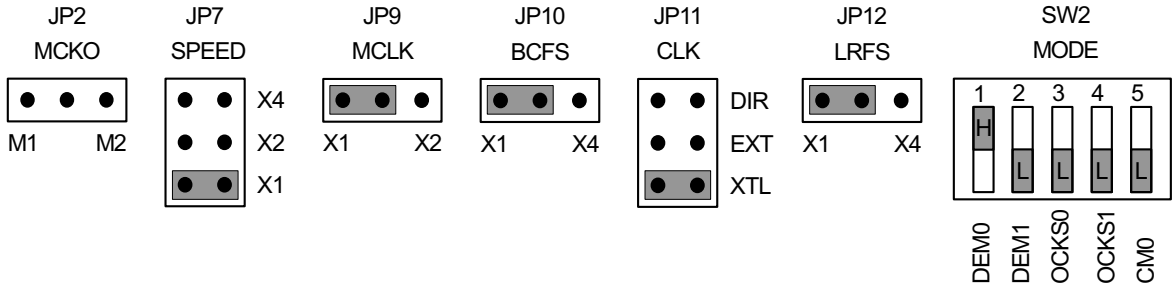
Digital signals generated by AKD43XX are used. PORT3 (ROM) is used for the interface with AKD43XX. Master clock is sent from AKD4552 to AKD43XX and BCLK, LRCK, SDTI are sent from AKD43XX to AKD4552. Nothing should be connected to PORT1 (DIR). In case of using external clock through a BNC connector (J5), select EXT on JP11 (CLK) and short JP8 (XTE) and open JP13 (EXT).



- Clock example

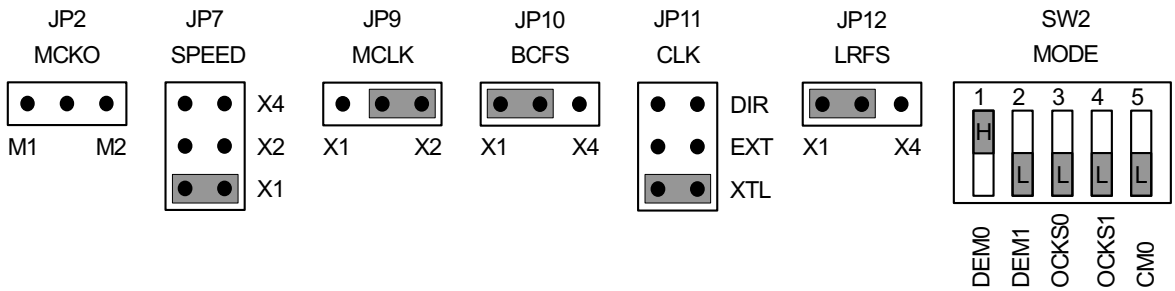
4-1) Normal speed of DAC (MCLK=256fs)

Master clock frequency example of X2 : X2 = 8.192MHz, 11.2896MHz, 12.288MHz



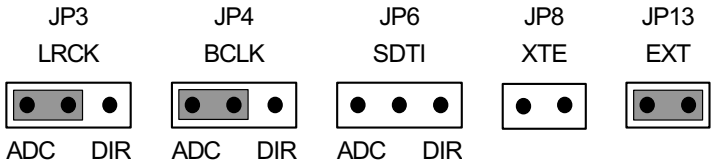
4-2) Normal speed of DAC (MCLK=512fs)

Master clock frequency example of X2 : X2 = 16.384MHz, 22.5792MHz, 24.576MHz



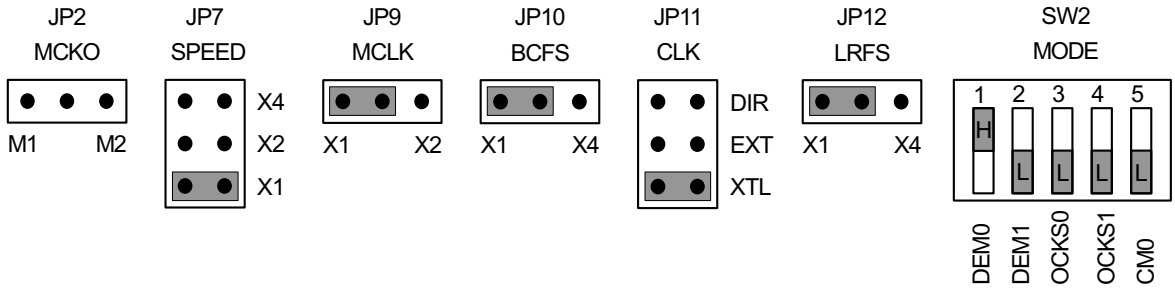
(5) Evaluation of D/A using A/D converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards with PORT3 (ROM). Nothing should be connected to PORT1 (DIR). In case of using external clock through a BNC connector (J5), select EXT on JP11 (CLK) and short JP8 (XTE) and open JP13 (EXT). This mode corresponds to normal speed only.

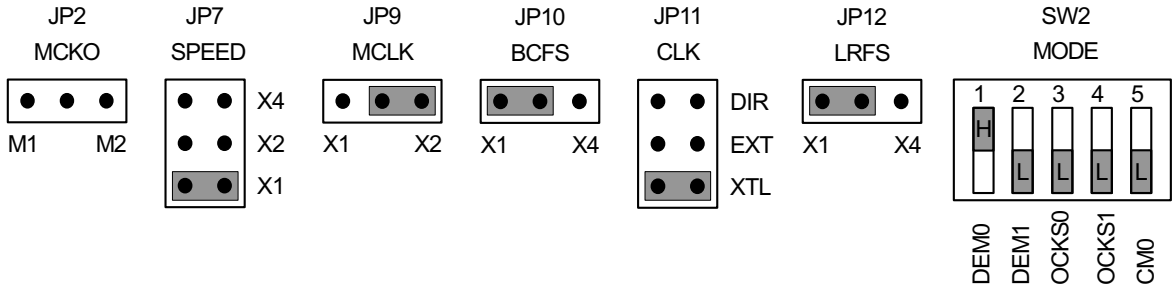


• Clock example

5-1) Normal speed of DAC (MCLK=256fs)
Master clock frequency example of X2 : X2 = 8.192MHz, 11.2896MHz, 12.288MHz

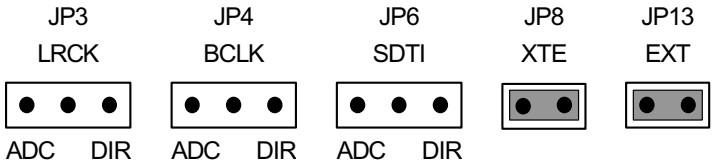


5-2) Normal speed of DAC (MCLK=512fs)
Master clock frequency example of X2 : X2 = 16.384MHz, 22.5792MHz, 24.576MHz



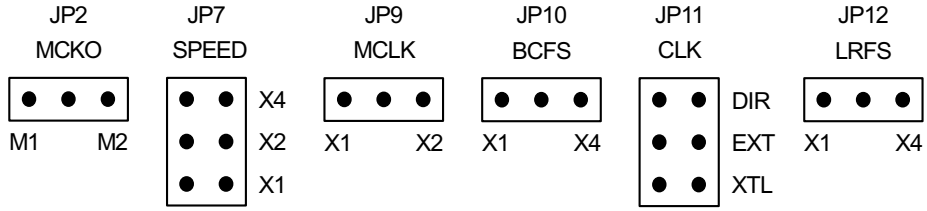
(6) Evaluation of A/D using D/A converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards with PORT3 (ROM). Nothing should be connected to PORT1 (DIR).

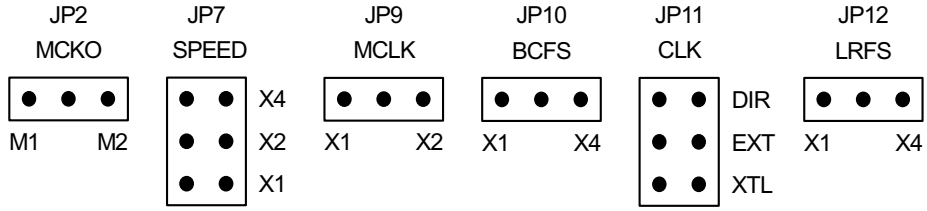


- Clock example

6-1) Normal speed of ADC (MCLK=256fs)
Do not use X2.

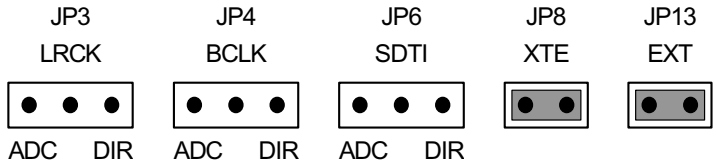


6-2) Normal speed of ADC (MCLK=512fs)
Do not use X2.



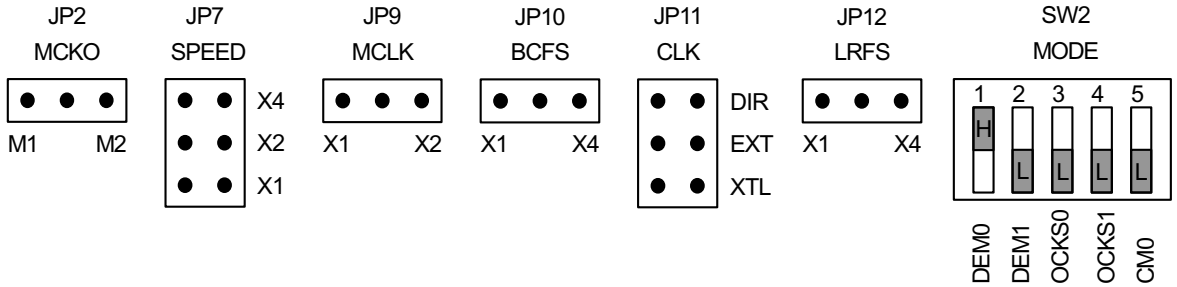
(7) All interface signals including master clock are fed externally.

Under the following set-up, all external signals needed for the AK4552 to operate could be fed through PORT3 (ROM). In case of interfacing external sources to D/A converter, JP6 (SDTI) should be open. And in case of using A/D data to externally, JP6 (SDTI) is set ADC side. When JP6 (SDTI) is open, the A/D data can be output from the SDTO pin of PORT3 (ROM) at the same time if JP5 (SDTO) is short.



• Clock example

7-1) Normal speed, Double speed, 4 times speed of ADC and DAC
Do not use X2.



■ DIP switch set up

Upper-side is “H” and lower-side is “L”.

[SW2] (MODE) : Sets the de-emphasis filter of AK4552 and clock mode of U4 (AK4112A).

No.	Pin Name	Mode
1	DEM0	See Table 2.
2	DEM1	
3	OCKS0	See Table 3.
4	OCKS1	
5	CM0	L : X’tal mode, H : PLL mode

Table 1. Set up SW2

DEM1	DEM0	Mode	
L	L	44.1kHz	
L	H	OFF	default
H	L	48kHz	
H	H	32kHz	

Table 2. Set up of DEM0/1 of AK4552

No.	OCKS1	OCKS0	MCKO1	MCKO2	fs (kHz)
0	L	L	256fs	256fs	32, 44.1, 48, 96
1	H	L	512fs	128fs	32, 44.1, 48

Table 3. Set up of OCKS0/1 for AK4112A

■ Other jumper pins set up

[JP1] (GND): Analog ground and digital ground
open: separated
short: common (The connector “DGND” can be open.) <default>

[JP5] (SDTO): SDTO of AK4552
Always open. It is possible to short for evaluation mode 7.

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (PDN): Resets the AK4552. Keep “H” during normal operation.
[SW3] (DIR): Resets the AK4112A. Keep “H” during normal operation.
[SW4] (DIT): Resets the AK4103. Keep “H” during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor ERF pin of the AK4112A. LED turns on when some error has occurred to AK4112A.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System two Cascade
- MCLK : 256fs
- BCLK : 64fs
- fs : 32kHz, 44.1kHz, 48kHz, 96kHz
- Bit : 24bit
- Band width : ADC : 10Hz ~ 20kHz (Normal Speed), 10Hz ~ 48kHz (Double Speed)
- Measurement Filter : DAC : 10Hz ~ 20kHz (Normal Speed), 10Hz ~ 40kHz (Double Speed)
- Power Supply : VA = VD = 3.0V
- Interface : DIT/DIR
- Temperature : Room

Parameter		Result (Lch / Rch)	Unit
ADC Analog Input Characteristics			
S/(N+D) (-0.5dB Input)	fs=32kHz	87.8 / 87.9	dB
	fs=44.1kHz	88.5 / 88.5	dB
	fs=48kHz	89.2 / 89.2	dB
	fs=96kHz	89.5 / 89.4	dB
D-Range (-60dB Input)	fs=32kHz, A-weighted	96.1 / 96.1	dB
	fs=44.1kHz, A-weighted	97.1 / 97.1	dB
	fs=48kHz, A-weighted	97.5 / 97.5	dB
	fs=96kHz	93.3 / 93.3	dB
S/N	fs=32kHz, A-weighted	96.1 / 96.1	dB
	fs=44.1kHz, A-weighted	97.1 / 97.1	dB
	fs=48kHz, A-weighted	97.6 / 97.6	dB
	fs=96kHz	93.3 / 93.3	dB
Interchannel Isolation		118.5 / 118.7	dB
DAC Analog Output Characteristics			
S/(N+D) (0dB Output)	fs=32kHz	88.3 / 89.2	dB
	fs=44.1kHz	88.1 / 88.8	dB
	fs=48kHz	88.3 / 89.2	dB
	fs=96kHz	85.6 / 86.3	dB
D-Range (-60dB Output)	fs=32kHz, A-weighted	100.0 / 100.0	dB
	fs=44.1kHz, A-weighted	100.4 / 100.4	dB
	fs=48kHz, A-weighted	100.6 / 100.6	dB
	fs=96kHz	95.6 / 95.6	dB
S/N	fs=32kHz, A-weighted	100.9 / 100.9	dB
	fs=44.1kHz, A-weighted	101.6 / 101.6	dB
	fs=48kHz, A-weighted	101.6 / 101.6	dB
	fs=96kHz	96.0 / 96.0	dB
Interchannel Isolation		116.2 / 116.4	dB

1. ADC (Normal Speed)

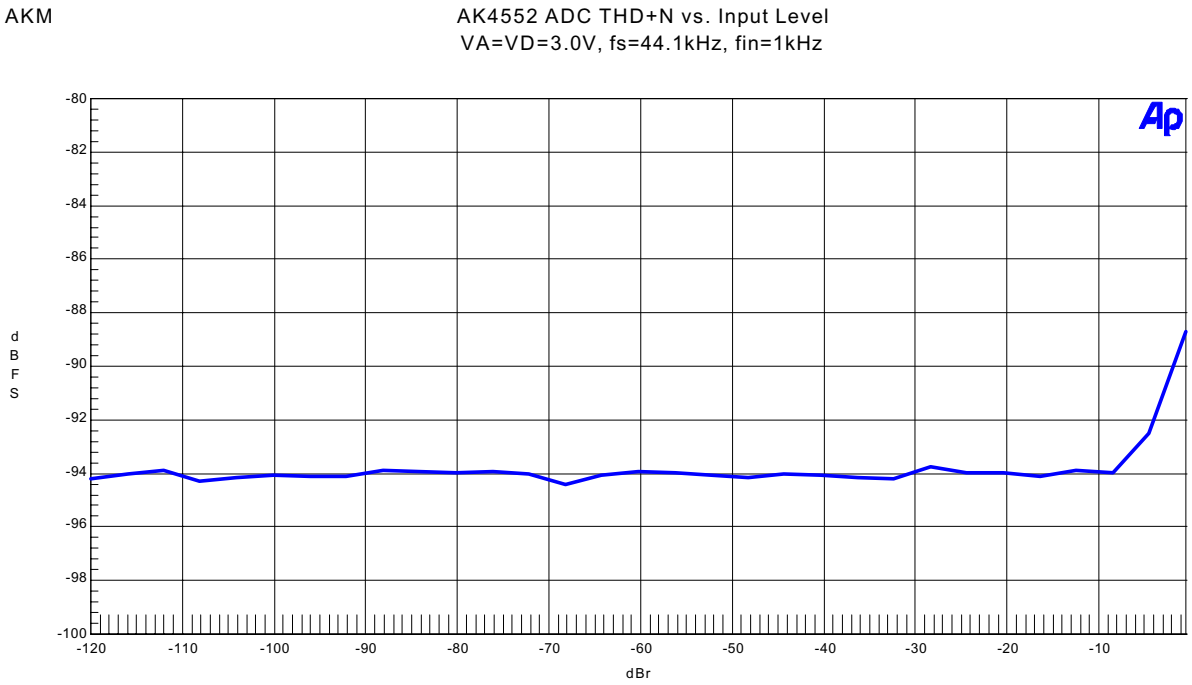


Figure 1. THD+N vs. Input Level

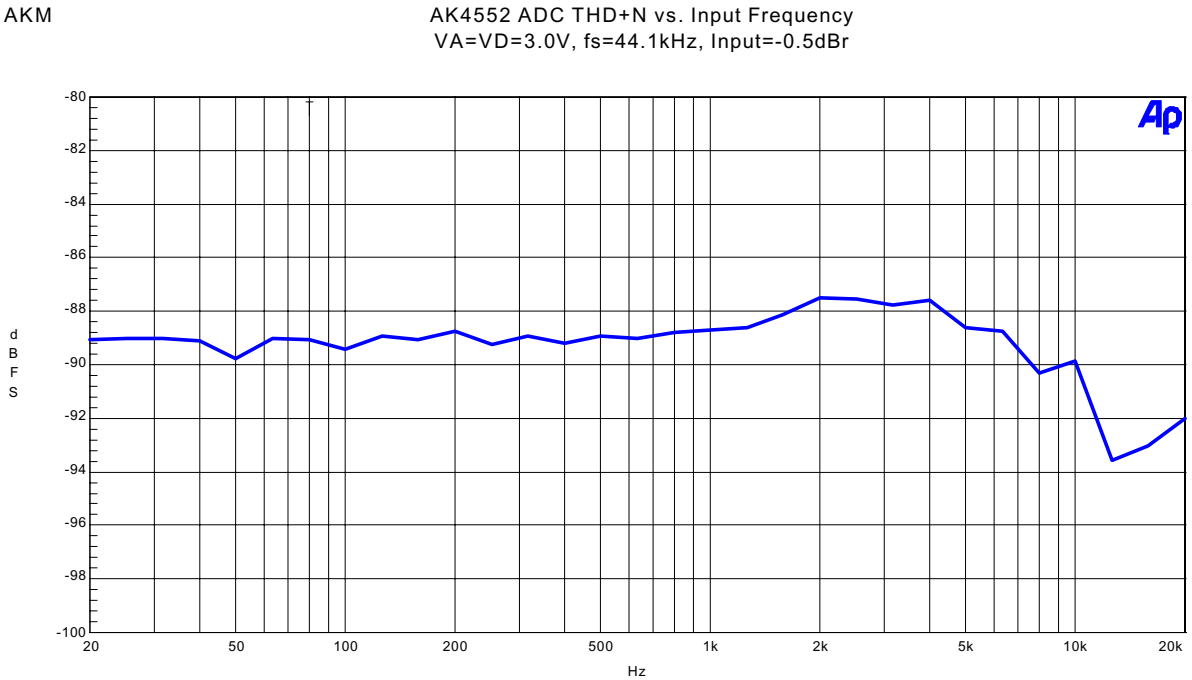


Figure 2. THD+N vs. Input Frequency

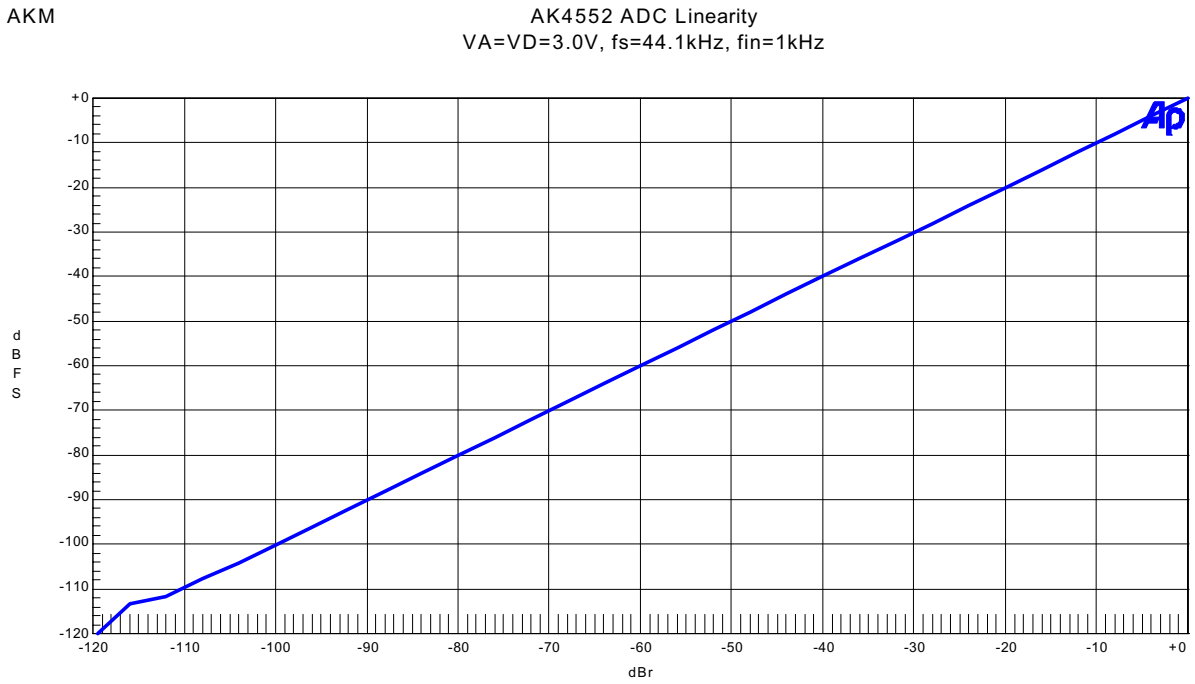


Figure 3. Linearity

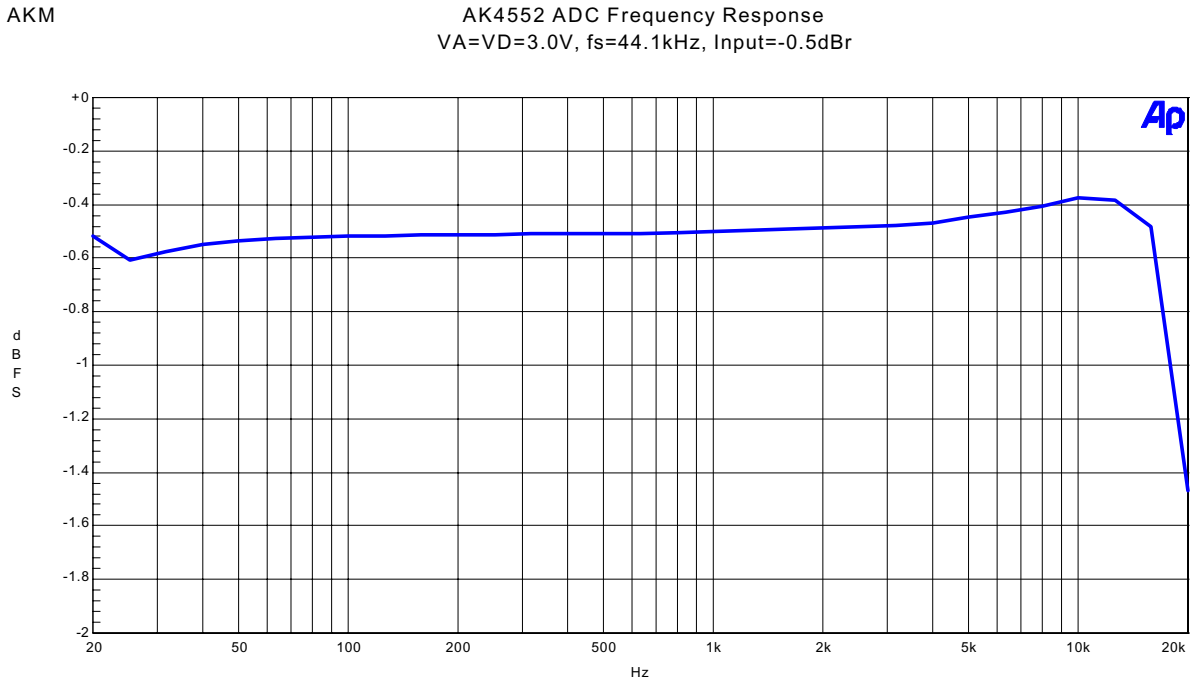


Figure 4. Frequency Response

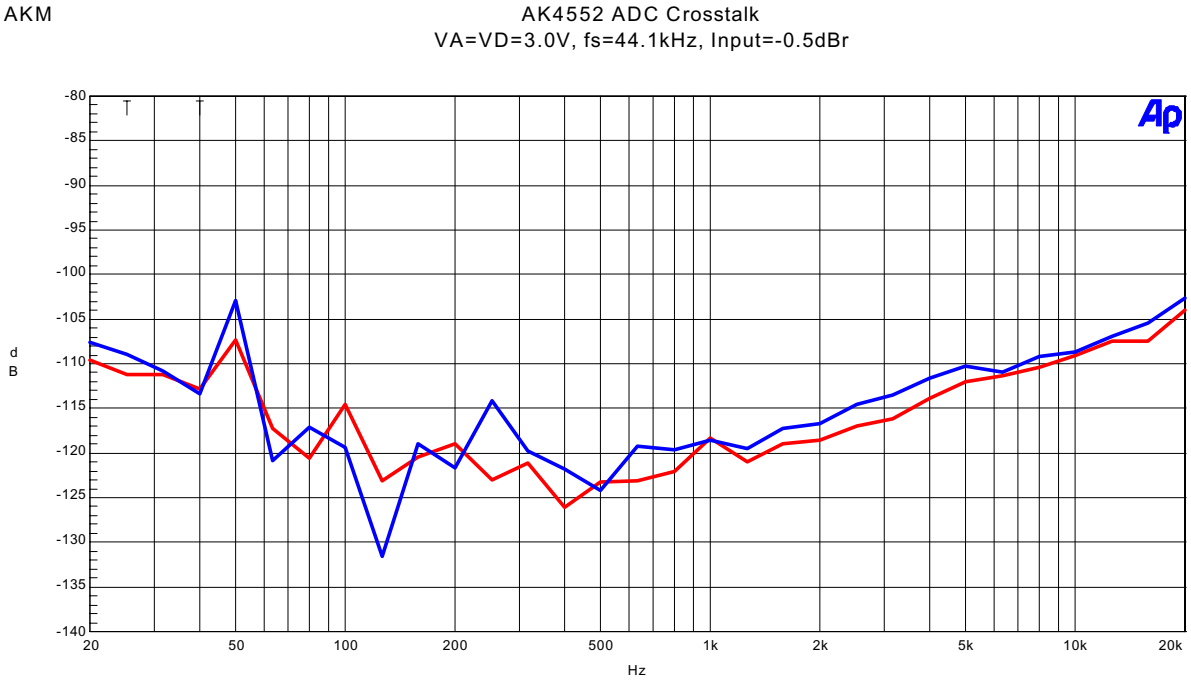


Figure 5. Crosstalk

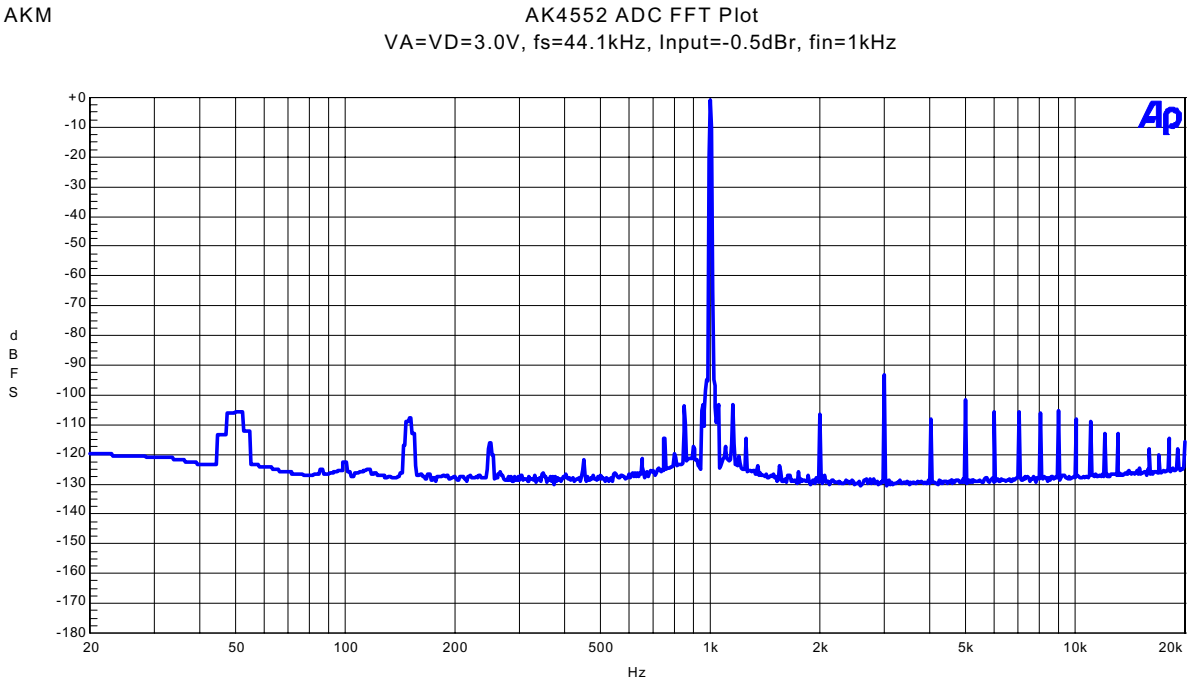


Figure 6. FFT Plot

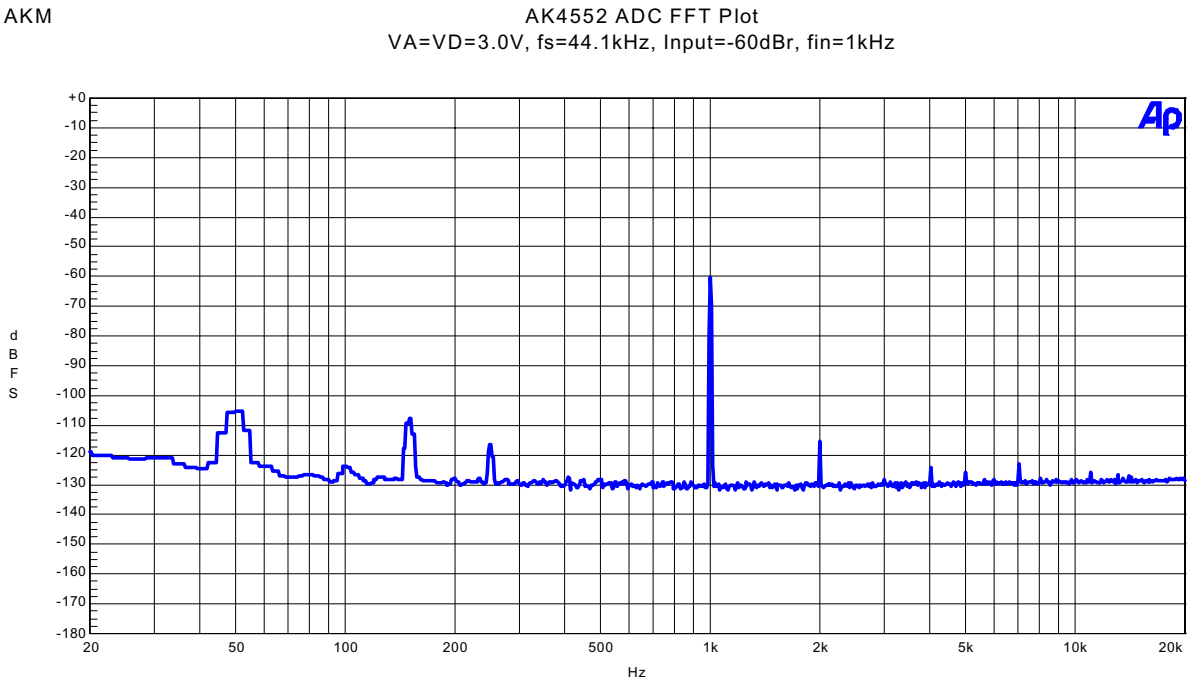


Figure 7. FFT Plot

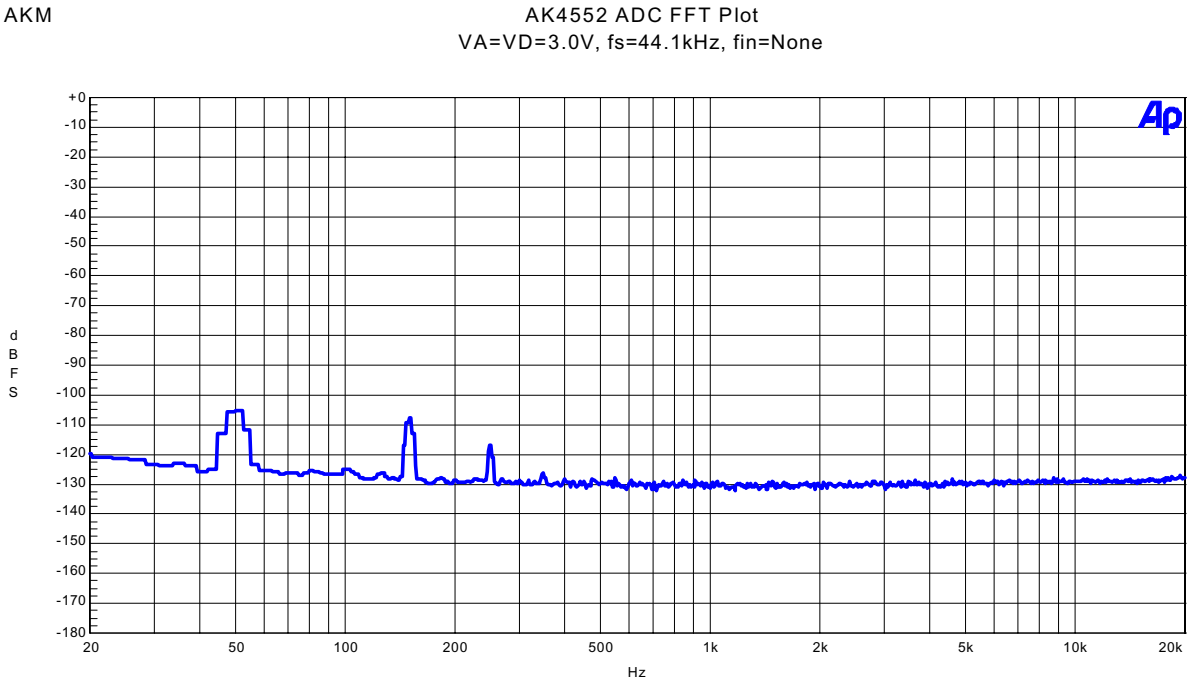


Figure 8. FFT Plot

2. DAC (Normal Speed)

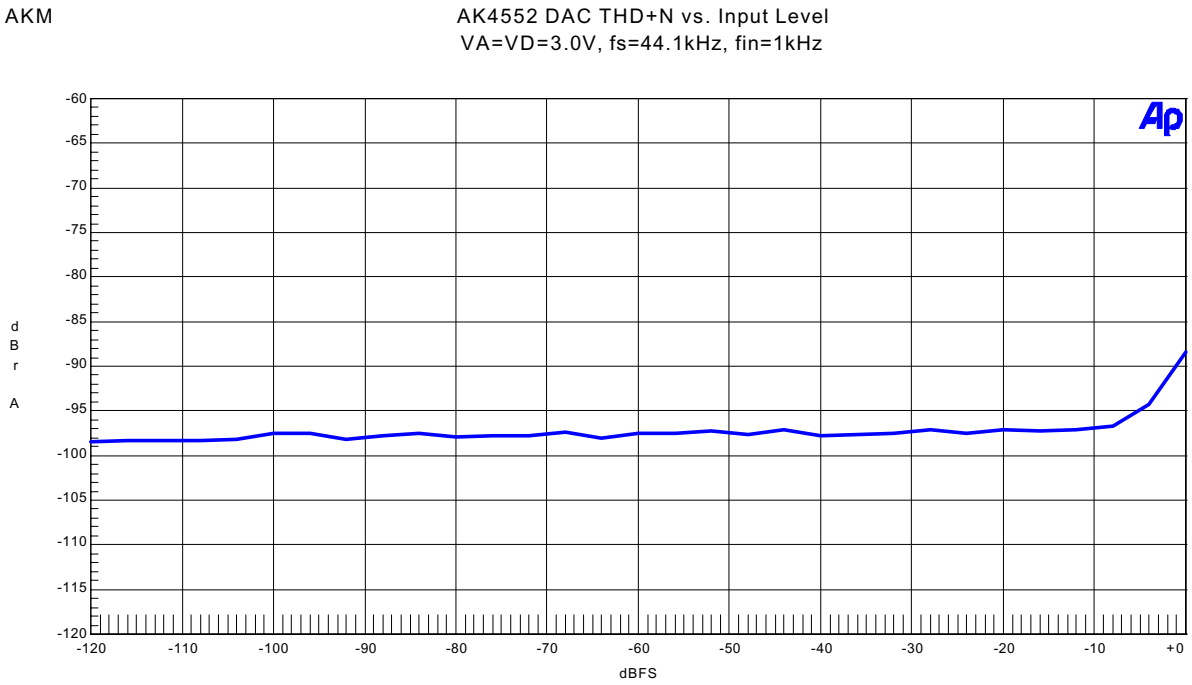


Figure 1. THD+N vs. Input Level

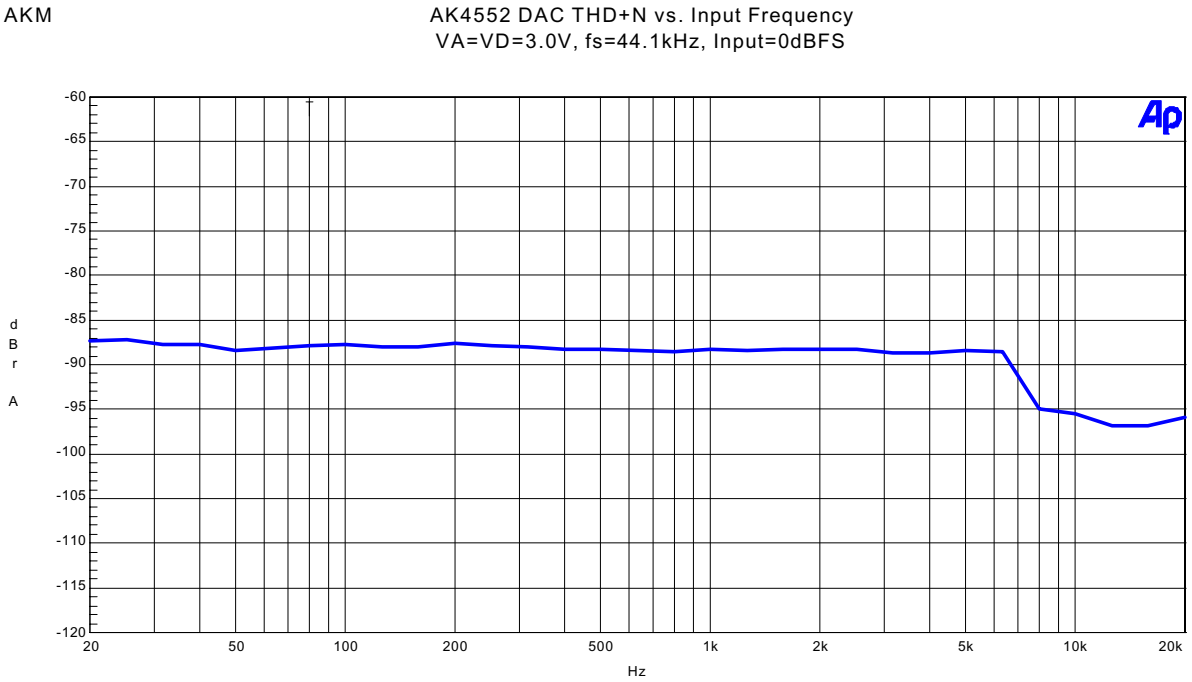


Figure 2. THD+N vs. Input Frequency

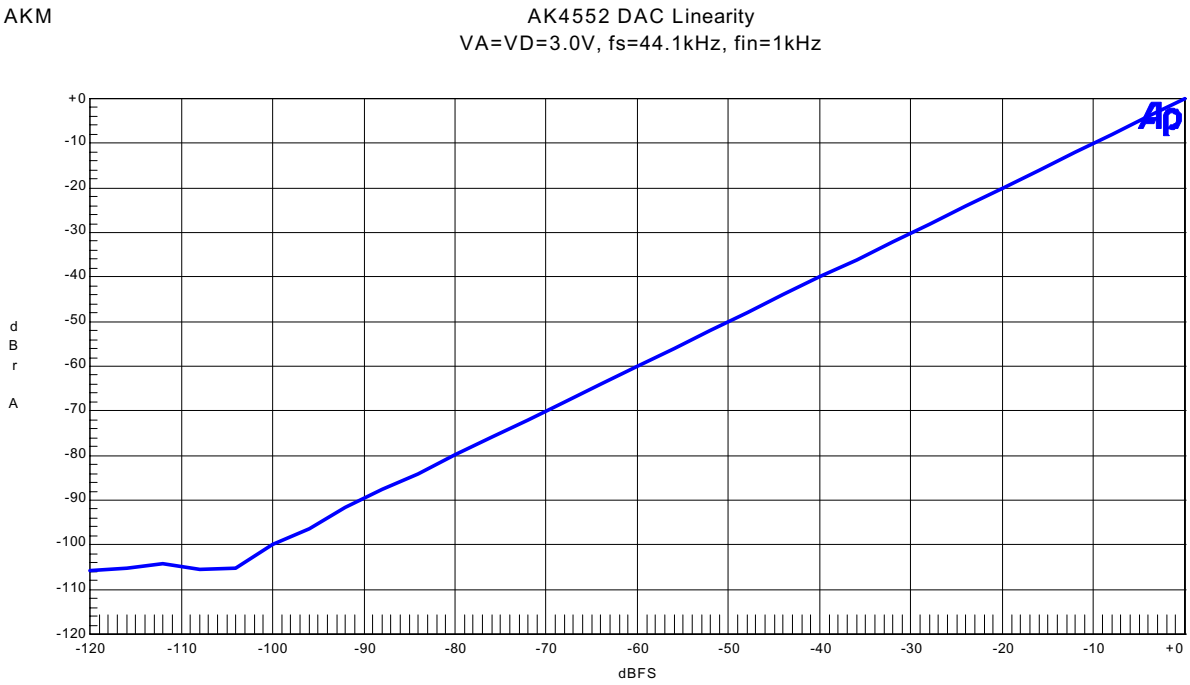


Figure 3. Linearity

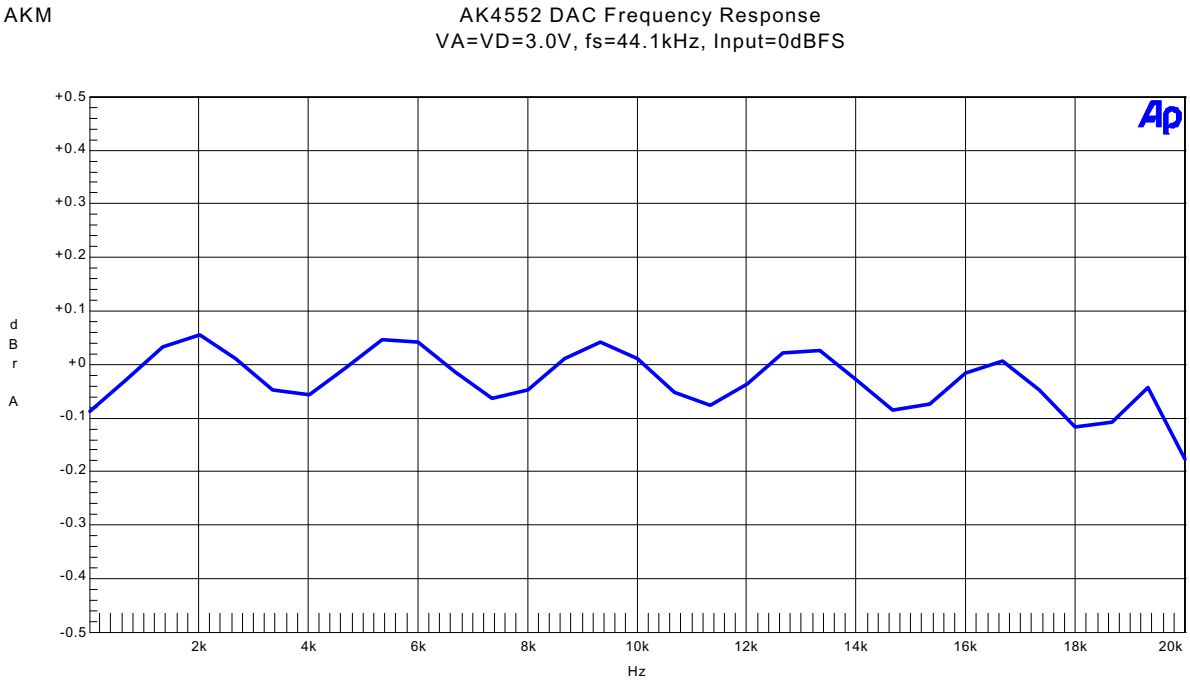


Figure 4. Frequency Response

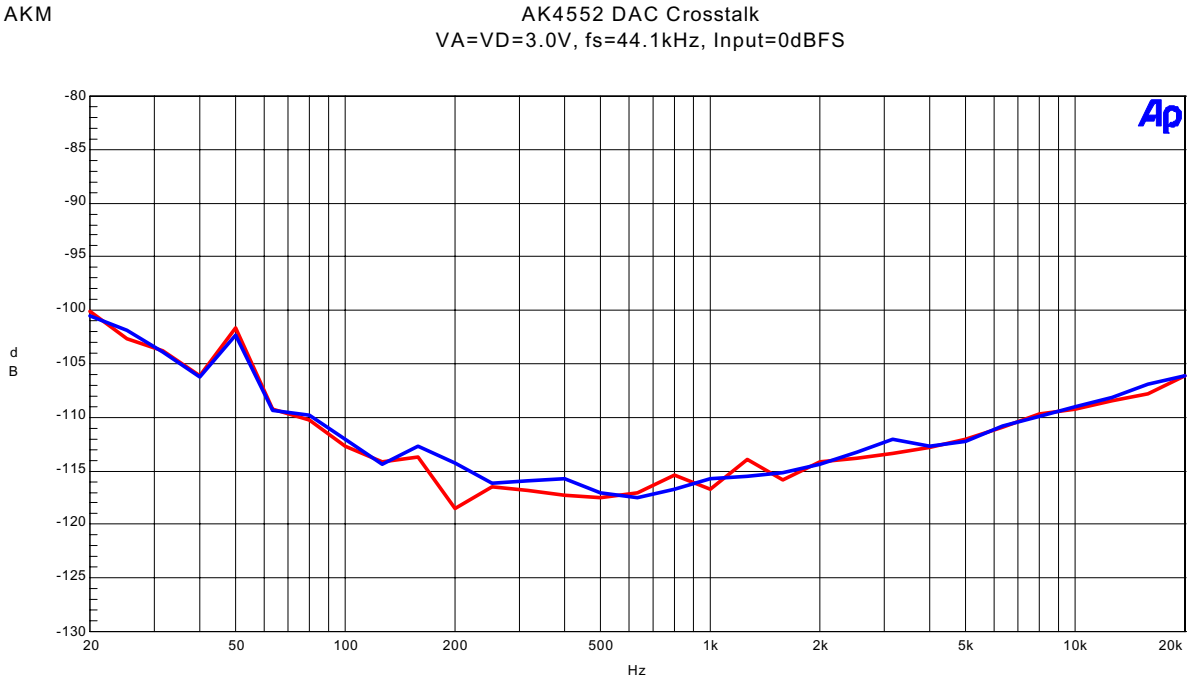


Figure 5. Crosstalk

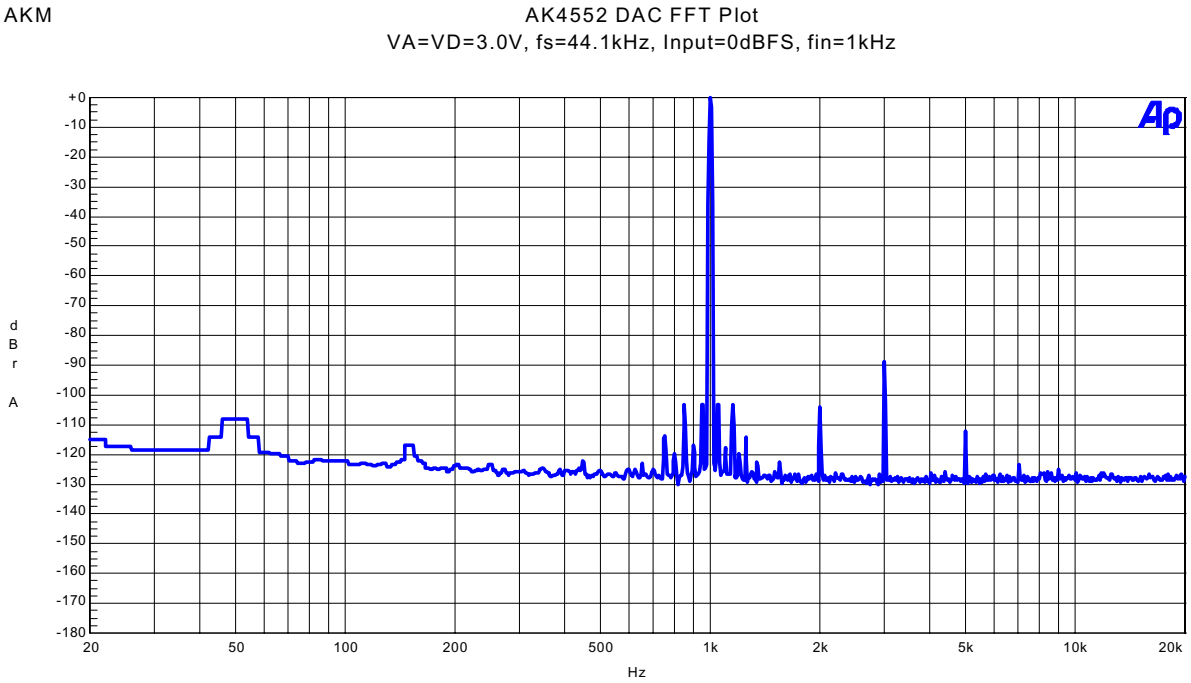


Figure 6. FFT Plot

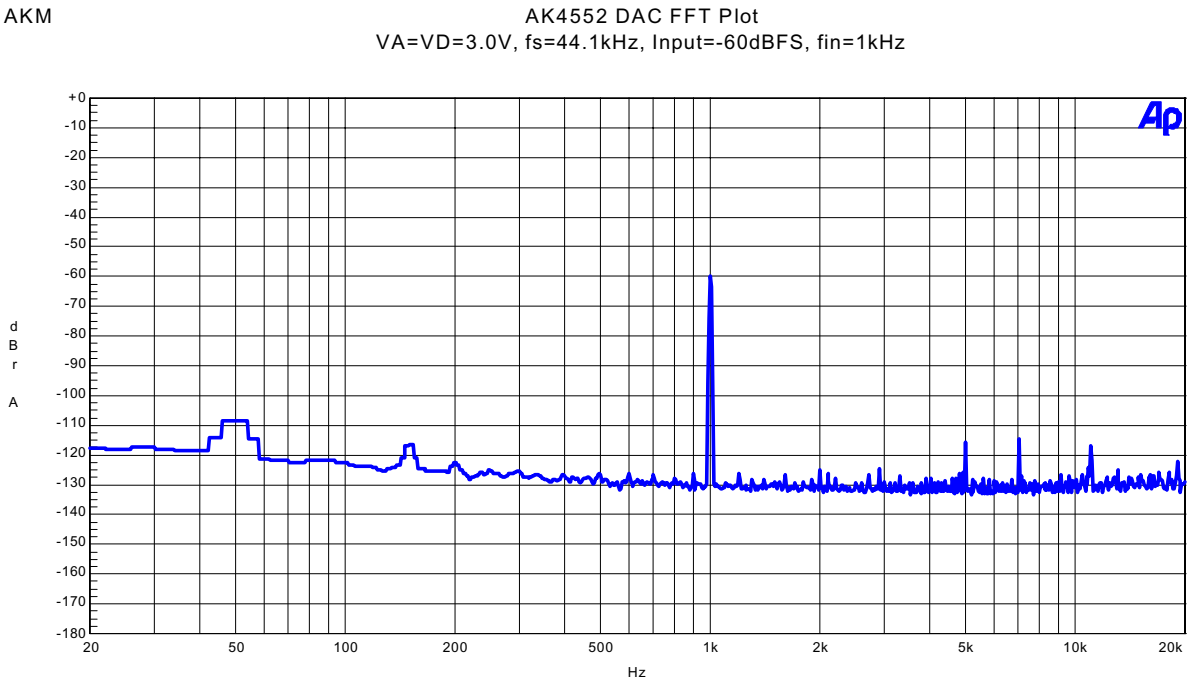


Figure 7. FFT Plot

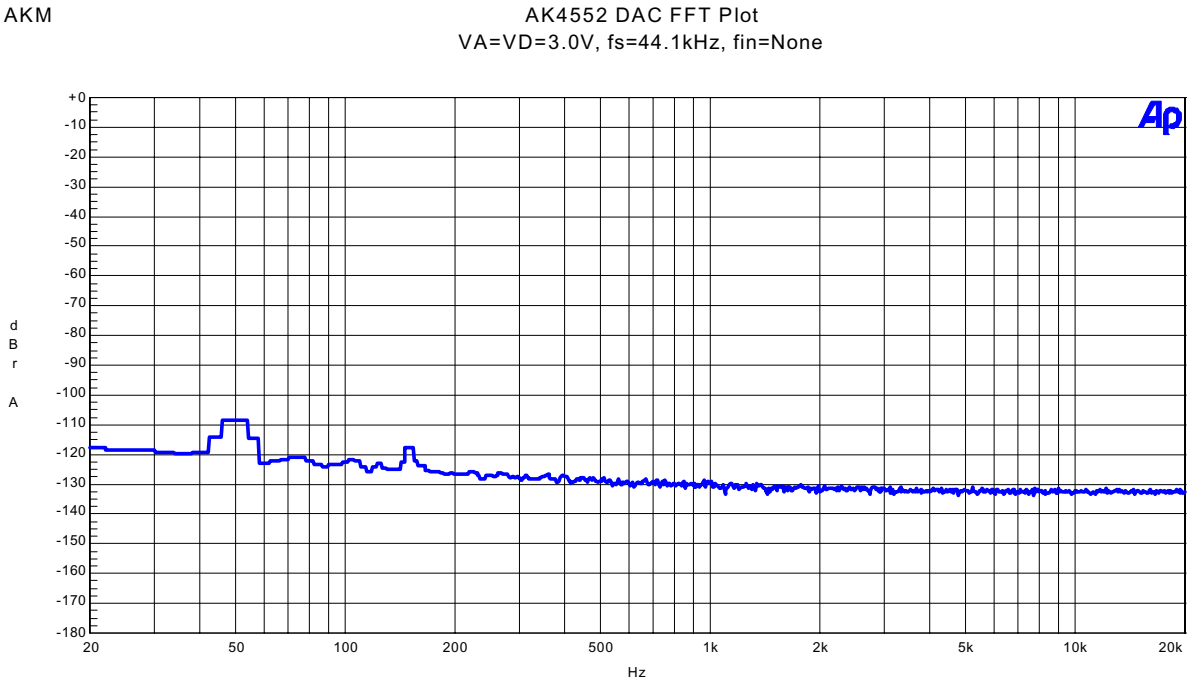


Figure 8. FFT Plot

3. ADC (Double Speed)

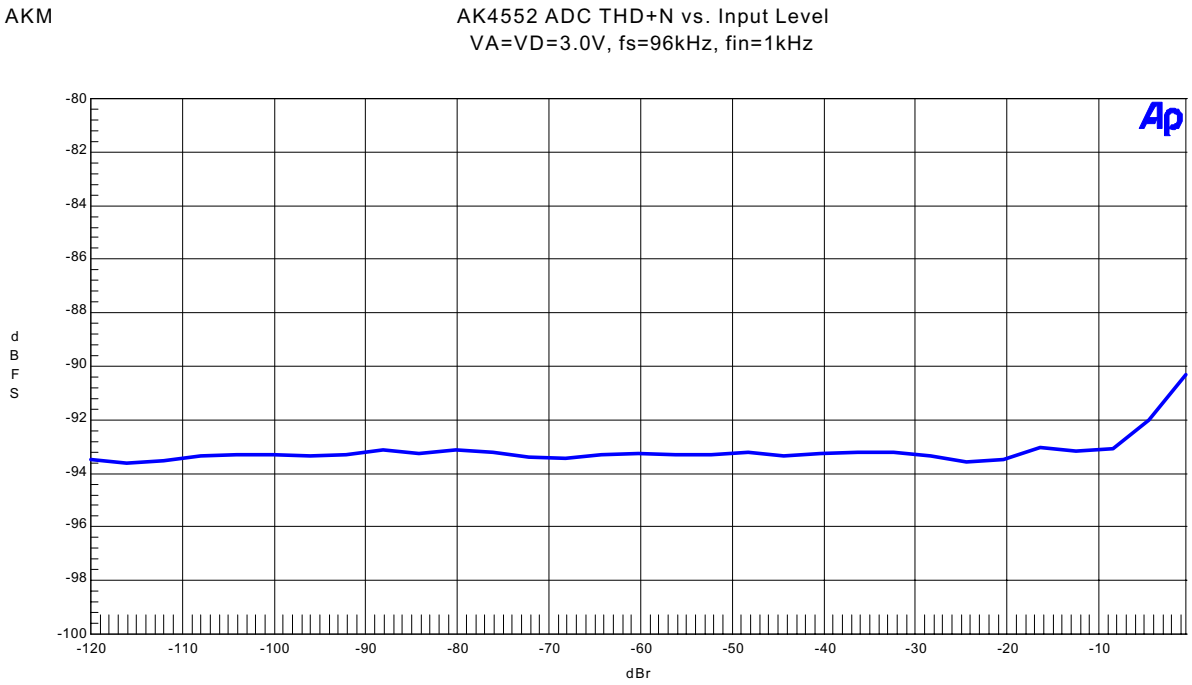


Figure 1. THD+N vs. Input Level

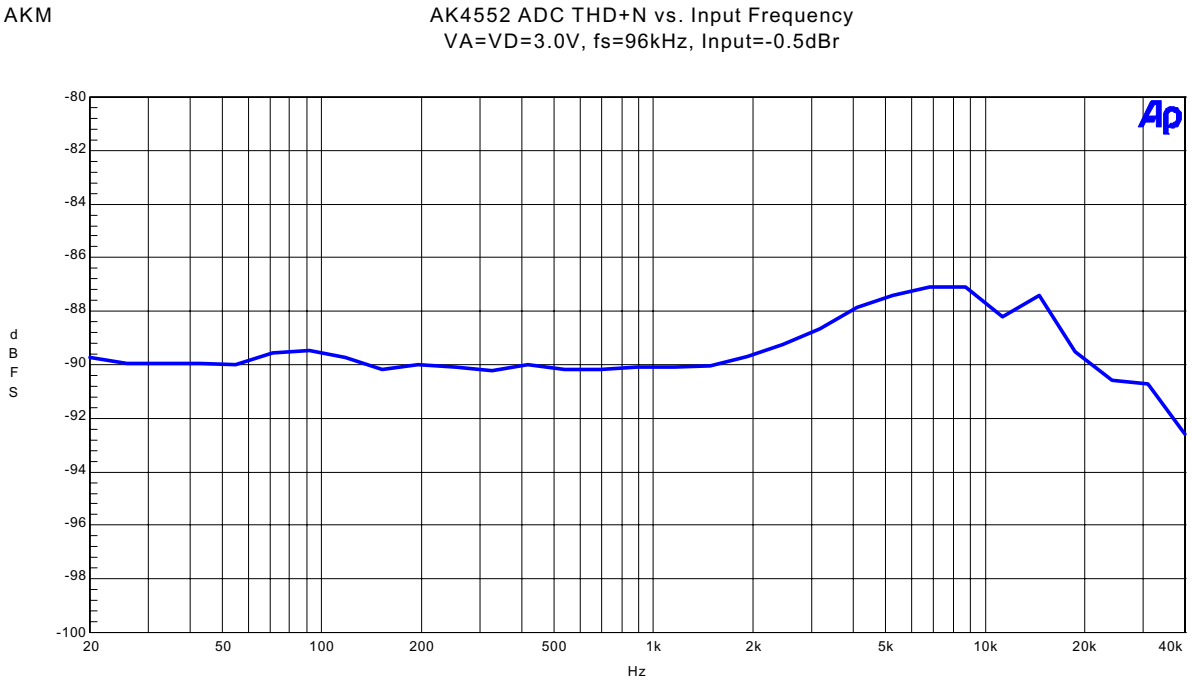


Figure 2. THD+N vs. Input Frequency

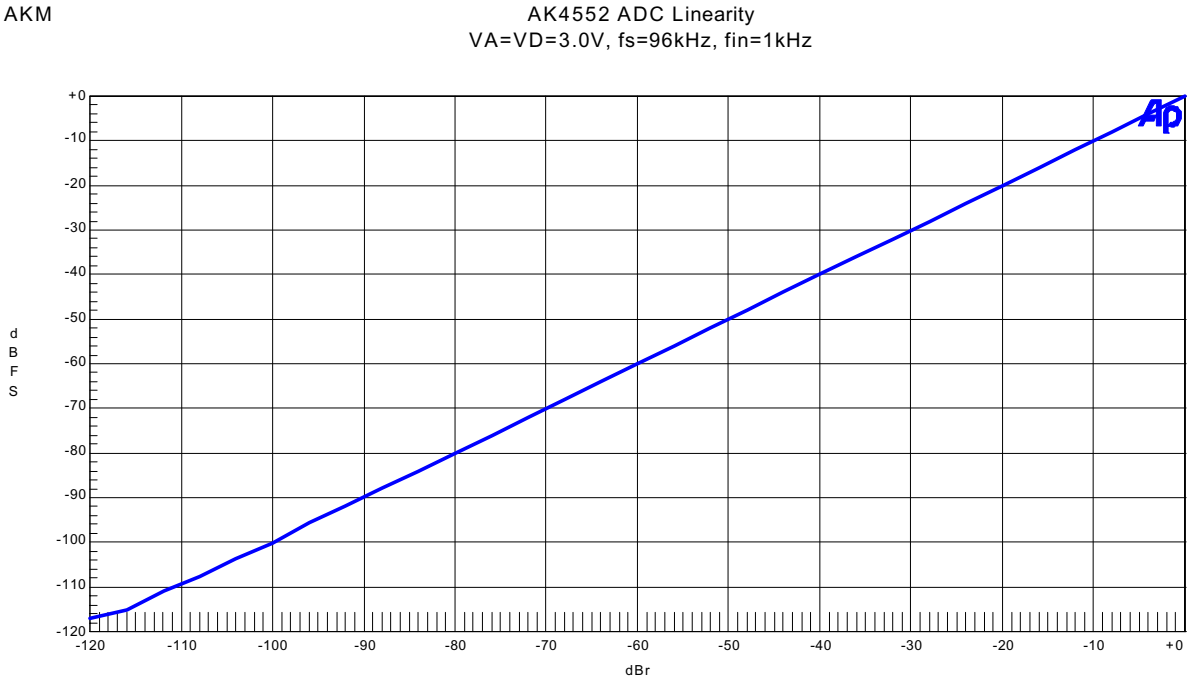


Figure 3. Linearity

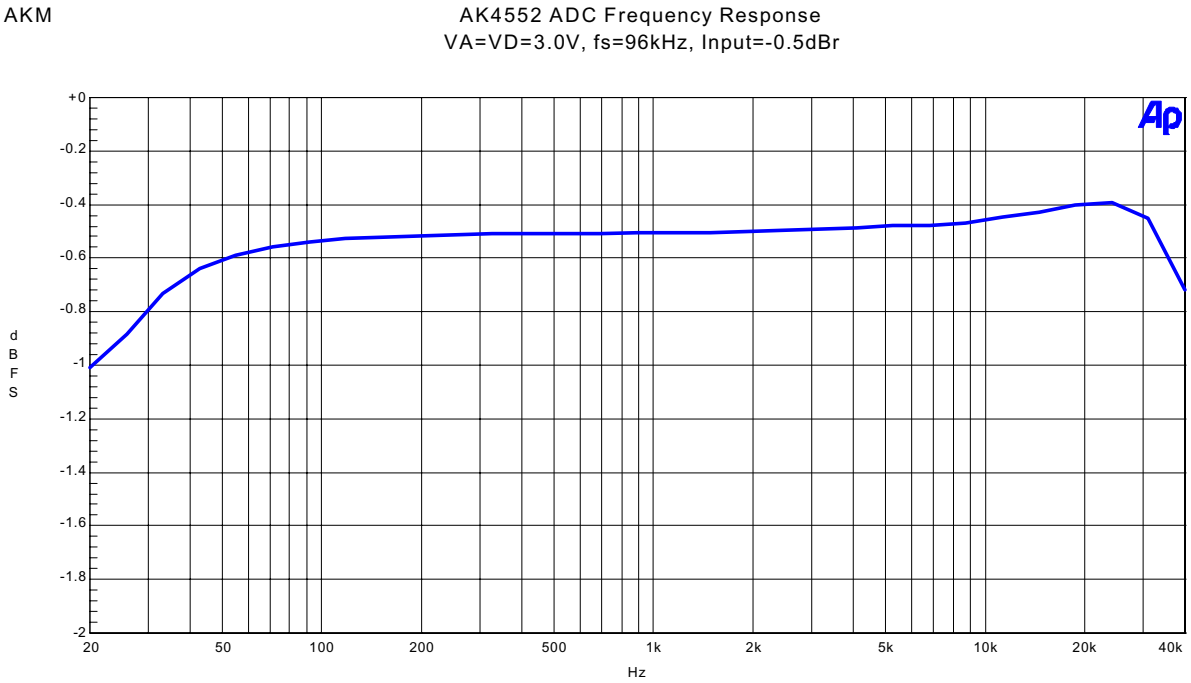


Figure 4. Frequency Response

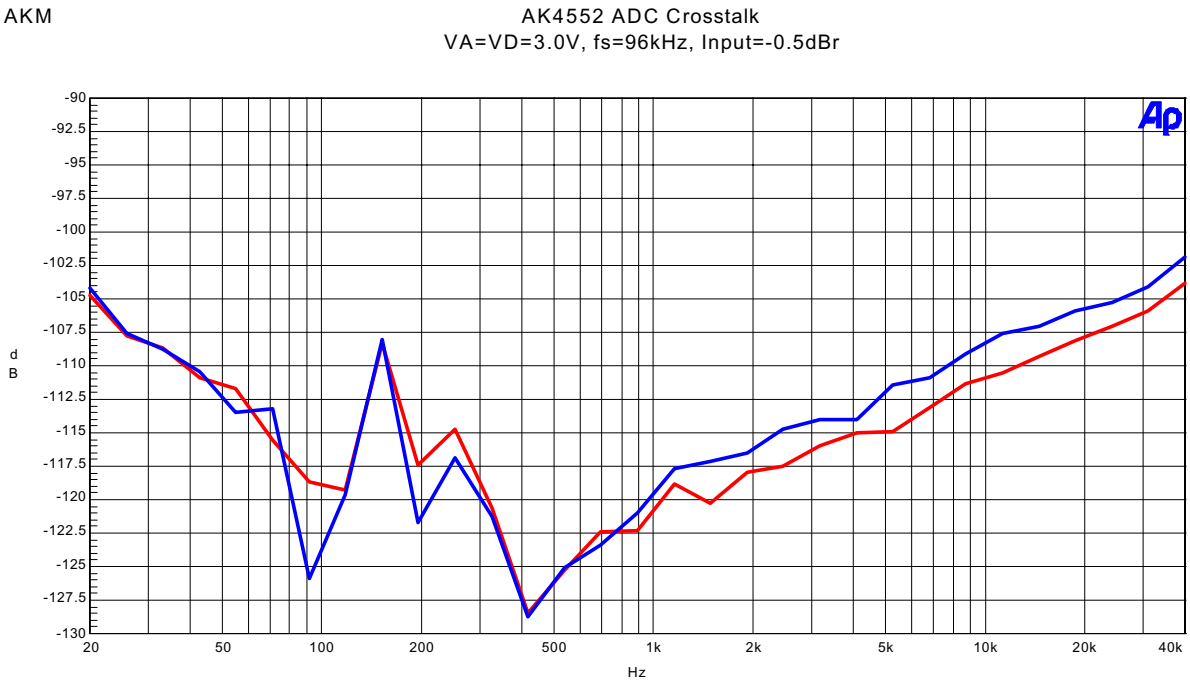


Figure 5. Crosstalk

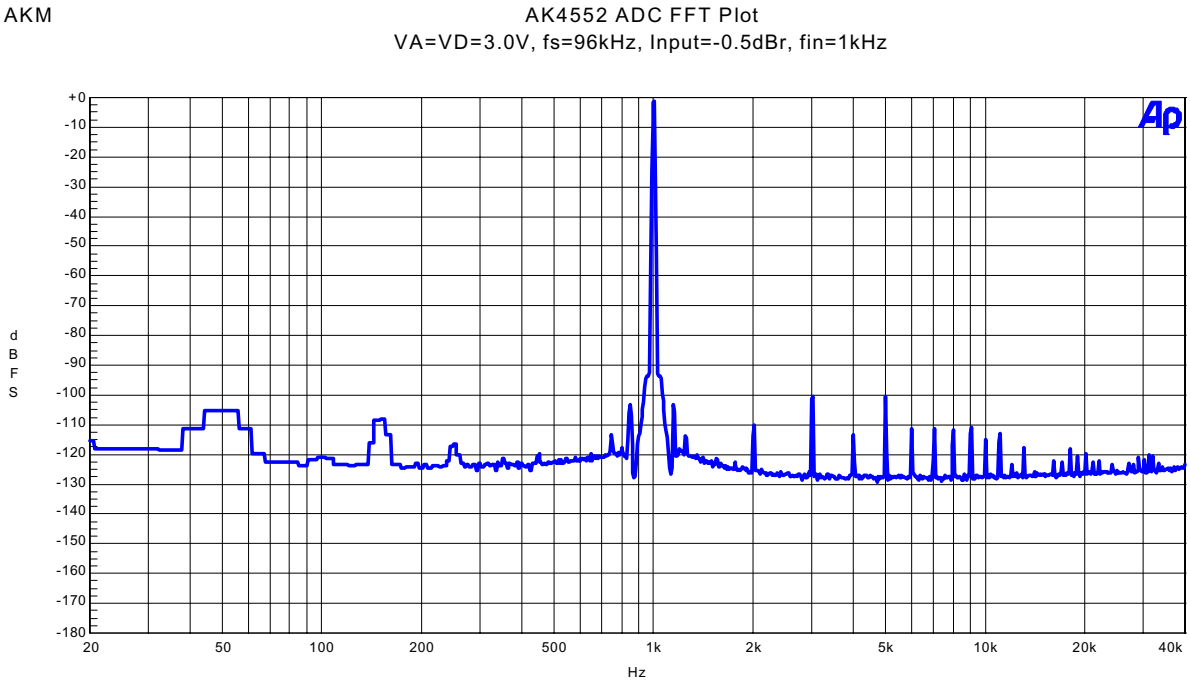


Figure 6. FFT Plot

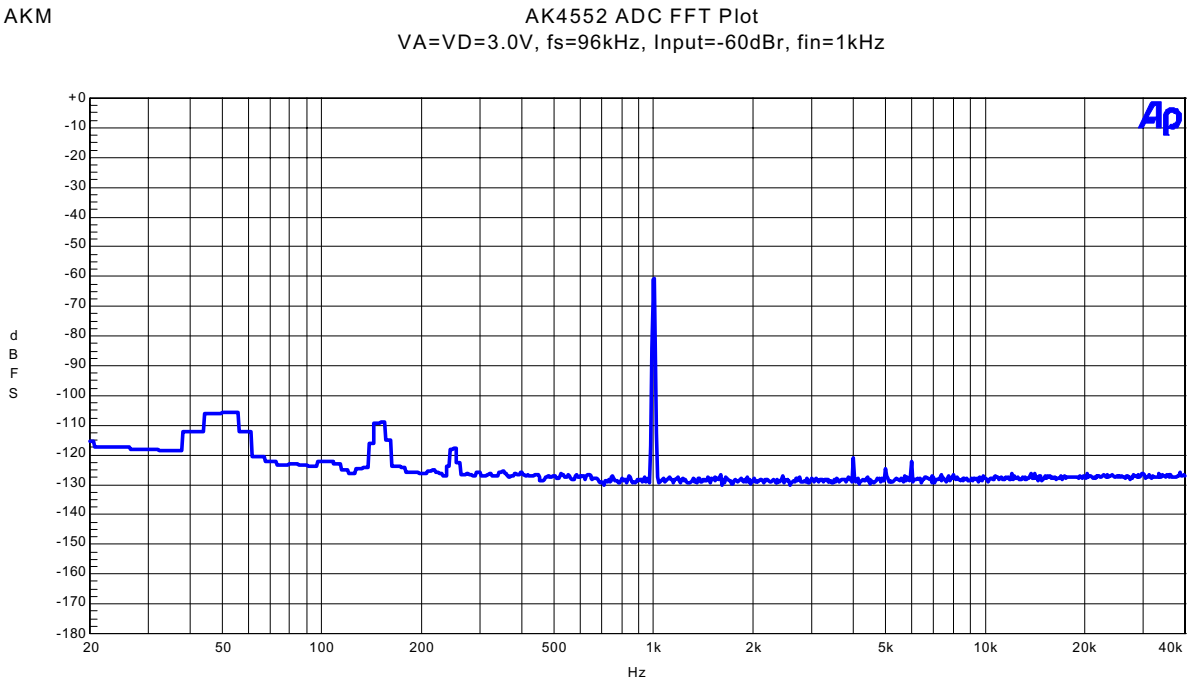


Figure 7. FFT Plot

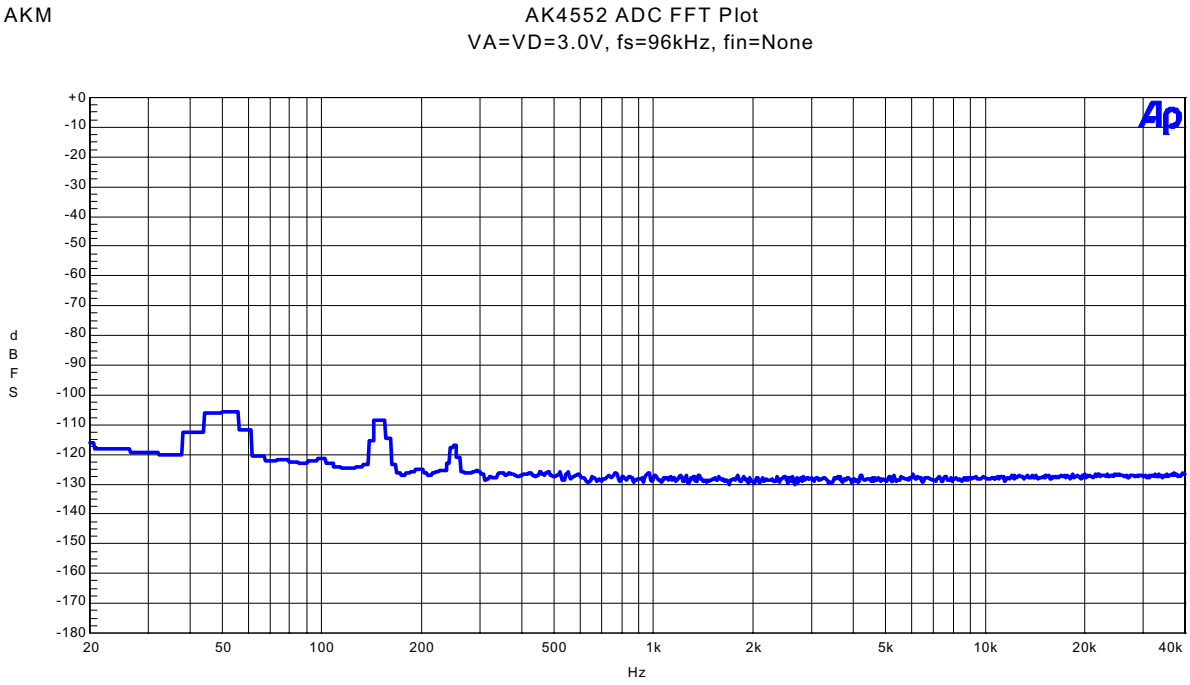


Figure 8. FFT Plot

4. DAC (Double Speed)

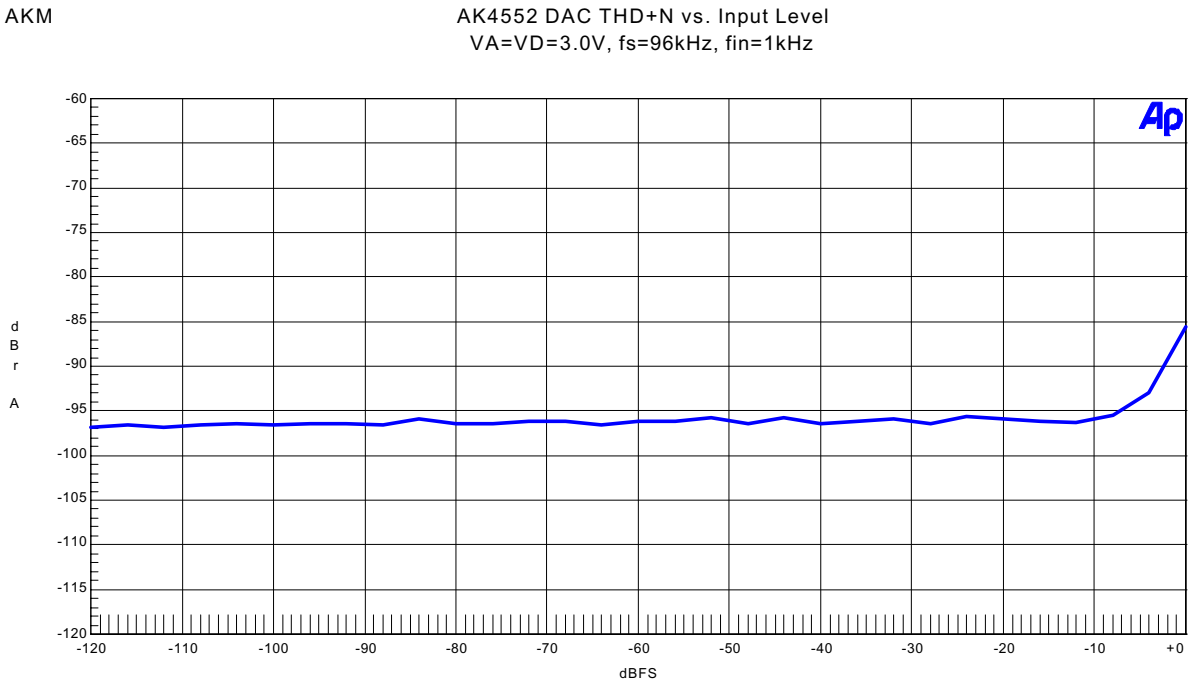


Figure 1. THD+N vs. Input Level

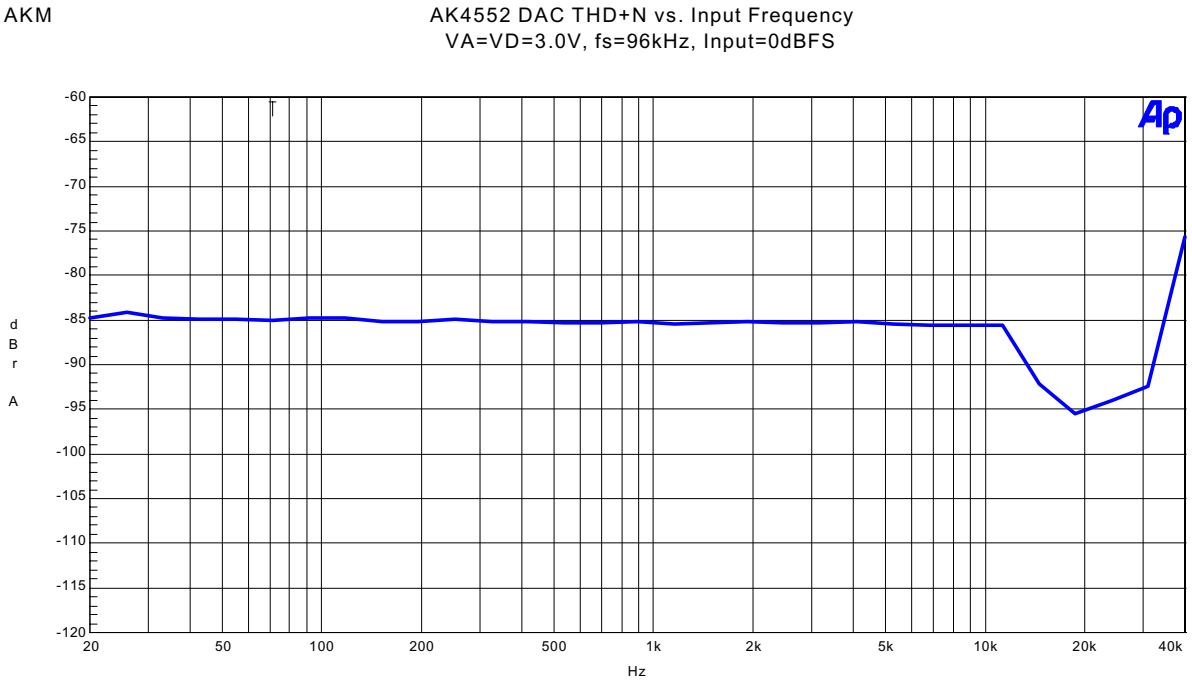


Figure 2. THD+N vs. Input Frequency

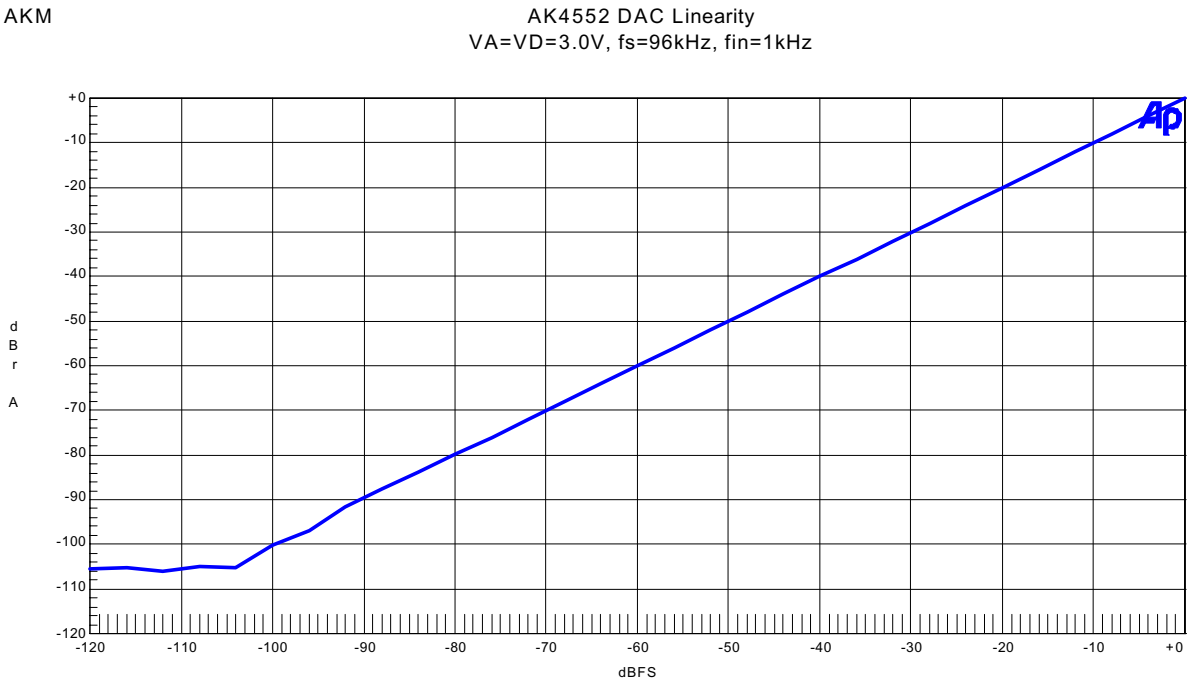


Figure 3. Linearity

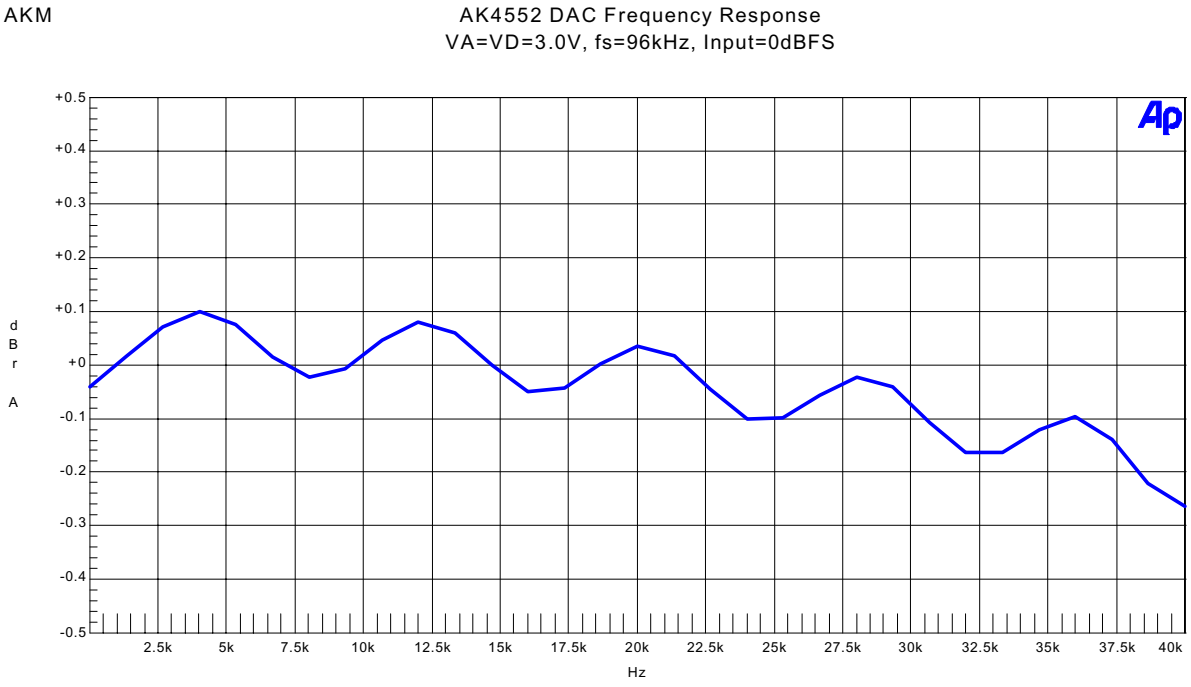


Figure 4. Frequency Response

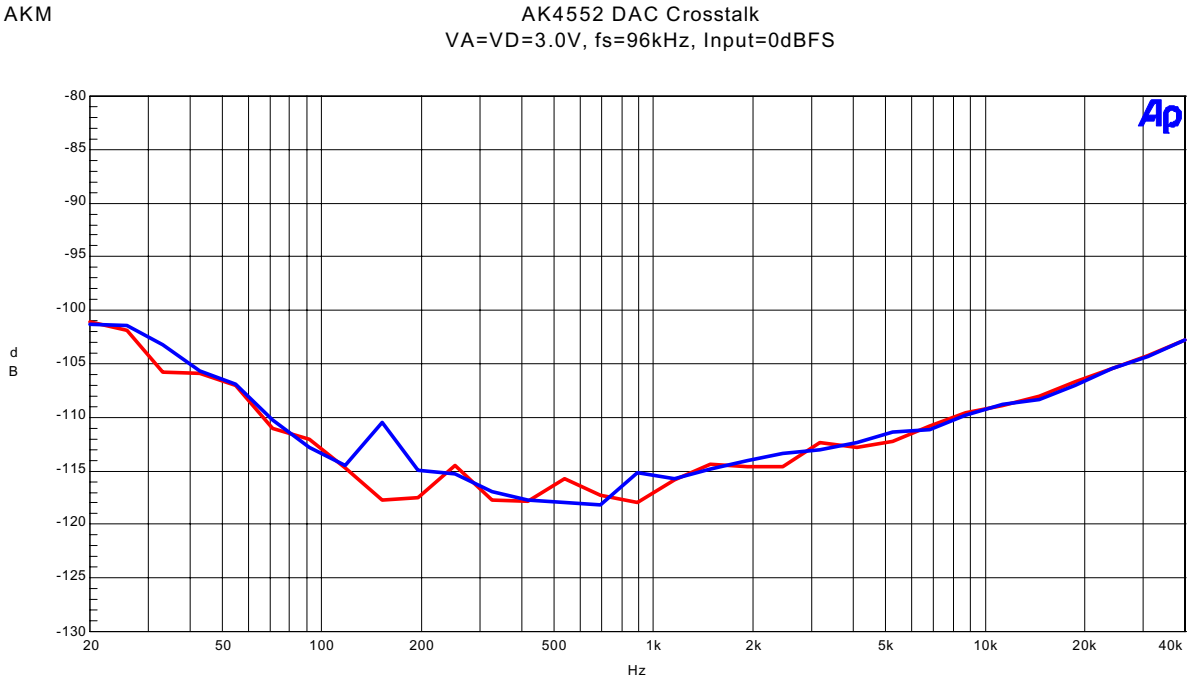


Figure 5. Crosstalk

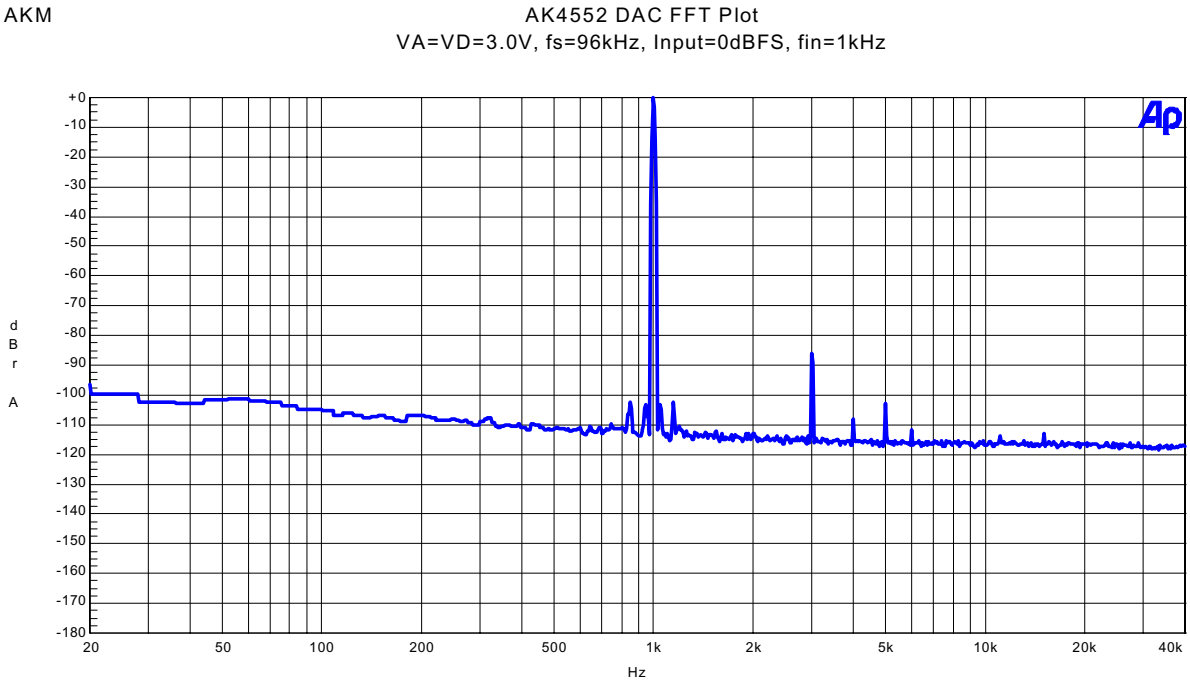


Figure 6. FFT Plot

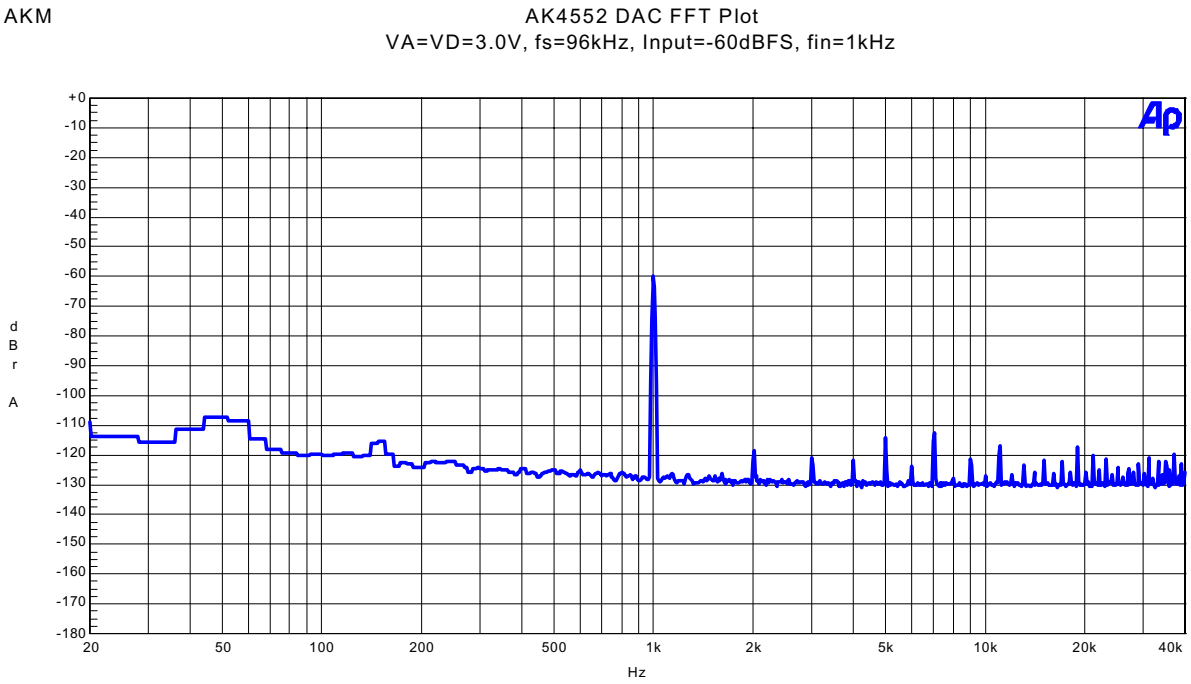


Figure 7. FFT Plot

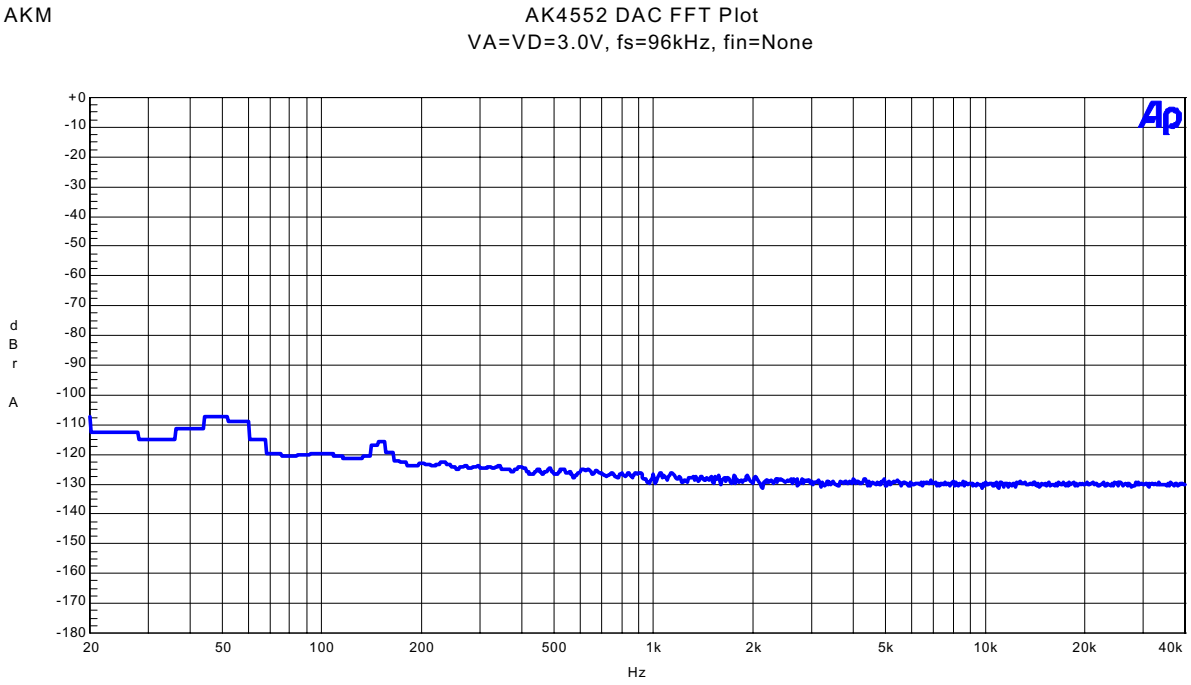
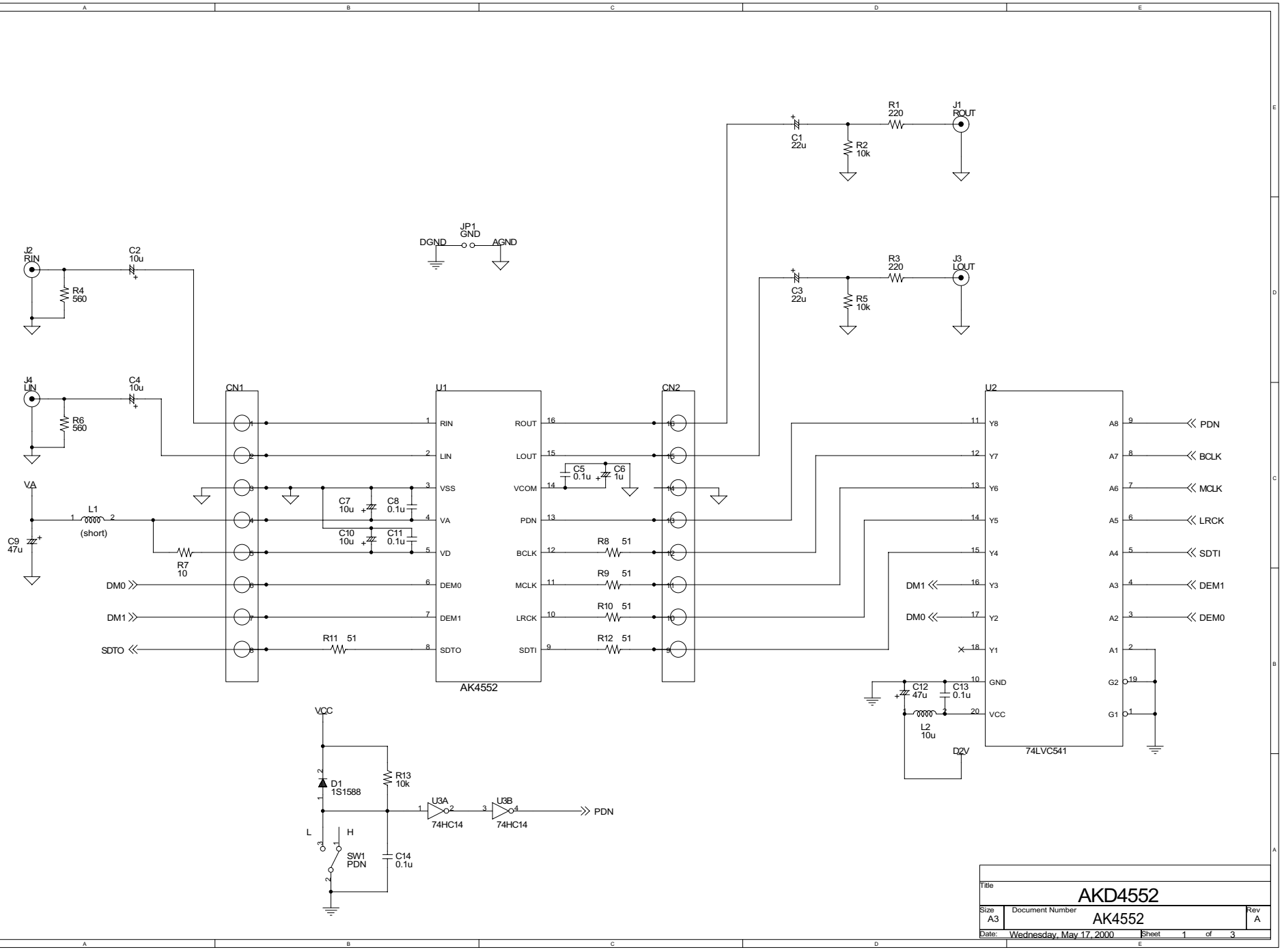


Figure 8. FFT Plot



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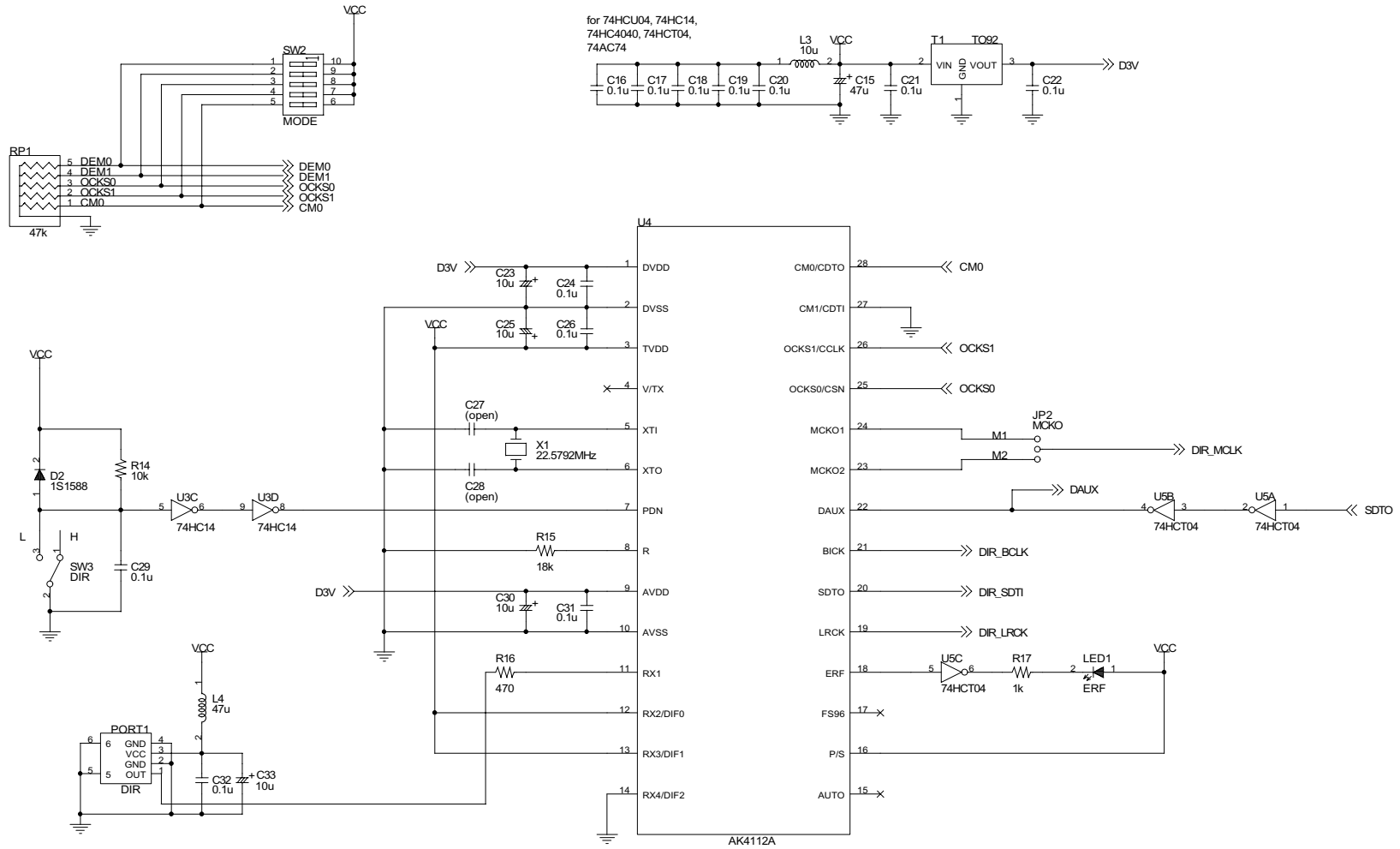

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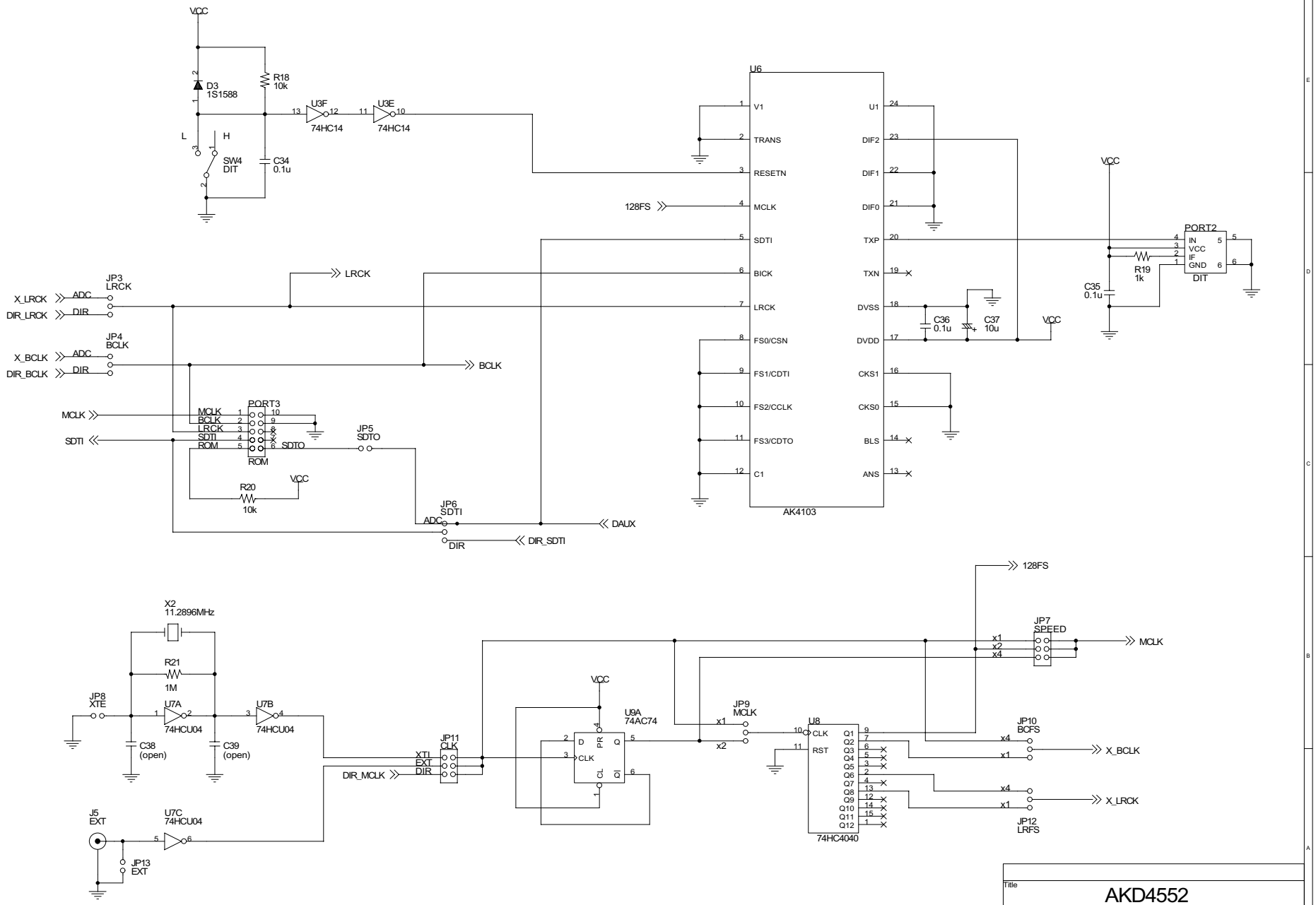

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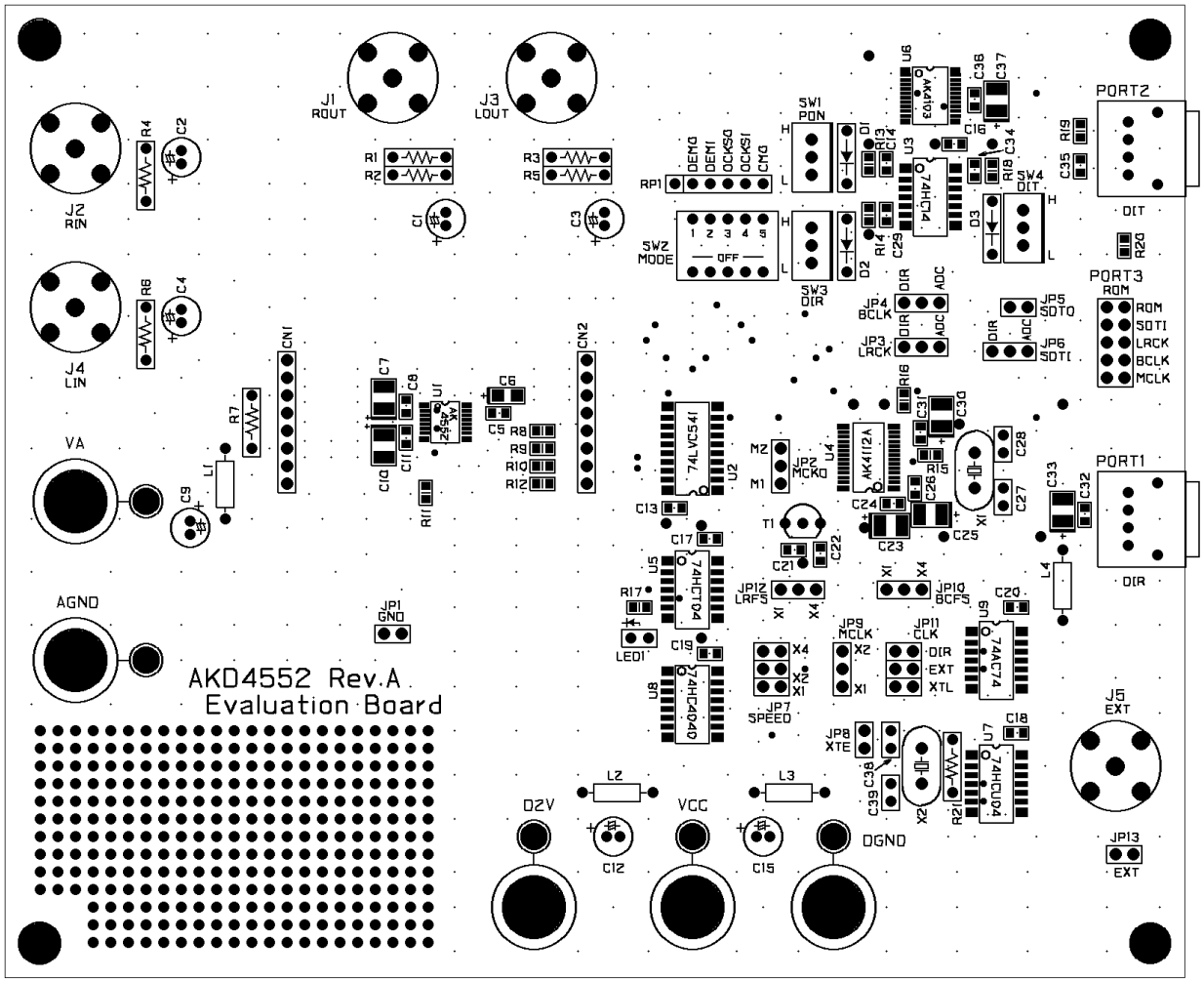
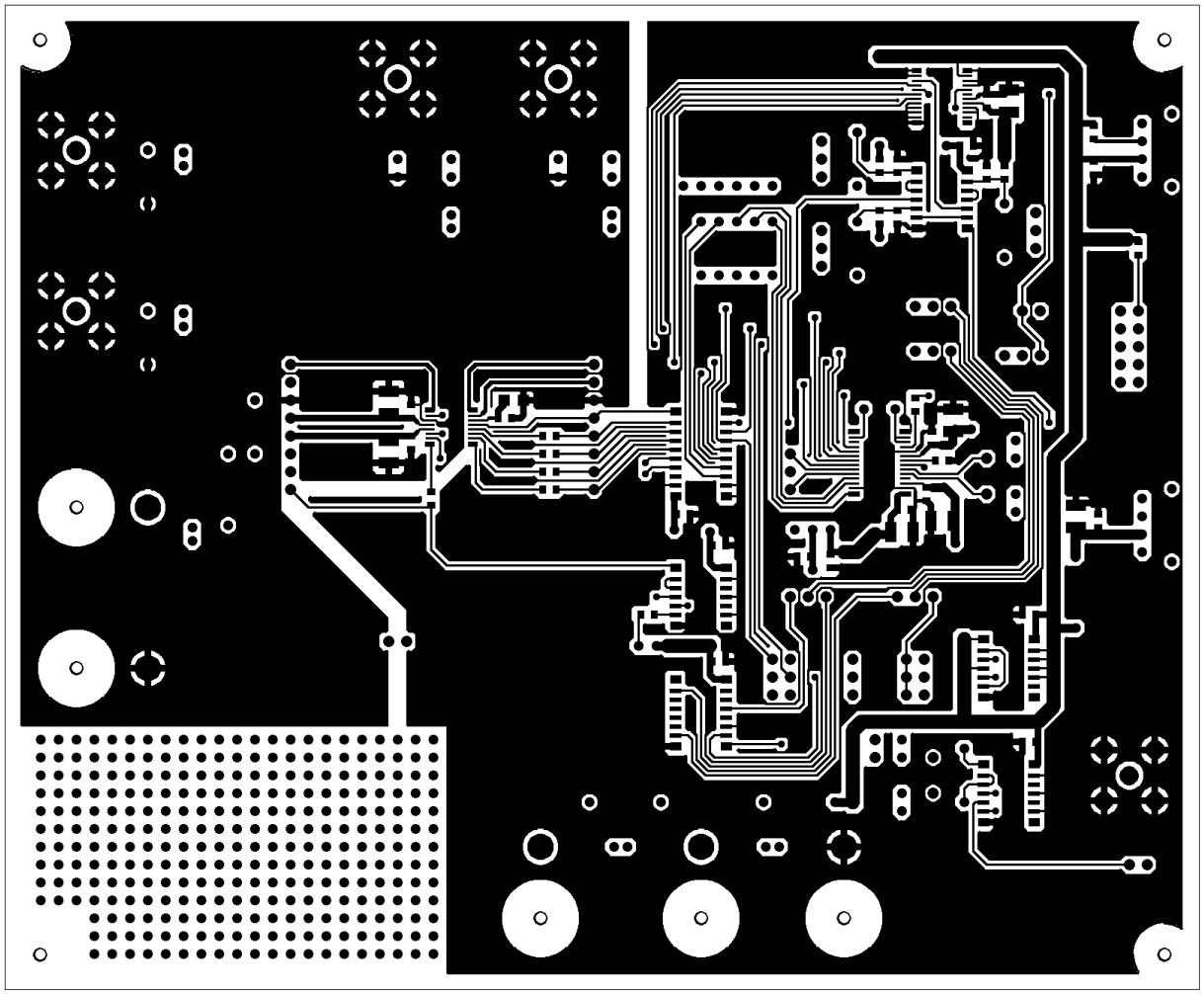


AKD4552 Rev.A L1 SR SILK



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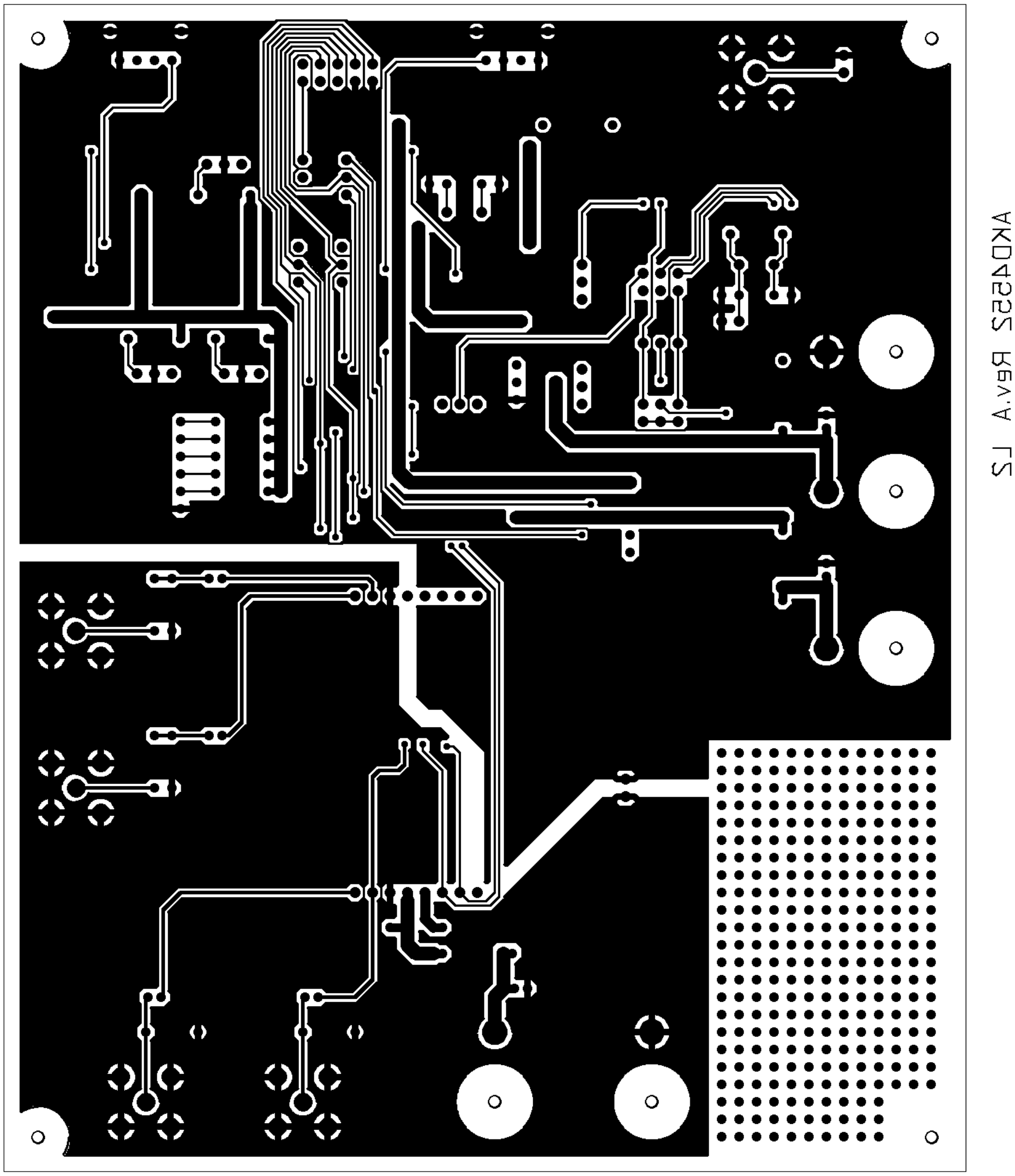
AKD4552 Rev.A L2

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