

Universal Telecommunication Hot Swap Family

System Power

ABSTRACT

This application note describes how to design a controlled current hot swap circuit with the Texas Instruments TPS2390 family of hot swap power managers.

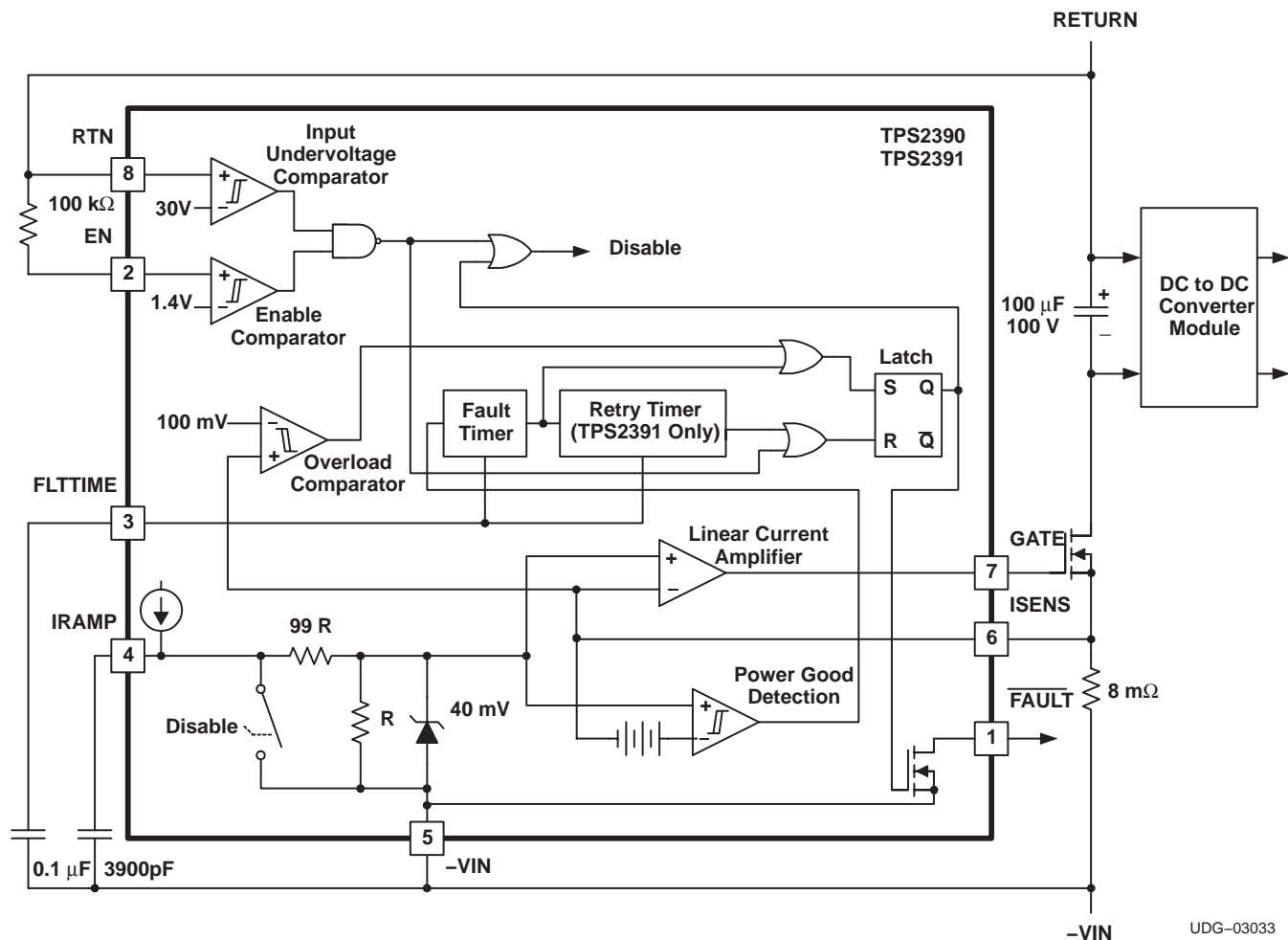
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1 A Typical Controlled-Current Hot Swap Implementation

Figure 1 is a schematic diagram of a typical controlled-current hot swap circuit built around the TPS2390/TPS2391 for up to 5 A in –48-V systems. Although the diagram is very simple, this implementation is complete and incorporates all components required to:

- Ride through 10-A current surges of up to 8 ms (programmable by C_{FLT}TIME)
- Disconnect if load current exceeds 5 A (programmable by R_{SENS}) for longer than 8 ms
- Disconnect if load current spikes above 12 A for more than 5 μ s, as in the case of a shorted load
- Control load current turn-on slew rate to 3.2 A/ms (programmable by C_{RAMP})

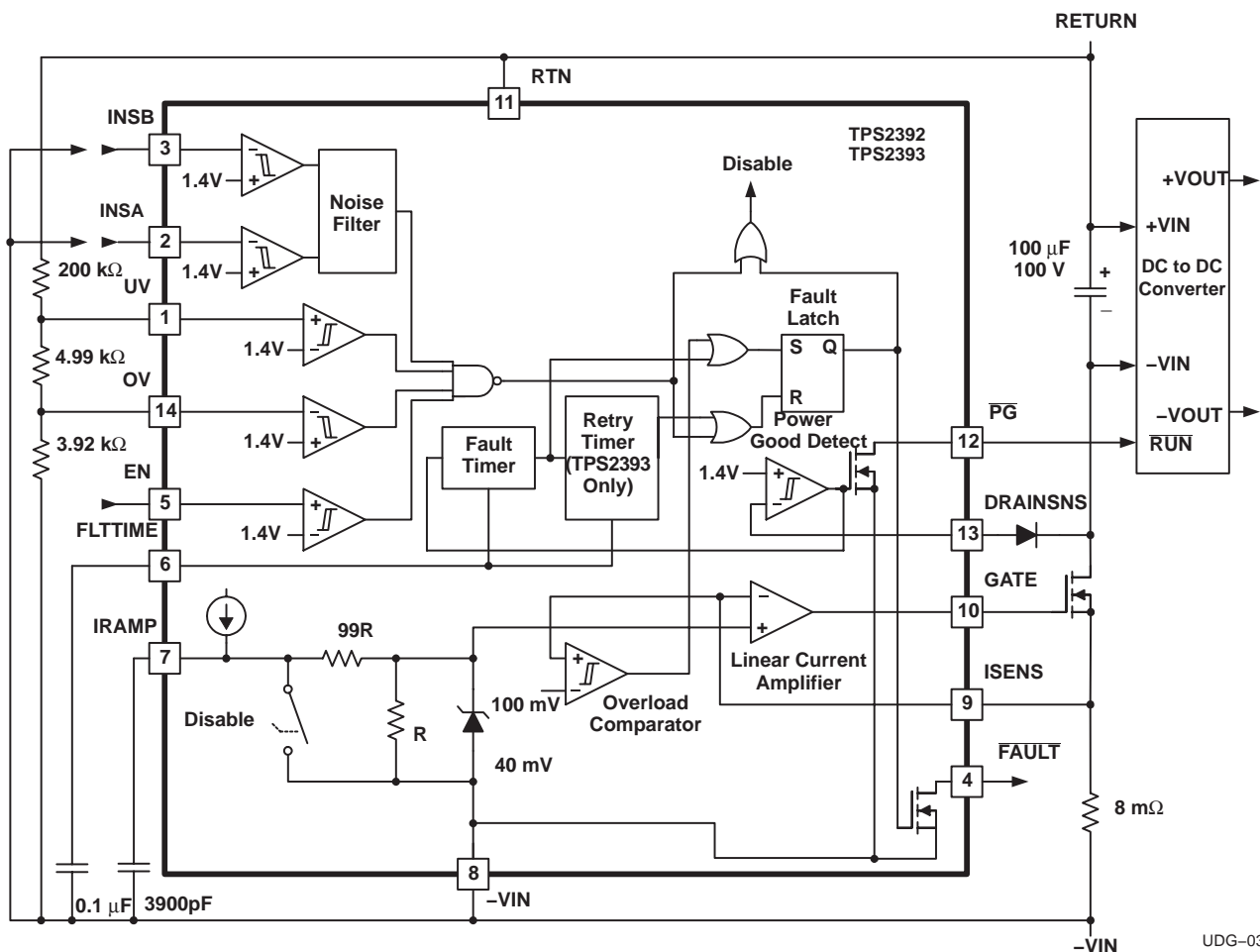


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Figure 1. TPS2390/TPS2391 Controlled-Current Hot Swap Circuit

Figure 2 is a schematic diagram of a similar hot swap circuit using the TPS2392/TPS2393. In addition to the previously described features, this circuit includes

- Programmable undervoltage and overvoltage thresholds
- Card insertion detection that prevents operation until the card is fully seated
- Logic output that indicates when the power FET is fully enhanced



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Figure 2. TPS2392/TPS2393 Controlled-Current Hot Swap Circuit

1.1 Selecting the Current-Sense Resistor

If a precise current limit threshold is desired, use a high-quality current sense resistor for R_{SENSE} . See Table 1 for possible alternatives. The PC board layout should use *force and sense* (also called *Kelvin connection*) techniques (see Figure 3) to prevent circuit board trace resistance from adding to the value of the resistor.

If the exact current-limit threshold is not critical, cost can be reduced by using a circuit board trace as the current-sense resistor. As with conventional resistors, use *force and sense* layout techniques with circuit board trace resistors to minimize uncertainty. In addition, to get the best possible tolerance from circuit-board trace resistors, mask any solder plating over the resistive trace. This helps because solder plating thickness is less controlled than copper thickness. Specify the copper thickness tolerance to the board manufacturing facility to insure process control and make the resistive trace as wide as practical. This minimizes the effects of etch tolerance on resistor value. It also gives the best thermal dissipation of the heat developed in the resistive trace. It is tempting to specify an internal copper plane for the current sense resistor because these often use higher resistance (thinner) copper, however, outside layers are preferred because they conduct heat better. To determine the minimum allowable width for the resistor and for the traces connecting to the resistor, consult standard IPC-D-275^[1] or Figure 4 for minimum trace width guidelines.

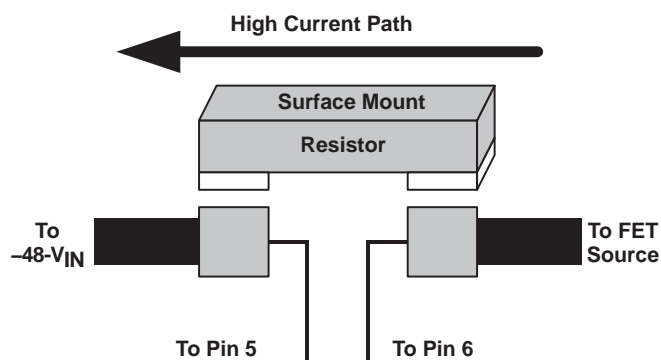


Figure 3. Current Sense Connections Using Force and Sense Technique

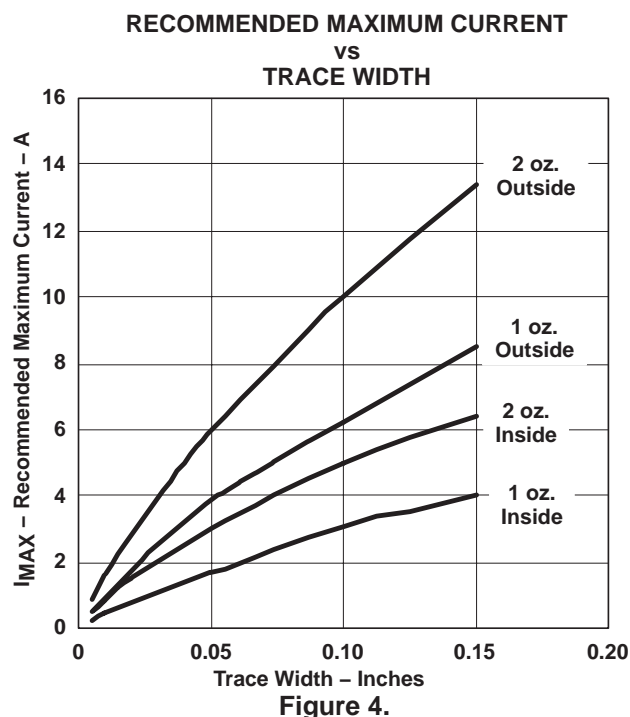


Table 1. Some Commercial Current Sense Resistors

MANUFACTURER	MODEL	RESISTANCE RANGE (mΩ)		TOLERANCE (%)	POWER RATING (W)	FEATURES
		Minimum	Maximum			
IRC	OARS	3	50	1 or 5	1, 2	Surface Mounting
	CSL	0.25	2.5	1 or 5	5	4-Wire
	CSS	0.5	2	5	1	2-Wire and 4-Wire
Caddock	SR10	8	1000	1	1	4-Wire
	SR20	8	1000	1	2	4-Wire
Dale	WSR2	1	1000	1	2	2-Wire
	WSK2512	1	25	1	1	4-Wire
	SPU114	1.67	20	1	1	4-Wire

Another approach to low-cost current sense resistors is to use a short length of low temperature-coefficient wire for the resistor. One choice for this is manganin wire, an alloy of copper, manganese, and nickel. In wire size AWG #18, manganin wire has 0.361 Ω/meter so 2.2 cm of AWG #18 manganin wire has a resistance of 8 mΩ. Manganin wire has a low-temperature coefficient, is low cost, solderable, and bendable. The presence of nickel in the alloy gives the manganin wire more series inductance than expected by the geometry, but when used with a current ramp, this slight extra inductance has very little effect.

1.2 Selecting the Capacitors

The current slew rate capacitor C_{RAMP} is optional. If omitted, load current is controlled, but the maximum load current slew rate is then limited only by the slew rate of the linear current amplifier (LCA). To control load current slew rate to a lower value, select C_{RAMP} in Farads by the following formula.

$$C_{IRAMP} = \frac{I_{IRAMP} (A) \times A_{CS}}{R_{SENSE} (\Omega) \times \frac{\delta I}{\delta t} (A/s)} = \frac{10^{-5} \times 0.01}{R_{SENSE} \times \frac{\delta I}{\delta t}} \quad (1)$$

where

- I_{IRAMP} is the charging current (10 μA)
- A_{CS} is the current sense gain (0.01)
- R_{SENSE} is the current sense resistor
- $\delta I / \delta t$ is the desired current slew rate

The fault capacitor programs the maximum on-time with a high current load, either during start-up or during overcurrent when operating. Select $C_{FLT\,TIM}$ in Farads as:

$$C_{FLT\,TIM} = \frac{I_{FLT\,TIM} \times t_{(max)}}{V_{CFLT\,TIM}} = \frac{5 \times 10^{-5} \times t_{(max)}}{4 \text{ V}} \quad (2)$$

where

- $t_{(max)}$ is the maximum desired time in seconds
- $I_{FLT\,TIM}$ is the charging current (50 μA)
- $V_{CFLT\,TIM}$ is the nominal voltage on $C_{FLT\,TIM}$ before the TPS2390 shuts down

When using the TPS2391, the load will automatically retry after a fault and a delay. This off-time delay between shut down and retry is fixed at $t_{(max)} \times 100$, giving a typical on duty cycle of 1%. This can be helpful if soft faults are possible and should not lead to any problems, as retry cycles are always run with controlled current.

1.3 Selecting the Power FET

In any power switching application with soft start, there are a few different operating modes for determining power dissipation in the power FET: turning on into a normal load; turning on into a faulty load; and normal operation. Most often, the worst-case considerations involve turn-on into a faulty load, but all modes should be considered.

The simplest to consider is normal operation because this is a steady state calculation. In this case, the power FET is fully enhanced and power dissipation is calculated as the data sheet worst case on resistance multiplied by the load current squared:

$$P_{Diss\,FET} = \left(I_{LOAD(max)} \right)^2 \times R_{DS(on)(max)} \quad (3)$$

This represents steady-state power dissipation. To be sure that the system is safe operating with this much power dissipation, calculate the thermal resistance of the power FET and heat sink to ambient, multiply that by the worst-case power dissipation (see equation (3)), add that to worst case ambient temperature:

$$T_J = T_A + P_{Diss(max)} \times \theta_{JA} \quad (4)$$

Compare the result to the maximum junction temperature on the power FET data sheet to determine if the selected power FET and heatsink are adequate.

Turn-on into a normal load is a bit more complex, because it involves a one-time event where power dissipation is much higher than normal operating power dissipation. In this case, split the time into an interval when current is ramping and another interval when current is limited. You can normally ignore the current ramp interval because this is a short time and current is not very high. Calculate the actual turn-on time by the time that it takes to charge C_{LOAD} up to V_{IN} at I_{MAX} .

$$\text{where } I_{MAX} = \frac{0.04 \text{ V}}{R_{SENSE}} \quad (5)$$

$$t_{\text{CHG}} = \frac{C_{\text{LOAD}} \times V_{\text{IN}}}{I_{\text{MAX}}} \quad (6)$$

Then calculate the average power dissipation during that interval as half of the peak power dissipation:

$$P_{\text{Diss(avg)}} = \frac{I_{\text{MAX}} \times V_{\text{IN}}}{2} \quad (7)$$

because of the linear voltage ramp that occurs at a constant current into a capacitive load. The product of the average power and the charge time is the energy that is instantly forced into the thermal mass of the power FET and the heat sink. Refer to the safe operating area curve on the data sheet for the power FET to confirm that the device is capable of dissipating that energy.

Turn-on into a worst-case faulty load (short circuit) is similar to turn-on into a normal load, but the charge time is the time for the fault timer to time out and the average dissipation is twice as high as in the normal case because the full supply remains across the FET. Again, confirm that the power FET and heat sink are rated to accept one-shot (in the case of the TPS2390) or repetitive (in the case of the TPS2391) energy surges of $\text{Energy} = I_{\text{MAX}} \times V_{\text{IN}} \times T_{\text{FAULT}}$.

Power FET safe operating area (SOA) calculations should take into account the thermal time constant of the power FET itself, the thermal time constant of the power FET package, and the thermal time constant of the heatsink assembly. Using a power FET model that includes these separate coefficients, designers can balance heatsink size, fault time, maximum current, and power FET selection so that the system can survive a worst-case faulty load.

The SOA curve on the power FET data sheet (see Figure 5 for an example) represents the ability of the power FET to absorb one-time, short-duration, high-energy pulses. In the case of these short-duration pulses, the heat sink is of no benefit because the thermal mass of the heat sink or board radiating area combined with the thermal resistance from the junction to the heat sink has a time constant significantly longer than energy surge. So if the power pulse (fault time) is shorter than 10 ms, for example, then the power FET itself must absorb the energy. For longer or repetitive surges, a heat sink is beneficial.

A typical system might have a load capacitance of 200 μF , a supply voltage as high as -80 V , and running load current as high as 5 A. For this system, select the maximum current to be higher than the operating current by enough margin for component tolerances. In this case, use 8 A. Calculate R_{SENSE} .

$$R_{\text{SENSE}} = \frac{0.04\text{ V}}{8\text{ A}} = 0.005\Omega \quad (8)$$

Calculate the time to charge the 200- μF load capacitance to -80 V at 8 A.

$$t_{\text{CHG}} = \frac{80\text{ V} \times 0.0002\text{ F}}{8\text{ A}} = 2\text{ ms} \quad (9)$$

This suggests the fault timer should be set enough above 2 ms to allow for component tolerances. In this case, select 4 ms.

Given these parameters, the next task is to select the appropriate power FET. Breakdown voltage must be greater than 80 V and operating current must be greater than 8 A. In addition, voltage drop should be small enough that the power dissipated in the FET during operation is insignificant and the voltage drop doesn't significantly interfere with system operating margin at low input supply. A good choice might be a power FET rated at 100 V with $R_{DS(on)} < 0.044 \Omega$ in a D² package. Most often, a power FET like this is rated for much higher than an 8-A operating current, so operating current rarely limits choices. Figure 5 shows the safe operating area curve for a typical power FET with these ratings. The curves in Figure 5 show that this device can handle pulses up to 100 A at high voltage, but only for short times. By interpolating between the 1 ms and 10 ms curves, we estimate that for 80 V pulses of 4 ms, this power FET is only good for approximately 3.5 A, which is inadequate for this application. A larger power FET is required.

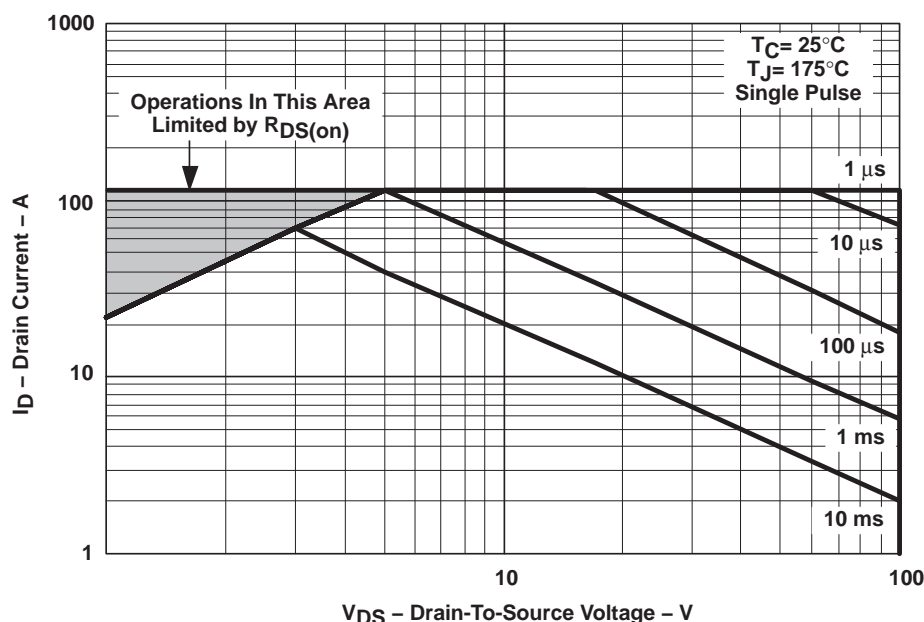


Figure 5. Typical Power FET Safe Operating Area Curves

2 Using the TPS2390 and TPS2391

The TPS2390 has a logic input called EN to turn on the power switch, making this part more than just a hot swap power manager. The TPS2390 can also be used as a protected *smart* power switch. When used this way, the TPS2390 provides logic controlled soft turn-on, current limit, circuit breaker protection, and indication of a fault.

The TPS2390 has internal undervoltage protection factory set to approximately 30 V. However, the EN input can also be used as a precision, adjustable UV protection input, supplementing the internal UV comparator (see Figure 6).

EN can also be used as an overvoltage protection input with a few additional components (see Figure 7).

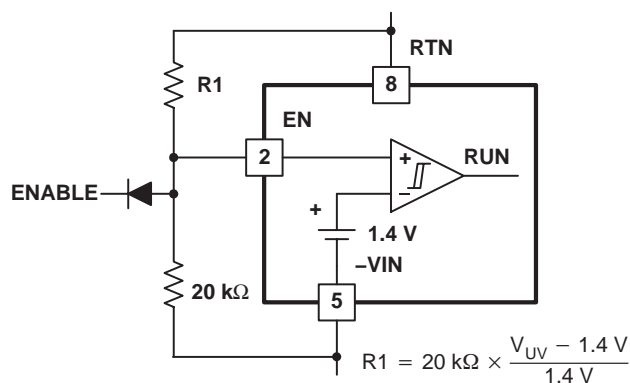


Figure 6. Raising the TPS2390 Undervoltage Threshold

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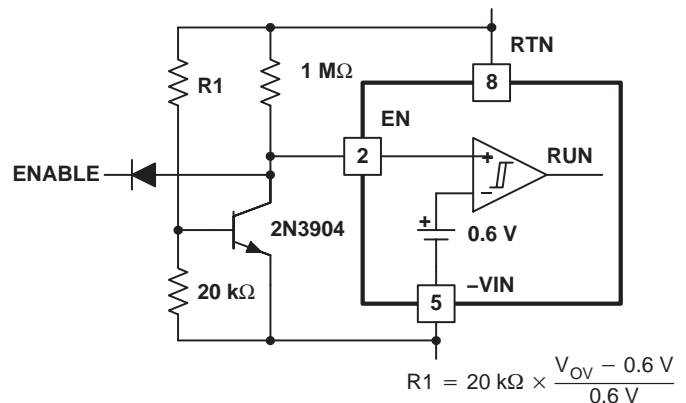


Figure 7. TPS2390 Overvoltage Shutdown

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The EN input can also be used for delayed turn-on as the TPS2390 does not start until EN rises to 1.4 V (see Figure 8).

In some cases, it is valuable to switch on two or more supplies in sequence. The TPS2390 can be cascaded for sequencing using the EN input. When the output of one supply is above a user-programmed threshold, this can produce a signal to turn on a second TPS2390. The signal might come from the downstream dc-to-dc converter, or simply from the first TPS2390 output.

Another feature of the TPS2390 is controlled current ramping. Placing a capacitor on C_{RAMP} requires that the current into the load smoothly ramp from zero to a programmed maximum. The maximum is internally fixed at 40 mV divided by R_{SENSE} , and the ramp reaches maximum when C_{RAMP} reaches 100 times that, or 4 V. If the voltage on C_{RAMP} is greater than 4 V, internal circuitry still limits load current to 40mV divided by R_{SENSE} .

Maximum current can also be set to a lower current by commanding the voltage on C_{RAMP} below 4 V (see Figure 9).

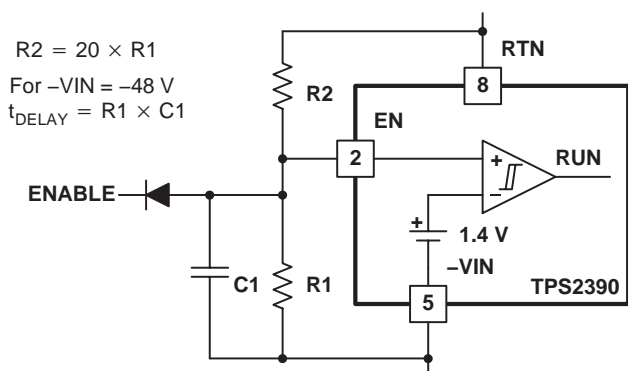


Figure 8. Delaying the TPS2390 Turn-On

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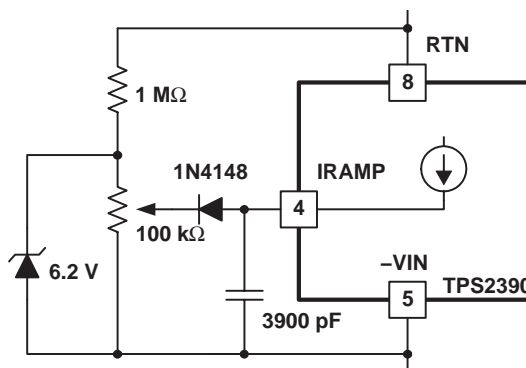
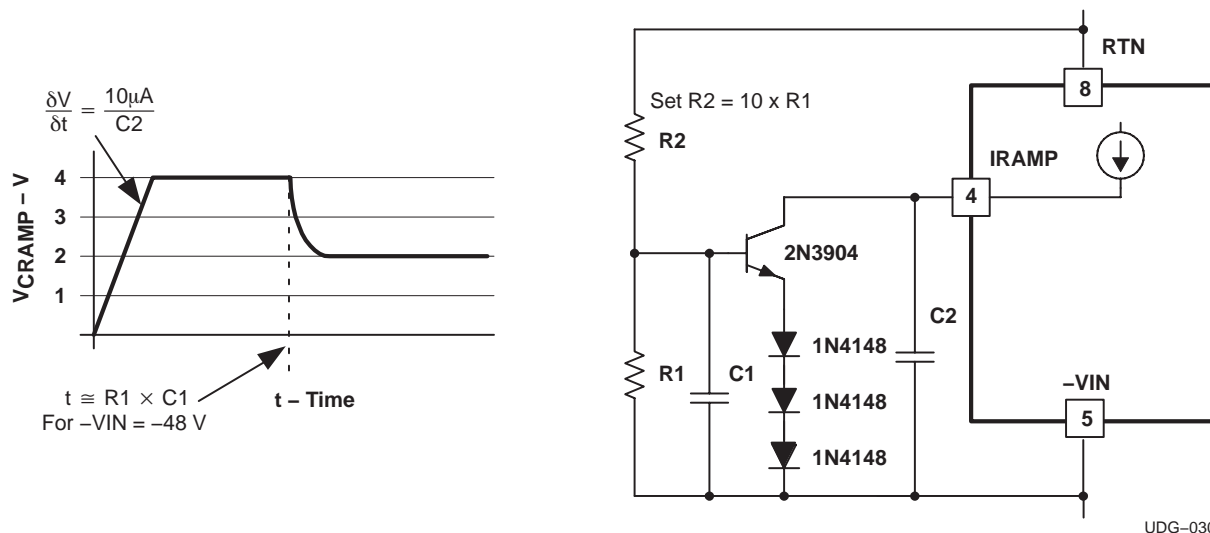


Figure 9. Lowering the Current Limit Threshold

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In some cases, a profile different from fixed current slew rate may be desired. For example, if a design requires a large maximum current during starting and a smaller maximum during operation consider using a switched clamp on C_{RAMP} . (See Figure 10)



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Figure 10. Programming the TPS2390 For High Inrush and Lower Operating Current

Another feature of the TPS2390 is the $\overline{\text{FAULT}}$ output. This high-voltage, open-drain output can be used to drive an LED, to drive an opto-isolator, or can be directly connected to logic.

All of the previously discussed uses for the TPS2390 apply to the TPS2391 as well. The only difference between these two devices is that the TPS2390 latches off in a fault while the TPS2391 shuts down and then retries in the event of a fault.

2.1 Even more capability with the TPS2392 and TPS2393

Both the TPS2390 and TPS2391 are housed in a tiny, 8-pin MSOP (DGK) package. The TPS2392 and TPS2393 offer all of the features of the tiny TPS2390 and TPS2391 plus a few others and are packaged in the slightly larger 14-lead TSSOP (PW) package.

Additional features of the TPS2392 and TPS2393:

- Separate undervoltage and overvoltage comparator inputs
- Debounced board insertion inputs
- Power good logic output

If programmable undervoltage protection is not required, the UVLO input can also be used as a second active-high logic enable input with a precise threshold. If overvoltage protection is not required, the OVLO input can be used as an active-low logic enable input with a precise threshold.

The INS inputs are also precision, active-low enable inputs, but also feature 2.5-ms filtering to prevent turn-on jitter with noisy connections or signals. These inputs can be connected to short pins on the ends of the card edge connector to prevent starting until the board is fully seated.

The power-good-low ($\overline{\text{PG}}$) output of the TPS2392 is a high-voltage open-drain output that remains high impedance until the IRAMP capacitor (C_{RAMP}) charges and the drain of the external power FET is close to $-\text{VIN}$. At that time, the $\overline{\text{PG}}$ output pulls to $-\text{VIN}$. This output can be used to start a downstream dc-to-dc converter, as shown in Figure 2.

Another use of the $\overline{\text{PG}}$ output is to enable another hot swap device, sequencing on power to another load. In the example shown in Figure 11, the $\overline{\text{PG}}$ output of one TPS2392 pulls low on the overvoltage resistor divider of another TPS2392 to start the second TPS2392, while the OV input also retains the over-voltage protection function.

Depending on the size of the load capacitor and the IRAMP capacitor, the output may pull low when the load capacitor is fully charged, or it may be delayed while IRAMP continues to charge to 5 V. If a delayed turn-on of the dc-to-dc converter or following TPS2392 is desired, select a large IRAMP capacitor on the preceding TPS2392.

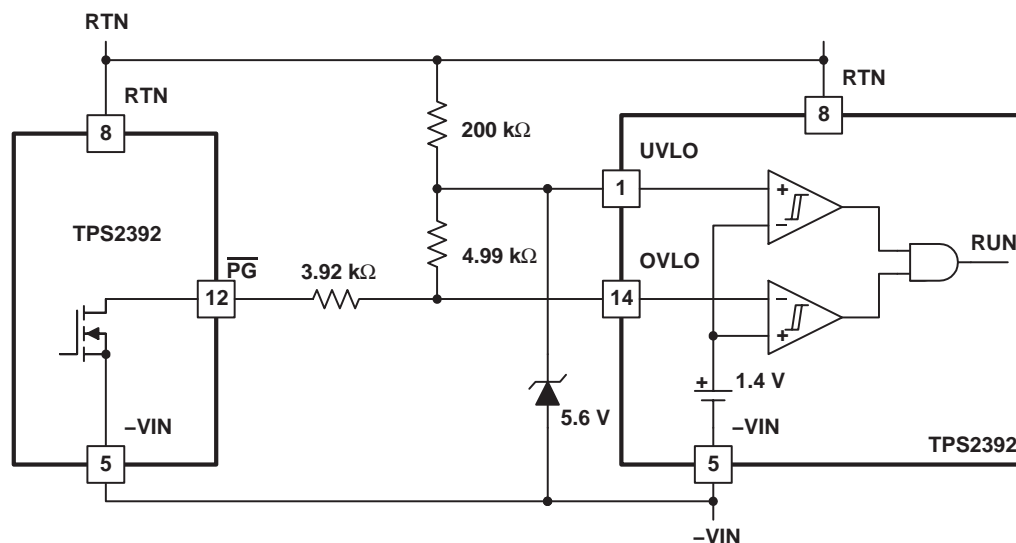


Figure 11. Using the TPS2392 PG Output to Turn On Another TPS2392

3 References

1. IPC-D-275 available from IPC; 2215 Sanders Rd; Northbrook, IL 60062; 1-847-509-9700; For more information about IPC, see their website: <http://www.ipc.org/>

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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