Powering today's multi-rail FPGAs and DSPs, Part 2

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Power Management Products/Portable Power dc/dc Applications

Introduction

Most electronics have one or more digital processing ICs, such as FPGAs or DSPs, that require multiple power-supply rails. There are various options to consider and potential pitfalls to avoid in powering these digital ICs. This article, Part 2 of a two-part series, provides recommendations and guidance for developing a power solution for multi-rail applications where the input power supply voltage is assumed to be equal to or greater than the system rail voltage (e.g., 12, 5, or 3.3 V). While Part 1 (see Reference 1) discussed system-level concerns such as the power budget and sequencing options, this article focuses on how to choose between the types of point-of-load (POL) dc/dc converters and how to design them to meet dc accuracy, start-up, and transient requirements.

Review of step-down dc/dc converter topologies

There are two types of step-down or "buck" POL dc/dc converters: linear regulators and inductor-based switching regulators. Figure 1 shows the functional diagram of a linear regulator.

The primary benefit of linear regulators is the low cost of their ICs, design time, and board area, since they have an internal switch and need only an input and output capacitor. In addition, linear regulators provide a clean, low-noise output voltage. Their primary drawback is low efficiency, equal to V_{OUT}/V_{IN} at heavy load, resulting in a power dissipation of $(V_{OUT}-V_{IN}) \times I_{OUT}$. Power is lost as heat that must be dissipated by the regulator's package and/or external heat sink. Since the minimum input voltage for most regulators currently on the market is 1.8 to 2.7 V, linear regulators are best suited for higher-voltage rails with lower load currents. A second drawback seen in the lowest-cost, featureless regulators is fast, uncontrollable startup, which will be discussed later in this article.

Figure 1. Linear regulator

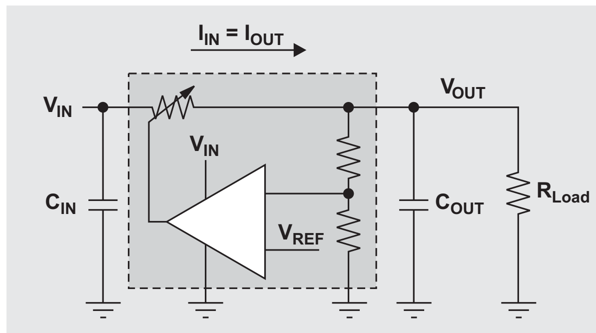
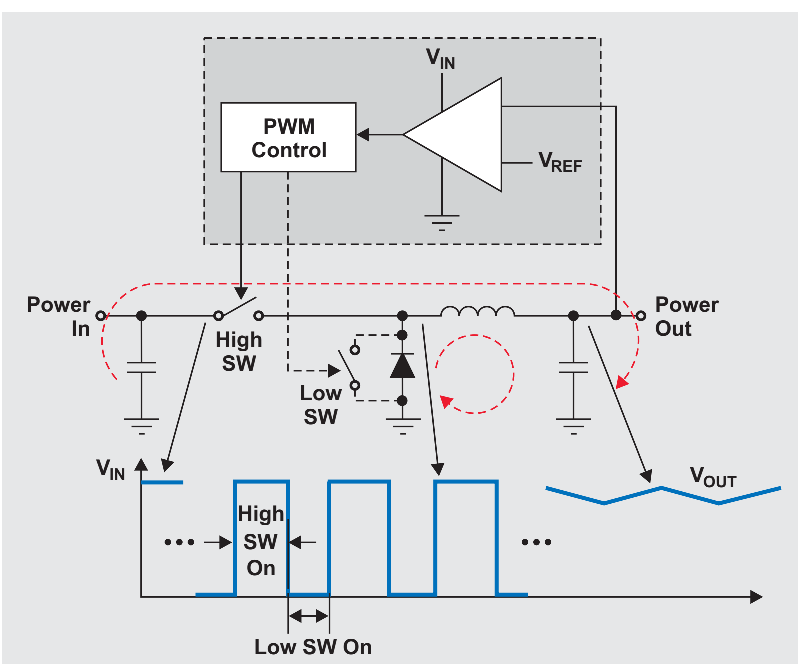


Figure 2 shows a block diagram of a synchronous buck switching regulator. Buck switching regulators use two switches to generate a pulse train with a duty cycle equal to V_{OUT}/V_{IN}. The regulator's feedback control loop modulates either the pulse width of a fixed-frequency pulse train or both the pulse frequency and width to maintain regulation as the load varies, hence the term "pulse width modulation" (PWM). The square-wave pulse train is then filtered by an inductor and capacitor (the LC output filter) to provide a dc output voltage with a triangular-shaped output voltage ripple.

The converter's topology, whether with fixed- or variable-frequency PWM, influences output ripple. The control loop for fixed-frequency PWM converters uses an error amplifier with a negative feedback loop that regulates the output voltage across a load range by modulating the pulse width.

Figure 2. Synchronous buck switching regulator



The output ripple of these regulators is formed by the product of the inductor ripple current and the output capacitor's equivalent series resistance (ESR). Thus, choosing a larger inductor than necessary and a low-ESR output capacitor minimizes output ripple. However, low-ESR output capacitors make the feedback loop more difficult to compensate. Fortunately, power IC manufacturers provide power-supply design software that greatly reduces the design time for fixed-frequency PWM converters. The control loop for most variable-frequency converters consists of a comparator, with either time or voltage hysteresis, that turns the switch on or off if the output voltage goes respectively below or above the reference voltage. These hysteretic converters require less design time than fixed-frequency converters due to their simplified control loop. In addition, since the comparator turns the switch on almost immediately after the output falls below the comparator's reference voltage, a hysteretic converter may respond faster to current increases (transients) than the fixed-frequency converter with a finite-bandwidth control loop. However, a hysteretic converter requires a minimum output ripple to operate.

Compared to linear regulators, switching converters have much higher efficiency (85 to 95% typically), but the cost of their ICs, support components, design time, and board area is usually higher. Another drawback of switching regulators compared to linear regulators is their switching noise (e.g., EMI) and output ripple. Switching noise can be minimized through careful component selection, such as shielded inductors and low-ESR output capacitors, and through proper board layout. Hysteretic converters produce output voltage ripple and radiated emissions at variable switching frequencies, which may be difficult to filter. However, when either the output current or the input-to-output differential is large or the input supply has limited power—e.g., an inexpensive wall brick—only a switching converter can provide high enough efficiency to minimize the power lost through heat.

Step-down switching converters are available in various levels of integration. Drop-in modules have limited design flexibility and tend to cost more; but they require the least amount of design time, needing only an input and output capacitor. At the other extreme are controllers that require external switches as well as the inductor, filter capacitors, and compensation components. They have the most design flexibility and, with enough design effort, can be the most cost-effective solution; but they usually consume the largest amount of board space. In between are the integrated FET buck converters that require less board area, have somewhat less design flexibility, and vary in total solution cost compared to controllers. A synchronous converter/controller uses transistors for both switches and therefore is typically more efficient than a converter that uses a diode for the low-side switch, especially when the output voltage is below 2 V. Therefore, the choice between a linear regulator, a fixed-frequency controller/converter, or a hysteretic controller/converter depends on application requirements as well as on balancing efficiency, cost, and size.

Converter output voltage accuracy

The dc tolerance of most FPGA and DSP core and I/O rails is still ±5%; however, tolerances for some core rails as well as power rails for other ICs have dropped to ±3%. The lower end of the tolerance range (–5 or –3%) is typically the minimum voltage at which some performance standard (e.g., DSP operating speed) is guaranteed for a particular IC. The upper end of the range may be close to the IC's absolute maximum operating voltage. Understanding how to compute the dc tolerance for a power supply is critical not only to guarantee performance but also for system reliability. The dc tolerance does not include dips due to load-step transients. A load-step transient occurs when a digital device being powered by the POL converter increases its load-current demand very quickly. The factors that contribute directly to the dc tolerance for a power supply are the reference voltage tolerance, the feedback resistor tolerance, and the IC's line and load regulation specifications. As an example, an excerpt from the datasheet of the TPS54310 adjustable buck switching converter (see Reference 2) is shown in Figure 3.

Figure 3. Excerpt from TPS54310 datasheet

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CUMULATIVE REFERENCE						
V_{ref}	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation (1) (3)	I_L = 1.5 A, f_S = 350 kHz, T_J = 85°C			0.07	%/V
		I_L = 1.5 A, f_S = 550 kHz, T_J = 85°C			0.07	
	Load regulation (1) (3)	I_L = 0 A to 3 A, f_S = 350 kHz, T_J = 85°C			0.03	%/A
		I_L = 0 A to 3 A, f_S = 550 kHz, T_J = 85°C			0.03	

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10 of TPS54310 datasheet.

Table 1 computes the percentage that the 1.2-V ±5% output can dip during a load transient and still be within regulation, assuming a 5-V ±10% input rail and a 100-mA to 3-A dc output load range. Line regulation and load regulation specifications vary per device, even if those devices are from the same power IC manufacturer, so care must be taken when they are used in a calculation. Most recent converters have voltage feedforward, virtually eliminating the output voltage's dependence on input voltage and making line regulation almost negligible. Load regulation is a function of the power IC's loop gain; higher loop gain gives better load regulation. Note that many converters with fixed output voltages and internal compensation have better output voltage accuracy because the output voltage can be set by trimming the internal feedback resistors.

In the example in Table 1, only 2.843% of 1.2 V or 34.1 mV is available for load transient dip before the output voltage will fall below the –5% minimum tolerance. The capacitor(s) on the power rail must be able to supply this load current until the converter can respond, or the voltage will fall below regulation. Capacitors of various sizes and with low series resistance and inductance are paralleled for handling load transients. Sizing of the capacitors for this "decoupling network" and how that affects converter response time is discussed later in this article.

Table 1. Converter accuracy

CONTRIBUTING FACTOR	COMPUTATION	DROOP (%)
V_{REF} accuracy		–1
1% external feedback resistors	2 x $(1–V_{REF}/V_{OUT})$ x TOL	–0.5
Worst-case output ripple	Design for $V_{OUT(PP)}$ < 1% x V_{OUT}	–0.5
Line regulation	(0.07%/V) x (5.5 – 4.5) %	–0.07
Load regulation	(0.03%/A) x (3 – 0.1) A	–0.087
Total		–2.157
Remainder for load-transient dips	(5% – 2.157%)	2.843

Implementing a controlled monotonic rise of the power rail

The final recommended power-supply design practice to be discussed is monotonic rise at startup, as shown in the top graph of Figure 4.

Figure 4. Start-up voltage and current

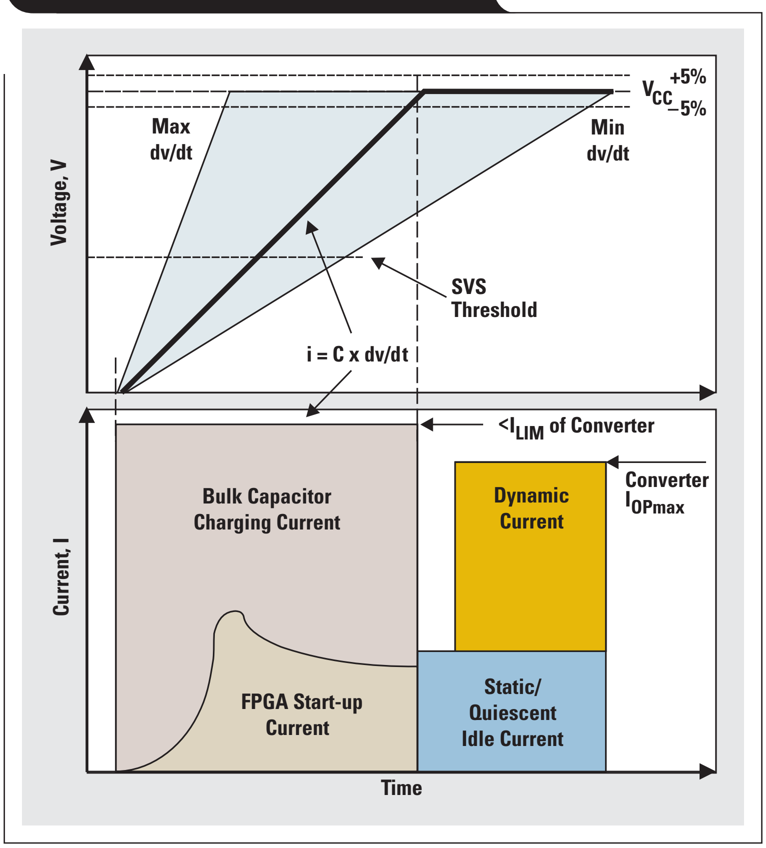
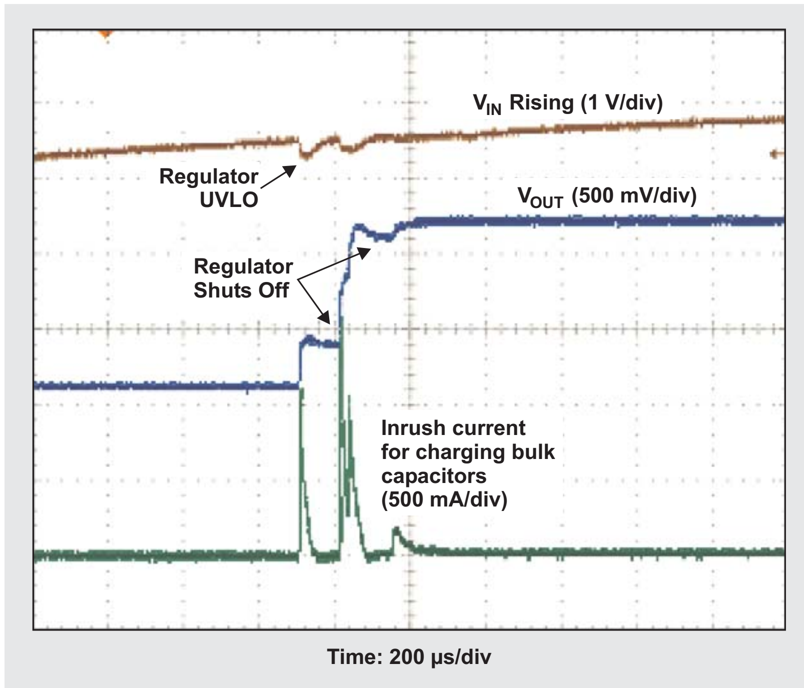


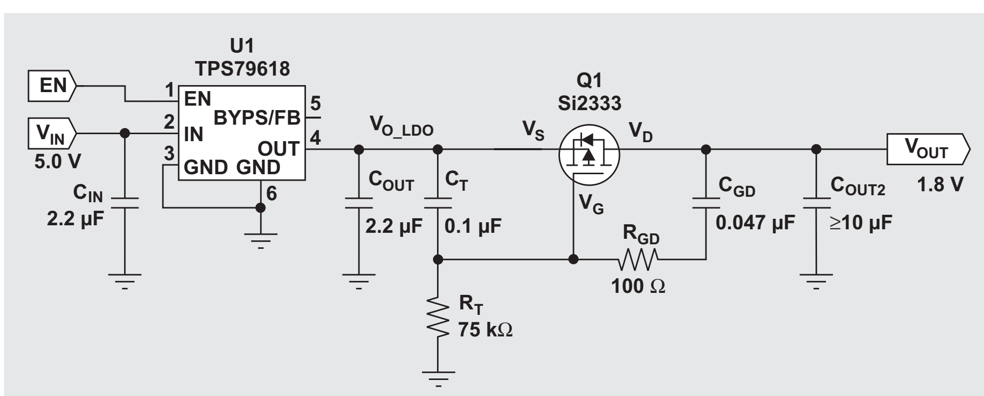
Figure 5. Linear regulator driving a large capacitive load



If the bulk capacitance is too large, thereby forcing the POL converter into current limit during startup, there is a risk of the converter cycling in and out of thermal shutdown and thereby never reaching regulation. A more common start-up problem for fast-starting linear regulators occurs when their input supply gets pulled down at startup, temporarily tripping the regulator's undervoltage lockout (UVLO) until the input capacitor recharges. This causes the regulator to repeatedly turn off briefly and then back on, resulting in the output voltage appearing to oscillate and/or finally ratcheting up to the final voltage. Figure 5 shows an example of a fast-starting linear regulator being powered from a bench supply, pulling the input supply down, tripping UVLO and turning off, repeating the same cycle, then finally reaching its regulated output voltage.

Few linear regulators have a controllable soft start. At startup, they provide current up to their current limit to charge the output capacitance until they either thermally limit themselves or pull down the input rail as shown in Figure 5. All switching converters have some sort of soft start, whether internally fixed or externally adjustable. A FET following any dc/dc converter can be used as a current-limiting switch to provide a soft start. Figure 6, taken from Reference 3, shows such an application; and Figure 7, also taken from Reference 3, shows the results of soft starting.

Figure 6. Linear regulator with FET following to provide soft start



There are two methods that linear regulators and switching converters commonly use to implement a soft start: reference voltage-controlled or current-limit-controlled. In both, a small external capacitor (in the picofarads to 1-µF range) controls the soft-start timing. A voltage-controlled soft start is usually implemented by slowly ramping up the reference voltage. Since the feedback loop forces the converter to provide enough current so that the output voltage follows the reference voltage, the output voltage ramps proportional to the soft-start capacitor that is providing the reference voltage during startup. A simple timing equation determines the size of the external capacitor needed to set the dv/dt of the output voltage. Assuming that the inrush current is predominantly for charging bulk capacitors, C_{Bulk}, the inrush current will be fixed, as shown in Figure 4, at $i = C_{Bulk} \times dv/dt$. Ratiometric sequencing, discussed in Part 1 of this series, can be implemented by having two converters with this type of soft start share the same soft-start capacitor. When using a current-limit-controlled soft start, the converter either slowly ramps or incrementally steps up the current limit to the maximum. The converter then looks like a current source, providing a slowly increasing current to the load. The voltage feedback loop still tries to provide the desired output voltage, so the converter provides as much current as the current limit (and any thermal protection) will allow. The output voltage's exact ramp rate, dv/dt, varies as a function of the absolute value of the output voltage (i.e., a 1.2-V rail will ramp more quickly than a 3.3-V rail), the resistive and capacitive loading on the rail, and the converter's final current-limit setting.

Dealing with load-step transients

All POL dc/dc converters have a finite transient response time, whether it's the loop bandwidth of the traditional PWM converter or the fixed on/off times of the hysteretic converter. Figure 8 shows the response of a low-current linear regulator to a change in the output load current—for example, a line of code that causes a DSP to perform complex computations.

Figure 7. Linear regulator with FET following to provide soft start

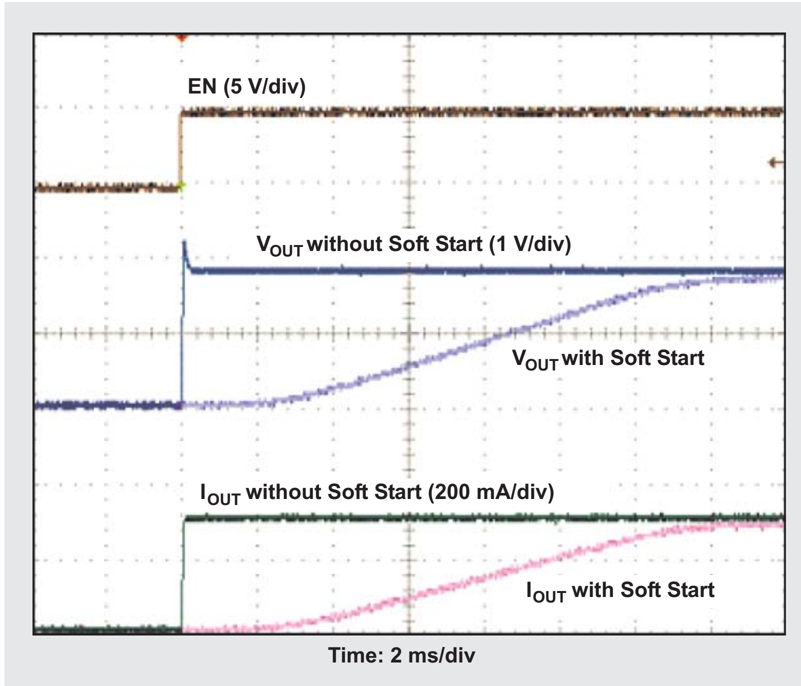


Figure 8. Example load-step transient response

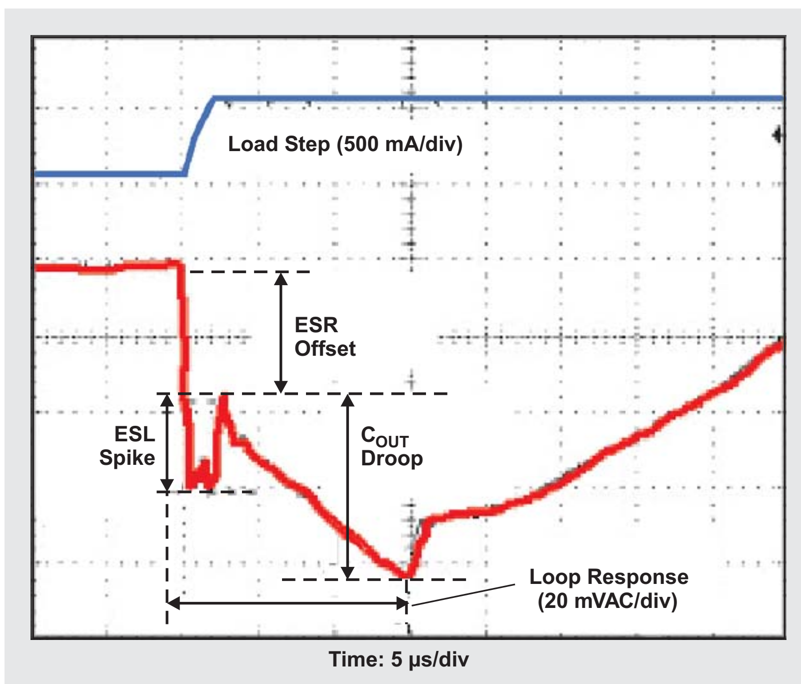
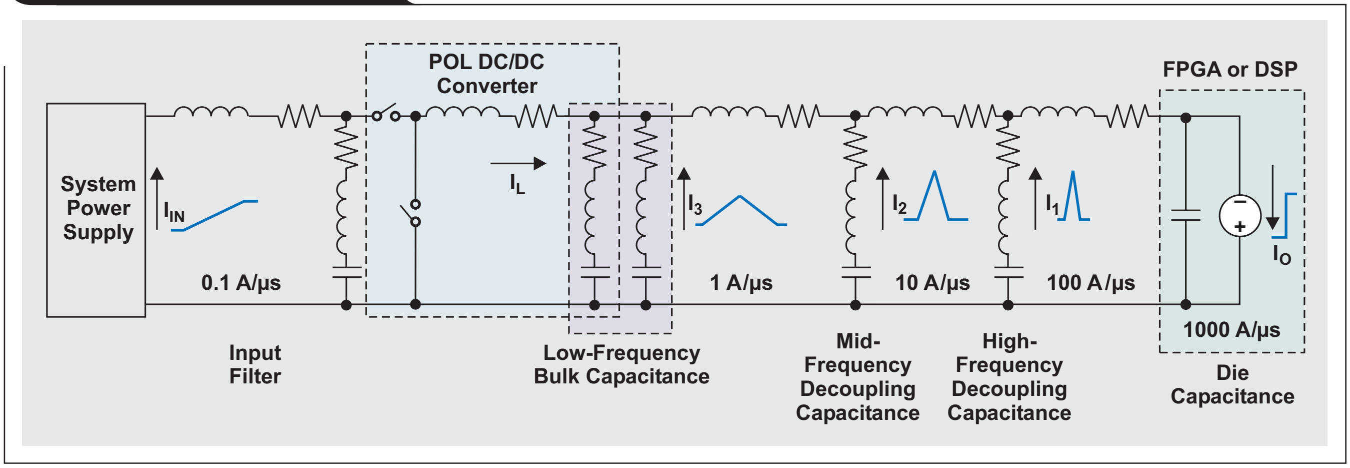


Figure 9. Decoupling network



Using output capacitors with low ESR and equivalent series inductance (ESL) helps to minimize the transient droop. However, additional capacitance is almost always required at the power rail's output and localized bypass capacitance to assist the converter in handling the step transient. Figure 9 shows load-step-transient propagation and its suppression by a decoupling network. The various-sized capacitors suppress the different frequency components of the load-step transient so that the POL converter, and ultimately its input power supply, have to support only the small, low-frequency component of the load step. For example, if the FPGA or DSP gives a load step of 1000 A/µs, then the decoupling network suppresses the transient so that the converter has to respond only to a 1-A/µs transient.

Small capacitors (in the picofarads to 1-µF range) handle the high-frequency component of the load step. Capacitors from 1 to 22 µF handle the mid-frequency component, and low-ESR bulk capacitors from 47 to 1000 µF handle the low-frequency component. A common method for optimizing the decoupling network (i.e., minimizing the amount of capacitance added) is the target-impedance method, which is explained more fully in Reference 4. This method requires that the designer know the worst-case load-step transient of the device being powered (e.g., from 200 mA to 2.2 A in 0.5 µs or 4 A/µs for 10 µs) and have some idea of the transient-response capabilities of the POL converter. If the POL converter is not close to the digital IC being powered and/or the board layout requires that the power rail use small traces and/or vias to get to the load, then approximations of the board resistance and inductance may be necessary for the model, as illustrated in Figure 9.

For most FPGA and DSP applications, the worst-case load-step transient is rarely known and it is simpler to use rules of thumb to design the decoupling network. For example, it is not uncommon to allocate a certain percentage of each capacitor type (high-, mid-, and low-frequency) per the number of power pins used in total or per section of the digital IC. While effective, this method tends to overdesign the decoupling network, underutilizing the linear regulator's or switching converter's transient-response capabilities and consuming board space for extra capacitance.

With rule-of-thumb methods, the decoupling network and POL converter are designed independently. This poses a risk that the POL converter may become unstable due to the additional capacitance of the decoupling network; so it is critical that the converter be compensated for the total capacitance at its output. Texas Instruments has reference documents and design software at power.ti.com/swift to assist with converter design and compensation. Artificially applying a load-step transient to the output of the converter and observing the ringing (oscillations) on the output voltage as the converter responds to the transient is another way to determine stability of the converter. As a rule of thumb, if the converter has over three oscillations before settling, it is considered on the verge of being unstable (underdamped). A slow response with no ringing or overshoot is considered to be very stable (overdamped).

PC processors can have multiple load-step transients in the 1000-A/µs range and so require both a fast transient POL converter and a large decoupling network. To reduce the cost of the decoupling network and minimize the board space it uses, PC motherboard manufacturers now use the target-impedance method or a similar method to minimize the number of capacitors and to take full advantage of the transient capabilities of the dc/dc converter. Individual FPGA and DSP applications are currently lower-power and slower-switching compared to PC processors. So, until either FPGAs or DSPs generate load steps similar to PC processors or the size or cost of the decoupling network becomes too large, a rule-of-thumb approach to sizing the decoupling network is a reasonable compromise between optimal design and fast time to market.

Conclusion

Choosing the right power-supply solution for multi-rail applications is more than balancing size, efficiency, and cost between a linear regulator and the various types of switching converters. Issues such as power-up sequencing and start-up current management must also be considered. In addition, the converter will most likely need the help of decoupling capacitors to maintain regulation during load-step transient events.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title **TI Lit. #**

1. Jeff Falin, "Powering today's multi-rail FPGAs and DSPs, Part 1," slyt232
2. "3-V to 6-V Input, 3-A Output Synchronous-Buck PWM Switcher with Integrated FETs (SWIFT™)," TPS54310 Datasheet slvs412
3. Jeff Falin, "Monotonic, Inrush Current Limited Start-Up for Linear Regulators," Application Report slva156
4. "Practical Considerations in Current Mode Power Supplies," Application Report slua110

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