Evaluation Board for 8-Channel, 10-/12-Bit ADC with I²C Compatible Interface

EVAL-AD7997/AD7998

FEATURES

Evaluation board for the AD7997/AD7998
Standalone capability only
Various linking options

GENERAL DESCRIPTION

This data sheet describes the evaluation board for the AD7997 10-bit and AD7998 12-bit, I²C-compatible, successive-approximation ADCs. These ADCs operate from a single 2.7 V to 5.5 V power supply and feature throughput rates of up to 188 kSPS. Full details on the AD7997/AD7998 are available in the AD7997/AD7998 data sheet that is available from Analog Devices, Inc. and should be consulted in conjunction with this data sheet when using the evaluation board.

This evaluation board is intended for standalone operation, which requires the user to power the board and provide all I²C control signals through external connectors. Power and control signals are connected to the board through the connectors listed in Table 5. For details on I²C interface timing, see the AD7997/AD7998 data sheet.

On-board components include an AD780, which is a pin programmable +2.5 V or +3 V ultrahigh precision band gap reference, a REF192 +2.5 V reference, and an AD713 op amp. Also included are inverters on the interface lines.

FUNCTIONAL BLOCK DIAGRAM

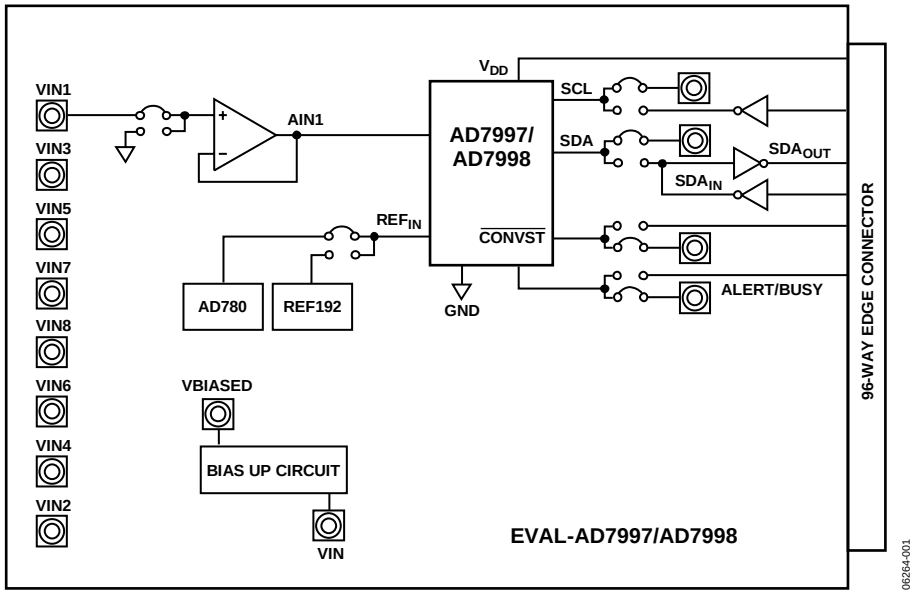

Figure 1.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

10/07—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Because this board is used as a standalone unit, external supplies must be provided. This evaluation board has five power supply inputs, as follows:

- EXT_VDD
- AGND
- +12 V
- −12 V
- AGND

A 2.7 V to 5.5 V supply must be connected to the EXT_V_{DD} input. The +12 V and −12 V supplies are required for the op amps. The supplies are decoupled to the ground plane with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors at the point where they enter the board. The supply pins of all the op amps and the reference are also decoupled with 10 µF tantalum and 0.1 µF ceramic capacitors, as are the V_{DD} pins.

LINK OPTIONS

There are 30 link options that must be set according to operating setup requirements before the evaluation board can be used. These link options and their functions are outlined in Table 1.

Table 1.

Link No.	Function
LK1 to LK8	Connect the inputs of the AD713 to the input sockets (VIN1 to VIN8) or tie the AD713 inputs to AGND. In Position A, the relevant AD713 input is connected to the relevant input SMB socket. In Position B, the relevant AD713 input is connected to AGND.
LK9	Selects the source of the VDD supply to the AD7997/AD7998. In Position A, the supply voltage is taken from the 96-way connector. In Position B, the supply voltage is taken from an external source via J2.
LK10	Selects the source of the REFIN voltage to be applied to the REF_{IN} pin of the AD7997/AD7998 and to the bias up circuits. In Position A, the AD780 supplies the +2.5 V reference to the AD7997/AD7998. In Position B, the REF192 supplies the +2.5 V reference to the AD7997/AD7998. In Position C, the reference is taken from the externally applied reference via the REFIN SMB socket.
LK11	Controls the program pin of the AD780 voltage reference. When inserted, the AD780 output voltage is set to +3.0 V. When removed, the AD780 voltage is set to +2.5 V.
LK12	Selects the source of the CONVST input signal for the AD7997/AD7998. In Position A, the CONVST signal is taken from the 96-way connector. In Position B, the CONVST signal is taken from the externally applied CONVST signal via the SMB socket.
LK13	Selects the voltage being applied to the AS pin, which is used to set the final three bits of the AD7997/AD7998 I^2C bus address. In Position A, the AS pin is tied to VDD. In Position B, the AS pin is tied to AGND. Refer to the AD7997/AD7998 data sheet for the I^2C address for each configuration.
LK14	Adds a 51 Ω termination resistor to AGND at the VIN input socket. When a 51 Ω termination is required, this link should be inserted.
LK15	Selects the source of the +12 V supply for the EVAL-AD7997/AD7998. In Position A, the +12 V supply is sourced from the 96-way connector. In Position B, the +12 V supply is sourced externally via J3.
LK16	Selects the source of the −12 V supply for the EVAL-AD7997/AD7998. In Position A, the −12 V supply is sourced from the 96-way connector. In Position B, the −12 V supply is sourced externally via J3.
LK17	Selects the serial clock to feed into the 74HC05. In Position A, the SCL signal comes from the 96-way connector. In Position B, the SCL signal comes from the external SMB socket, \SCL.
LK18	Selects the destination for the inverted SDA output from the AD7997/AD7998. In Position A, the inverted SDA signal is fed to the 96-way connector. In Position B, the inverted SDA signal is fed to the SDA_O/P SMB socket.
LK19	Selects the source of the SDA signal to be fed into the 74HC05. In Position A, the SDA signal comes from the 96-way connector. In Position B, the SDA signal comes from the external SMB socket, SDA_I/P.

Link No.	Function
LK20	Selects the serial clock to feed into the SCL pin of the AD7997/AD7998. In Position A, the SCL signal comes from the SMB SCL socket. In Position B, the SCL signal comes from the \SCL socket.
LK21	Selects the source/destination of the SDA signal to/from the SDA pin of the AD7997/AD7998. In Position A, the SDA signal comes from/goes to the SMB SDA socket. In Position B, the SDA signal comes from/goes to the 74HC05 chip, whose input/output signal in turn is chosen by LK18 and LK19.
LK22	Selects the destination of the ALERT/BUSY signal. In Position A, the ALERT/BUSY signal is fed to the SMB ALERT socket. In Position B, the ALERT/BUSY signal is fed to the 74HC05, where the inverted output is fed to the 96-way connector.
K1 to K8	Add a 51 Ω termination resistor to AGND at the VIN1 to VIN8 input sockets. When a 51 Ω termination is required, these links should be inserted.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions support the required operating mode. Table 2 shows the positions in which the links are set when the evaluation board is packaged. The board is set up for standalone capability.

Table 2. Initial Link Positions

Link No.	Position	Function
LK1	A	The input of AD713 is connected to the VIN1 SMB socket.
LK2 to LK8	B	AD713 inputs are connected to AGND.
LK9	B	The V_{DD} supply is taken from the J2 socket.
LK10	A	The AD780 supplies the 2.5 V reference to the AD7997/AD7998.
LK11	OUT	AD780 voltage is set to 2.5 V.
LK12	B	The CONVST signal is taken from the CONVST SMB socket (externally generated signal).
LK13	A	The AS pin is tied to VDD; see the AD7997/AD7998 data sheet for the I^2C address.
LK14	OUT	No 51 V termination on the inputs.
LK15	B	+12 V supply is generated externally and applied through the J3 socket.
LK16	B	−12 V supply is generated externally and applied through the J3 socket.
LK17	B	The SCL signal to be fed from the \SCL socket.
LK18	B	The inverted SDA output signal is available at the SDA_O/P SMB socket.
LK19	B	The SDA signal to be applied to the 74HC05 inverter input is applied through SMB SDA_I/P.
LK20	A	The SCL pin on the AD7997/AD7998 is connected to the SMB SCL socket.
LK21	A	The SDA pin on the AD7997/AD7998 is connected to the SMB SDA socket.
LK22	A	The ALERT/BUSY pin on the AD7997/AD7998 is connected to the SMB ALERT socket.
K1 to K8	OUT	No 51 V termination on the inputs.

EVALUATION BOARD INTERFACING

Interfacing to the evaluation board is via a 96-way connector, J1. The pinout for the J1 connector is shown in Figure 2, and its pin designations are given in Table 4.

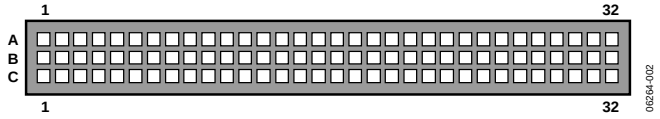

Figure 2. Pin Configuration for the 96-Way Connector J1

Table 3.

Pin	Description
FO	Flag Out. This pin is used to transmit data from the DSP into the SDA pin of the AD7997/AD7998.
FL1	Flag Out 1. This pin is used to generate the CONVST pulse to initiate a conversion.
FI	Flag In. This pin is used to transmit DATA into the DSP from the SDA pin of the AD7997/AD7998.
FL0	Flag Out 0. This pin is used to provide the SCL signal from the DSP to the AD7997/AD7998.
$\overline{IRQ2}$	Interrupt Receive. This pin is connected to the ALERT/BUSY pin of the AD7997/AD7998. It can be used to provide an interrupt when an ALERT occurs.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
VDD	Analog +5 V Supply. These lines are connected to the VDD supply line on the board via LK9.
−12 V	−12 V Supply. This line is connected to the −12 V supply line on the board via LK16.
+12 V	+12 V Supply. This line is connected to the +12 V supply line on the board via LK15.

Table 4. Pin Designations for the 96-Way Connector J1[1]

Pin	Row A	Row B	Row C
1	FO	FL1	FI
2			
3			
4	DGND	DGND	DGND
5			
6			
7			
8			
9			
10			
11			
12	DGND	DGND	DGND
13			
14			
15			
16	DGND	DGND	DGND
17	FL0		$\overline{IRQ2}$
18			
19			
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29		AGND	
30	−12 V	AGND	+12 V
31			
32	VDD	VDD	VDD

[1] The unused pins of the 96-way connector are not shown.

SOCKETS

There are 21 input/output sockets relevant to the operation of the AD7997/AD7998 on this evaluation board. The functions of these sockets are outlined in Table 5.

Table 5.

Socket	Function
J1	96-way connector for serial interface and power supply connections.
J2	External VDD and AGND power connector.
J3	External +12 V, −12 V, and AGND power connector.
VIN	SMB socket for bipolar input signal to bias up.
VBIASED	SMB output from bias up circuit; unipolar out.
VIN1 to VIN8	8 SMB sockets for Analog Input Channels 1 to 8.
REFIN	SMB socket for REFIN voltage.
\SCL	SMB socket for inverted external SCL input.
SCL	SMB socket for an external SCL input.
CONVST	SMB socket for external CONVST input signal.
SDA_I/P	SMB socket for external SDA input data, SDA
SDA_O/P	SMB socket for SDA data out from AD7997/AD7998; data is inverted before it is applied to this socket.
ALERT	SMB socket for the ALERT/BUSY output.
SDA	SMB socket for SDA data to/from the AD7997/AD7998.

EVALUATION BOARD SCHEMATICS AND ARTWORK

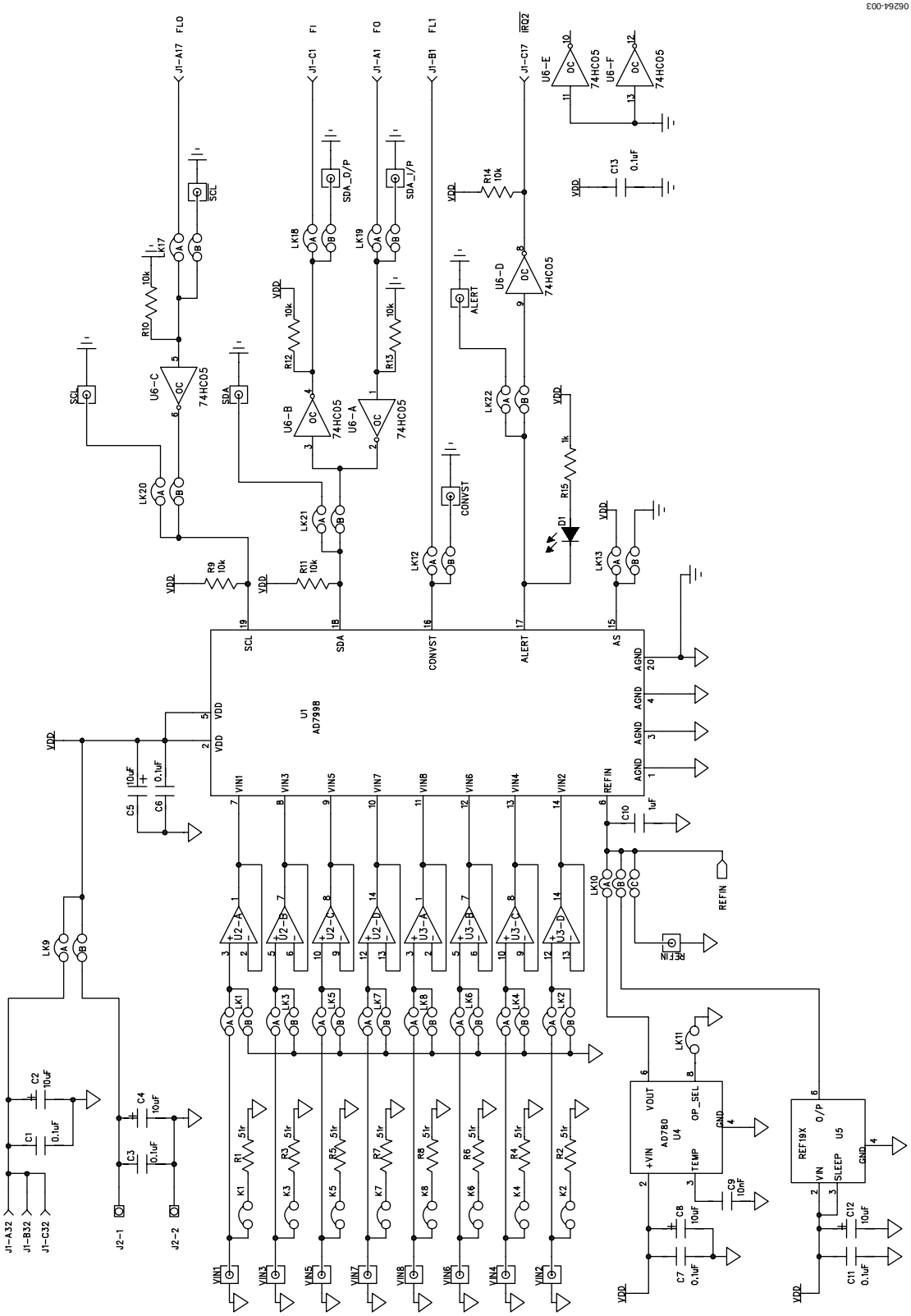

Figure 3. AD7997/AD7998 Evaluation Board Schematic 1

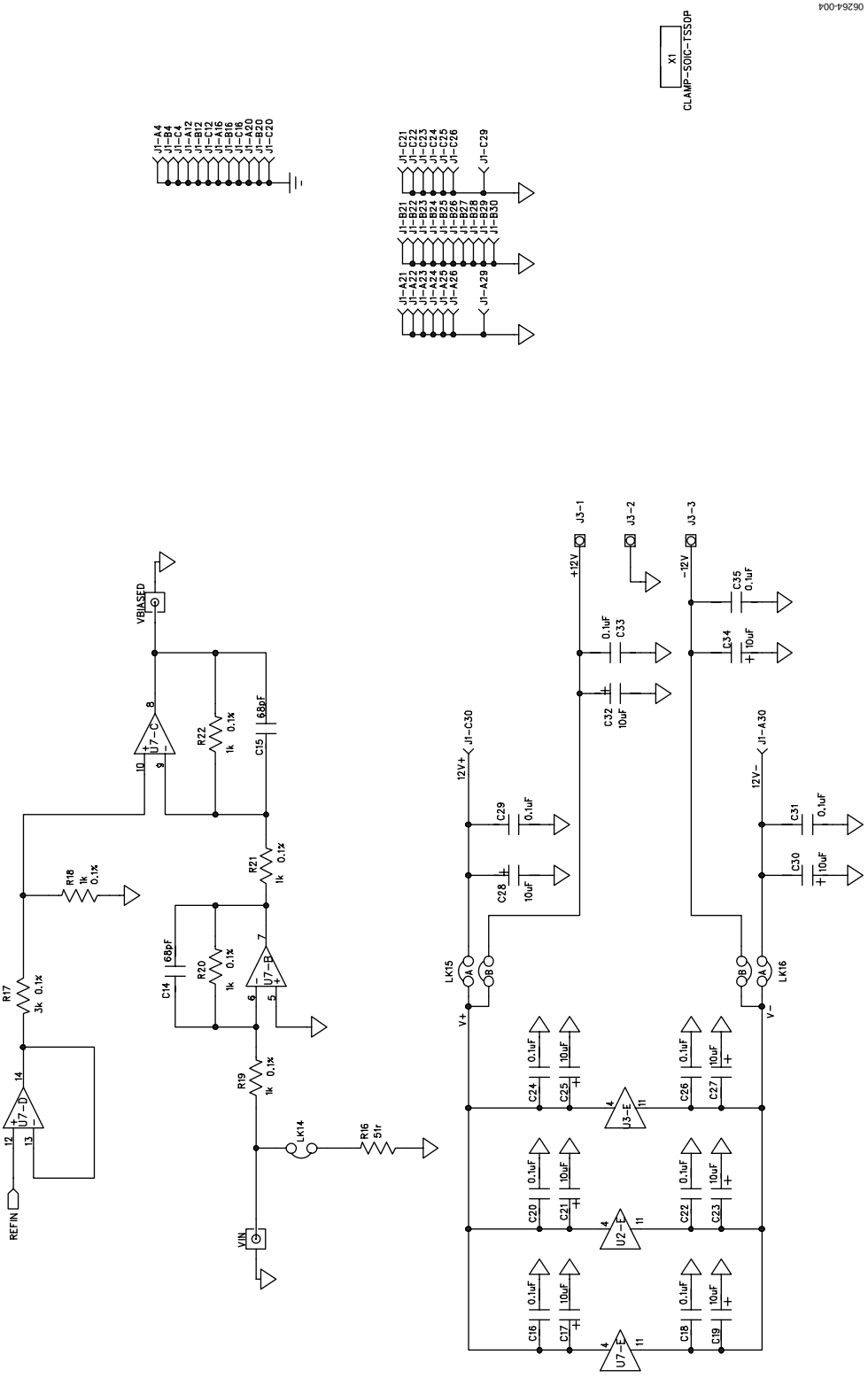

Figure 4. AD7997/AD7998 Evaluation Board Schematic 2

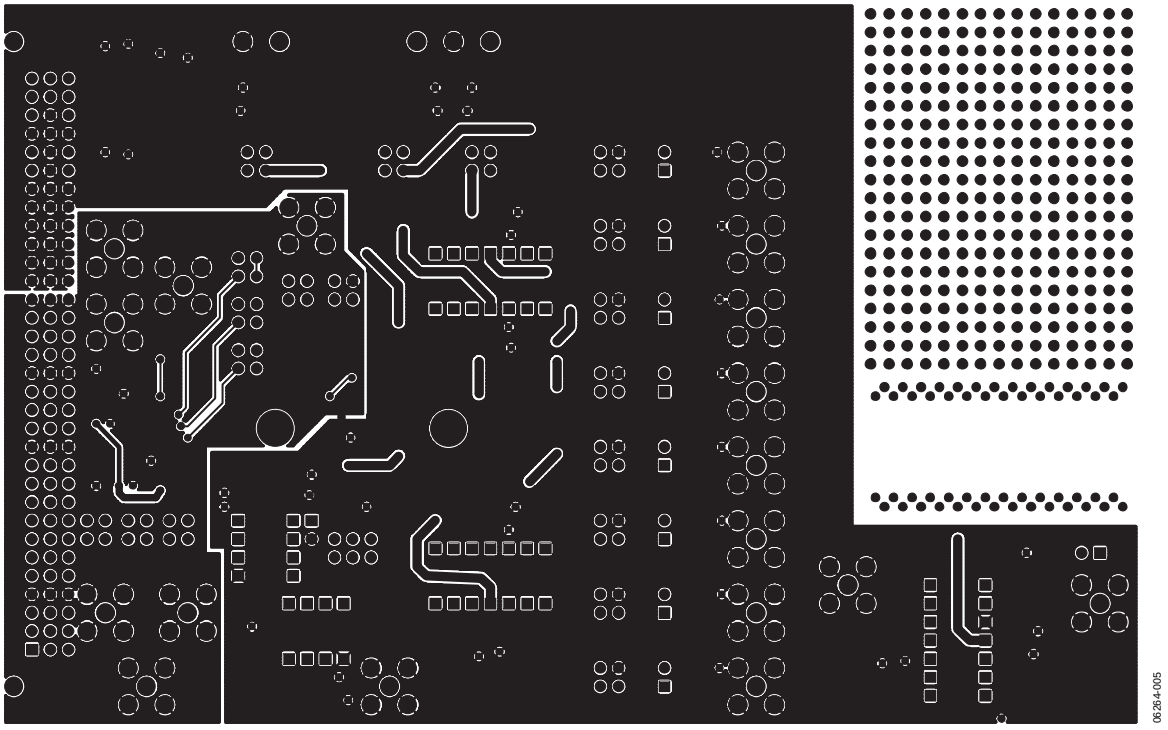

Figure 5. Bottom Layer Etch

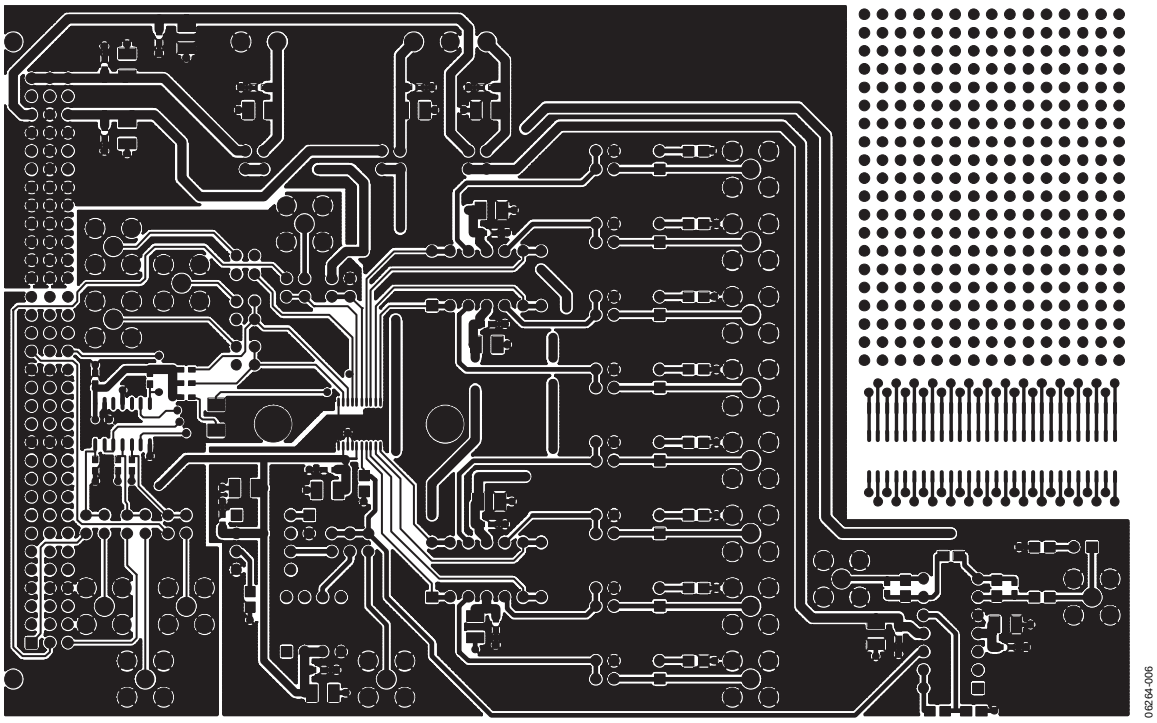

Figure 6. Top Layer Etch

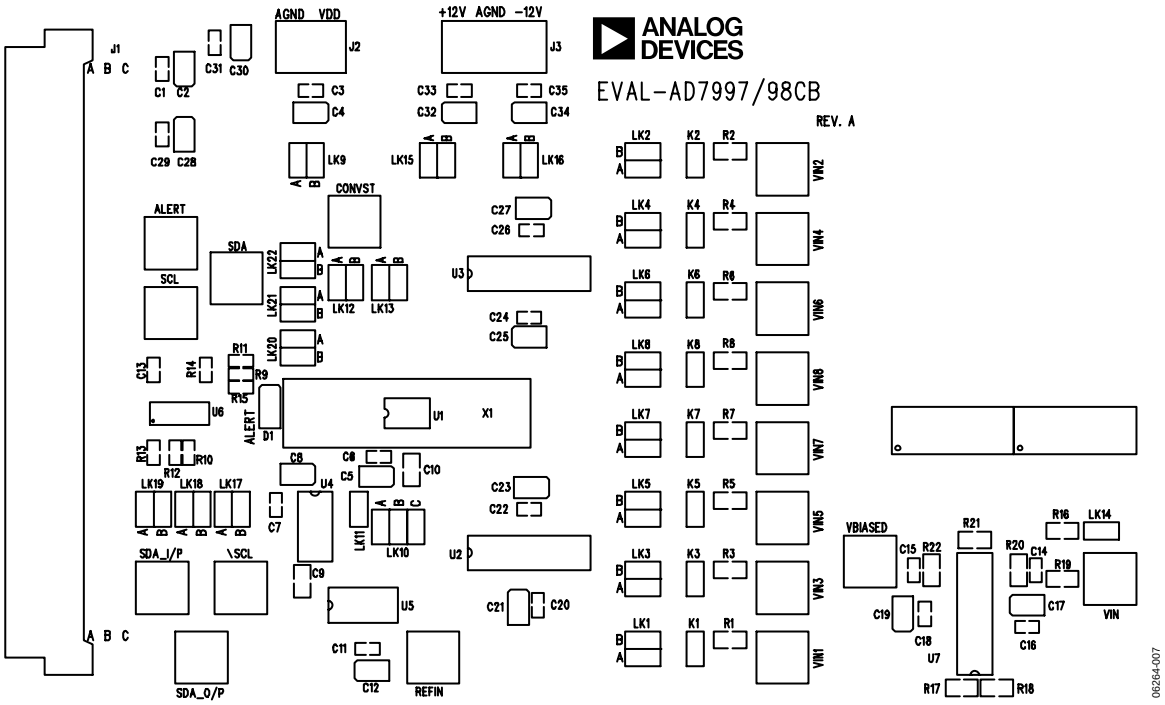

Figure 7. Silk Screen Top Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 6.

Qty	Reference Designator	Description	Order Number[1, 2]
16	C1, C3, C6, C7, C11, C13, C16, C18, C20, C22, C24, C26, C29, C31, C33, C35	0.1 µF multilayer ceramic capacitor (10% tolerance)	FEC 432-210
15	C2, C4, C5, C8, C12, C17, C19, C21, C23, C25, C27, C28, C30, C32, C34	10 µF 16 V SMD tantalum capacitor (10% tolerance)	FEC 498-737
1	C9	10 nF multilayer ceramic capacitor (10% tolerance)	FEC 499-225
1	C10	1 µF multilayer ceramic capacitor (10% tolerance)	FEC 4765874
2	C14, C15	68 pF multilayer ceramic capacitor (10% tolerance)	FEC 722-066
8	REFIN, SCL, SDA_O/P, SDA_I/P, \SCL, SDA, ALERT, CONVST	Gold SMB 50W jack	FEC 1111349
1	D1	Red SMD LED	FEC 105-8404
1	J1	96-pin DIN41612 90º connector	FEC 1096832
1	J2	2-pin terminal block	FEC 151-789
1	J3	3-pin terminal block	FEC 151-790
8	K1, K2, K3, K4, K5, K6, K7, K8	2-pin header	FEC 1022247 and 150-411
19	LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8, LK9, LK12, LK13, LK15, LK16, LK17, LK18, LK19, LK20, LK21, LK22	4-pin header	FEC 1022233 and 150-411
1	LK10	6-pin header	FEC 1022231 and 150-411
2	LK11, LK14	2-pin header	FEC 1022247 and 150-411
8	R1, R2, R3, R4, R5, R6, R7, R8	0.1 W SMD resistor	FEC 9334629
6	R9, R10, R11, R12, R13, R14	10 k, 0.1 W SMD Resistor	FEC 933-0399
1	R15	1 k, 0.1 W SMD Resistor	FEC 933-0380
1	R16	51 r, 0.1 W SMD Resistor	FEC 9334629
1	R17	3k01, 0.1 W SMD Precision Resistor	FEC 1140856
5	R18, R19, R20, R21, R22	1k, 0.1 W SMD Precision Resistor	FEC 1140805
1	U1	ADC	AD7997-0/AD7998-0BRUZ (Analog Devices)[1]
2	U2, U3	Quad op amp	AD713KNZ (Analog Devices)
1	U4	2.5 V/3 V reference	AD780ANZ (Analog Devices)
1	U5	Voltage reference	REF192GPZ (Analog Devices)
1	U6	Hex inverter with open drain	Digi-key 296-1190-1-ND
1	U7	Quad op amp	AD713KNZ (Analog Devices)
10	VBIASED, VIN, VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, VIN8	Gold SMB 50 W jack	FEC 1111349
1	Part of U1 Socket Assembly	20-pin TSSOP clamp (not normally used)	Supplied by Analog Devices
1	Part of U1 Socket Assembly	Pem nuts (2 total) - 440 thread (not normally used)	MAC-B Ltd.
1	Part of U1 Socket Assembly	Alignment studs (2 total) - 440 thread (not normally used)	MAC-B Ltd. 4000-440-SSC
1	Part of U1 Socket Assembly	Thumb screws (2 total) - 440 thread (not normally used)	MAC-B Ltd. 7120-SS-0
6	U2 to U7	Ultra low profile socket pins (x72)	FEC 519-935
4	Each corner	Stick-on feet (3M)	SJ5076BLACK

[1] FEC = the Farnell Company.
[2] CDs are not used for this evaluation kit.

ORDERING GUIDE

Model	Description
EVAL-AD7997CBZ[1]	AD7997 Evaluation Board
EVAL-AD7998CBZ[1]	AD7998 Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

EB06264-0-10/07(0)