Features

The CompactPCI (cPCI) 6540 Hot Swap Application Note provides design guidelines for a Universal Transparent or Non-Transparent cPCI Hot Swap Add-In board (using the PCI 6540CB PCI-X-to-PCI-X Bridge device). With superior PCI and PCI-X performance, the 64-bit, 133 MHz PCI-X-to-PCI-X PCI 6540 Bridge device provides I/O interconnect solutions to many high-end communications, server, storage, embedded-control, and consumer industries applications.

- **PCI-X Specification r1.0b**-compliant at 64-bit, 133 MHz
- 3.3V signaling with 5V input signal tolerance
- Asynchronous Frequency support for 33 to 133 MHz on primary and secondary PCI Buses
- PICMG 2.1, R2.0, Hot Swap Specification (PICMG 2.1, R2.0), compliant with PI=1 support
- Large 10-KB FIFO for optimal volume data transfer

General Description

The performance-tuned PCI 6540, a PCI-X r1.0b-compliant, 64-bit, 133 MHz PCI-X-to-PCI-X Bridge device, offers excellent performance solutions for various adapters and embedded systems.

The PCI 6540 is designed for high-performance, high-availability applications in Hot Swap Bus expansions, programmable data transfer rate control, frequency conversions from slower-to-faster, or faster-to-slower, PCI Buses. The PCI 6540 offers sophisticated buffer management and configuration options designed to provide customizable performance optimization for efficient PCI-X-to-PCI-X Conversion and Processor bridging.

![cPCI 6540 Hot Swap Design Block Diagram](image)
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>09/22/2004</td>
<td>1.0</td>
<td>Initial release.</td>
</tr>
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</table>
| 01/24/2006 | 1.1     | Updated schematic and PCI specification revision reference.  
           |          | Revised L_STAT information in Section 2.6.                |
| 03/03/2006 | 1.2     | Changed P_AVDD and S_AVDD voltages from 1.8V to 2.5V in the schematics. |
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Introduction

This application note provides design information for cPCI Hot Swap Add-In boards, using the PCI 6540 PCI-X-to-PCI-X Bridge. The subsystem described herein consists of cPCI Hot Swap Board electrical requirements, Hardware Connection control and Hot Swap control logic. This application note references a sample cPCI 6540 Hot Swap design. The sample cPCI 6540 Hot Swap Board reference schematics consist of the PCI 6540, Hot Swap control logic, CPLD control logic, clock routing circuitry, PMC connectors and cPCI edge connectors. (Refer to Section 5, “Schematics.”)

The PCI 6540 is equipped with Hot Swap register support and Hot Swap Control pins—ENUM#, L_STAT, and EJECT—that provide Hot Swap design capability. The PCI 6540 incorporates Hot Swap functionality, which meets PICMG 2.1, R2.0 PI=1 requirements.

Table 1. Hot Swap Control Signals

<table>
<thead>
<tr>
<th>Signal (Pin)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENUM#</td>
<td>Enumeration Output</td>
<td>Used to notify system host that a board has been freshly inserted or is about to be extracted. Asserted when the Hot Swap Control/Status register (offset E6h) INS (Insertion State) or EXT (Extraction State) bit is set (HS_CSR[7:6]=11b, respectively). If used, ENUM# requires an external pull-up resistor (3K to 4.7K Ohms).</td>
</tr>
<tr>
<td>L_STAT</td>
<td>CompactPCI LED On</td>
<td>Upon Insertion, hardware automatically turns ON the L_STAT signal (LED) until the Hardware Connection process completes. Upon Extraction, the LED remains OFF until the Hot Swap software device driver turns ON the LED by setting the Hot Swap Control/Status register (offset E6h) LOO (LED Status) bit (HS_CSR[3]=1) to indicate that Extraction is permitted.</td>
</tr>
<tr>
<td>EJECT</td>
<td>Hot Swap Eject</td>
<td>This handle switching input is de-bounced by external hardware and must be connected to logic 0, if the Hot Swap function is not used. Can cause ENUM# assertion.</td>
</tr>
</tbody>
</table>
1.2 CompactPCI Hot Swap Connections

To implement the cPCI feature, 10-Ohm Stub Termination Series resistors are required for PCI 6540 bus signals. The following diagram outlines the cPCI Bus Hot Swap signal electrical requirements. (Refer to Figure 2.)

During Insertion, the cPCI Bus is placed in a high-impedance state until the cPCI board is fully powered and enabled for PCI Bus access in Configuration space.

![Diagram of cPCI Hot Swap Connections](image)

**Table 2. Hot Swap Signal Electrical Requirements**

<table>
<thead>
<tr>
<th>Item</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cp</td>
<td>Capacitance associated with $R_P$ node, not to exceed 1.0 pF. In Figure 2, $R_P/C_P$ are on the same node as $C_{STUB2}$. However, $R_P/C_P$ may connect anywhere on the trace inside of $R_{STUB}$.</td>
</tr>
<tr>
<td>CSTUB1</td>
<td>Capacitance associated with left node of $R_{STUB}$, not to exceed 1.0 pF.</td>
</tr>
<tr>
<td>DP</td>
<td>The stub length for $R_P$ to be zero, but limited to 2.5 mm (0.1 inches). The capacitance associated with $D_P$ to be included in the capacitance requirement for $C_P$.</td>
</tr>
<tr>
<td>DSTUB</td>
<td>Trace length from connector to $R_{STUB}$, not to exceed 15.2 mm (0.6 inches).</td>
</tr>
<tr>
<td>DTOTAL</td>
<td>Total trace length from connector to PCI device I/O pin, including distance through $R_{STUB}$, not to exceed 63.5 mm (2.5 inches).</td>
</tr>
<tr>
<td>IIL/IH</td>
<td>The PCI signal's TOTAL low- and high-level leakage currents. These requirements apply to all PCI Bus I/Os when not driving the bus. Includes leakage of PCI chip and additional leakage through $R_P$, if present.</td>
</tr>
<tr>
<td></td>
<td>- For 5V only Hot Swap boards—$I_{IH}$ not to exceed +200 µA at $V_{IN}=2.7V$. $I_{IL}$ not to be less than .70 µA at $V_{IN}=0.5V$.</td>
</tr>
<tr>
<td></td>
<td>- For 3.3V only, or Universal Hot Swap boards— $I_{IH}$ not to exceed +55 µA. $I_{IL}$ not to be less than .35 µA if BD_SEL# is connected to the backplane. $I_{IH}$ and $I_{IL}$ requirements apply over the input voltage range 0.0 to 3.3V. For implementations that disconnect the precharge resistors during normal operation (as allowed in PICMG 2.1, R2.0, Section 3.1.3), the $I_{IH}$ and $I_{IL}$ constraints apply during normal operation only and are waived while the precharge resistors are connected. If BD_SEL# is disconnected from the backplane, the leakage values of the 5V boards apply.</td>
</tr>
<tr>
<td>Rp</td>
<td>Precharge voltage source resistance may exist as illustrated in Figure 2, in support of PICMG 2.1, R2.0, Section 3.1.3 precharge voltage requirements. If the PCI chip internally implements precharge, do not use an external $R_P$.</td>
</tr>
</tbody>
</table>
1.3 Precharge Resistor Circuitry (RP) Required for PCI Signals

CompactPCI 6540 Hot Swap board PCI Bus signals require precharge circuitry when the precharge voltage is applied to the cPCI board through a high-impedance source during Hot Swap Insertion. During Early Power, precharging of the Long Power pins (3.3 and 5V), Medium pins (PCI Control signals and standard Power pins), and Short pin (BD_SEL#) is kept to less than 4 ms. To facilitate precharging during Hot Swap Insertion or Extraction, the signals delineated in PICMG 2.1, R2.0 must be connected to specific voltage sources. (Refer to Table 3.)

### Table 3. Signal Voltage Sources

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>51K to VIO</td>
<td>ENUM#, S_CLKin, S_INTA#, S_REQ#, S_RSTIN#</td>
</tr>
<tr>
<td><strong>Note:</strong> HEALTHY# does not require precharging.</td>
<td></td>
</tr>
<tr>
<td>100K to VIO</td>
<td>S_GNT#</td>
</tr>
<tr>
<td>50K or 51K to Vf (1V Reference Voltage)</td>
<td>S_ACK64#, S_AD[63:0], S_CBE[7:0]#, S_DEVSEL#, S_FRAME#, S_IDSEL, S_IRDY#, S_LOCK#, S_PAR, S_PAR64, S_PERR#, S_REQ64#, S_SERR#, S_STOP#, S_TRDY#</td>
</tr>
</tbody>
</table>

In this sample, PCI 6540 Hot Swap application, the Rp 50K- or 51K-Ohm precharge resistors, of the sample cPCI 6540 Hot Swap design, are used and remain connected with an active Vf power source (1V). The PCI signal leakage remains within the tolerable high-level leakage current of Ileak (+55 ΜA) on the PCI Bus I/Os when the backend power stabilizes, and the PCI Bus is ready for normal bus operation while BD_SEL# and HEALTHY# are actively asserted. In the sample cPCI 6540 Hot Swap Board application, the PCI 6540 secondary PCI interface is configured to interface with the cPCI backplane. The secondary PCI signals listed in Table 3 must be coupled with the precharge resistors specified in PICMG 2.1, R2.0.

1.4 Hot Swap Control Logic

The sample Hot Swap application uses the LTC1643L-1 Hot Swap Controller (designed by Linear Technology, for hot swapping cPCI boards). The +3.3V, +5V, +12V, and -12V inputs to the LTC1643L are derived from medium-length Power pins. The LONG_3.3V, 5V, and VIO pins are utilized to provide power to the pull-up resistors, Bus Precharge circuits, PCI 6540 PCI-X-to-PCI-X Bridge device, and LOCAL_PCI_RESET# logic circuitry. The cPCI backplane BD_SEL# signal is connected to the LTC1643L Hot Swap Controller ON# pin. The LTC1643L Hot Swap Controller PWRGD# pin is connected to the backplane HEALTHY# signal.
The PCI Bus $\text{VP}$ (1V reference voltage) is generated to 1V reference voltage. The $\text{VP}$ 1.0V ($\pm$20%) reference precharge voltage is required to power the precharge circuits. When the cPCI board is ready for normal operation, the on-board precharge voltage source must be used to bring the network to the required precharge voltage.

For further details regarding required conditions for $\text{VPSOURCE}$ and $\text{VP}$ selection, as well as precharge resistor disconnection on PCI 6540 PCI Bus signals during normal operation, refer to PICMG 2.1, R2.0, Sections 3.1.3.1 and 3.1.3.3.

2 Hardware Connection Control

2.1 Hot Swap Board Slot Control

To control the Board Insertion and Extraction processes, the Hot Swap Platform (cPCI backplane) must be equipped with Hardware Connection Control. To ensure completion of the signal connection process, BD_SEL# is utilized in sensing the presence of connection when all other signals reliably make contact with the cPCI backplane. The shortest Hot Swap Interface pin is the last to mate during Insertion and the first to disengage during Extraction. For a cPCI system not implementing Hot Swap Control logic, BD_SEL# is grounded on the backplane.

BD_SEL# is driven low by the cPCI backplane Hot Swap Controller to enable the powering sequence and Hardware Connection states after the controller detects the presence of a Hot Swap board.

During Insertion, the cPCI backplane Hot Swap Controller controls backend power ramping by asserting BD_SEL# to bring the state of Insertion from P1/H0 (Physical Connection State 1, transitioning to the Hardware Connection where the board is fully seated, but not powered, and not active on the PCI Bus) to H1 (Hardware Connection State 1, where the board is powered up and sufficiently initialized to connect to the PCI Bus). When BD_SEL# mates with the cPCI backplane, the Physical Connection process is complete. BD_SEL# is continuously asserted until backend power gradually disengages. During Extraction, the BD_SEL# pin detaches from the cPCI backplane connector, the PCI 6540 immediately transitions to the H0 state (powered off), and the software device driver is in the S0 state (driver enters into a quiescent state).

2.2 CompactPCI Platform Reset

The PCI Bus resets when PCI_RST# (a bused signal driven by the system host) is active during power-on. The cPCI system platform may implement PCI_RST# as a radial signal from the system platform Hot Swap Controller to facilitate the Hardware Connection process between the Hot Swap board and system platform. The cPCI Hot Swap board must remain in reset until HEALTHY# is asserted, indicating the board is suitable to be released from reset—the board power status has reached Power Good and then allowed onto the PCI Bus. On the cPCI 6540 Hot Swap board, the reset (LOCAL_PCI_RST#) is generated by routing S_RST# through an inverter, and then combined with the Hot Swap Controller PWRGD# signal through a NOR gate. Figure 3 illustrates S_RST# and PWRGD# wired to generate the Hot Swap Board LOCAL_PCI_RST# signal.

LOCAL_PCI_RST# feeds into the PCI 6540 (normally by way of the PCI Reset Input pin) to reset the PCI 6540, which generates the Reset signal to reset the primary and secondary PCI Buses. LOCAL_PCI_RST# remains asserted until HEALTHY# is asserted (value of 1). If HEALTHY# de-asserts during this process, LOCAL_PCI_RST# is immediately asserted.

LOCAL_PCI_RST# remains asserted throughout the Physical Connection process. The PCI 6540 asynchronously three-states most of the primary and secondary PCI Bus signals, while LOCAL_PCI_RST# is asserted.

During Insertion, the cPCI backplane Hot Swap Controller controls backend power ramping by asserting BD_SEL# to bring the state of Insertion from P1/H0 (Physical Connection State 1, transitioning to the Hardware Connection where the board is fully seated, but not powered, and not active on the PCI Bus) to H1 (Hardware Connection State 1, where the board is powered up and sufficiently initialized to connect to the PCI Bus). When BD_SEL# mates with the cPCI backplane, the Physical Connection process is complete. BD_SEL# is continuously asserted until backend power gradually disengages. During Extraction, the BD_SEL# pin detaches from the cPCI backplane connector, the PCI 6540 immediately transitions to the H0 state (powered off), and the software device driver is in the S0 state (driver enters into a quiescent state).

Figure 3. cPCI 6540 Hot Swap Board S_RST# and PWRGD# Wiring

To protect the PCI board connected to the cPCI 6540RDK board from Early Power during Insertion and Extraction, the PCI 6540 places all PCI Interface signals in a high-impedance state when the Reset signal is asserted.
2.3 HEALTHY# during Insertion and Extraction States

HEALTHY# (a radial signal) is utilized to indicate board readiness to be released from reset and connect to the PCI Bus. The HEALTHY# signal is generated from the on-board Hot Swap Control logic if board power is reached (PWRGD=1), indicating to the system host that the board power state is healthy and the board is ready to be released from reset.

HEALTHY# is an Open Drain pin (IOL=4 mA). During Insertion, do not actively drive HEALTHY# if backend power is not within the required tolerance (±5%, per PICMG 2.1, R2.0). After backend power is stabilized, HEALTHY# is asserted with BD_SEL# prior assertion, to indicate that the H1 state is reached (board is powered up and sufficiently initialized to connect to the PCI Bus).

In the sample cPCI 6540 Hot Swap design, the cPCI backplane HEALTHY# pin is connected to the Hot Swap Controller PWRGD# signal. The S_RST# and PWRGD# signals, by way of an inverter and NOR gate, are combined to generate LOCAL_PCI_RST#. When LOCAL_PCI_RST# is active, it causes the PCI 6540 to three-state the output pins (in High Impedance mode) during precharge. During Extraction, HEALTHY# is de-asserted when the Power pins begin to disengage from the cPCI Bus connector.

2.4 Ejector Switch

The ejector switch is used to signal cPCI Hot Swap board Insertion or impending Extraction. During Insertion, the switch is closed, causing the INS bit to be set. ENUM# is then asserted to the system host to indicate that a board has been freshly inserted or is about to be extracted. After the board is fully seated, and the PCI 6540 is visible to the system with the LED turned OFF, the Hot Swap software must clear the INS bit to de-assert ENUM#. As a result, the EXT bit is set, indicating that Insertion is permitted.

During Extraction, the switch is opened from a closed position, which sets the EXT bit to 1. When the EXT bit is set to 1, ENUM# is asserted to the system host, indicating that the board is about to be extracted. After the system host acknowledges ENUM# for the Extraction process, the system Hot Swap software must clear the EXT bit to de-assert ENUM#. As a result, the INS bit is set, indicating that Insertion is permitted.

2.5 Hot Swap Control and Status Bits

The INS and EXT bits are also used by Hot Swap software to monitor ENUM# assertion status. The INS bit is set to indicate the board has been inserted. The EXT bit is set to indicate the board is about to be extracted. Both bits are utilized to acknowledge receiving ENUM# notification and de-assertion.

The EIM and LOO control bits are used to further support the Hot Swap process. EIM (ENUM# Mask Status, HS_CSR[1]) can be set to 1 to enable ENUM# assertion, or 0 to mask ENUM# assertion. The LOO bit controls whether the LED is ON or OFF.

With PI=1 compliancy, the PCI 6540 is equipped with two additional bits—PIE (Pending Insertion/Extraction) and DHA (Device Hiding Arm) (HS_CSR[2, 0], respectively). The PIE status bit tracks board Insertion and Extraction progress. Without PIE status bit support, the Hot Swap software may be unable to monitor the Ejector Switch state from the previous reset. The DHA status bit determines whether Device Hiding is invoked to allow complete software disconnection and authorized for the Extraction process to be invisible on the cPCI Bus, thereby avoiding the potential jeopardy of a PCI transaction being underway during Extraction.

2.6 LED Function

During Insertion, the PCI 6540 turns ON the L_STAT signal (LED ON) when Reset is asserted and L_STAT remains ON until ejector switch is closed.

The PCI 6540 implements the LED as a PI=1 time sequence. During the Extraction process, the LED remains OFF until it is turned ON by the software device driver, which sets the LOO bit to 1, indicating that the software device driver is quiescent and that Extraction is permitted.
2.7 Implementing Device Hiding

The PCI 6540 Device Hiding Arm (DHA) bit determines whether device hiding is enabled. Device hiding allows a board that is software disconnected and authorized for Extraction to be invisible on the cPCI Bus, thereby avoiding jeopardy to the system if a PCI transaction is in progress during Extraction. During Insertion, device hiding is enabled with the DHA bit set to 1, arming device hiding when LOCAL_PCI_RST# is de-asserted.

When the ejector switch is closed, the INS bit is set to 1 and the DHA bit is cleared, disarming device hiding. During Extraction, the PCI 6540 remains visible to the system host until the LED is ON with the LOO bit set to 1. When the ejector switch is open, the PCI 6540 goes into Device Hiding mode with the DHA bit set to 1.

2.8 Interrupt Routing

As a PCI-X-to-PCI-X Bridge device, the PCI 6540 is not equipped with PCI Interrupt pins in Transparent mode. In Transparent mode, the secondary INT[D:A]# signals are not connected through the PCI 6540. The INT[D:A]# signals are connected directly from the secondary bus to the primary bus. In Non-Transparent mode; however, the PCI 6540 is equipped with primary and secondary Interrupt pins, P_INTA# and S_INTA#, respectively. The PCI 6540 Non-Transparent Interrupt pins are connected based on the Interrupt Device Binding Rule and IDSEL AD Line Mapping, as mandated by the PCI-to-PCI Bridge Architecture Specification, r1.2, Chapter 9, Section 9.1. (Refer also to Appendix A, “PCI-to-PCI Bridge Interrupt Routing Application Note.”) In the sample cPCI 6540 Hot Swap design, the Interrupt circuitry is externally routed through the CPLD logic, which automatically enables the P_INTA# and S_INTA# signals when the cPCI 6540 board is configured in Non-Transparent mode and plugged into the system slot. For further details regarding the Interrupt circuitry layout, refer to page 7 of the cPCI 6540 Hot Swap Reference Schematics in Section 5.

2.9 Clock Routing

In Transparent mode, place the cPCI 6540 Hot Swap board into the system slot of the cPCI backplane, with the PCI 6540 secondary bus interface connected to the backplane and primary bus connected to the host CPU board. The primary bus clock frequency is supplied to the PCI 6540 by the host CPU board connected to the primary bus interface. The PCI 6540 is equipped with an internal secondary clock buffer that provides the S_CLKO[4:0] clock outputs. However, S_CLKO[4:0] cannot be utilized due to skew and slew-rate issues; therefore, an external clock buffer/distributor is utilized to support the PCI 6540 secondary bus interface clock frequency and PCI devices in the peripheral slots.

In the sample cPCI 6540 Hot Swap design, the secondary bus frequencies are provided by the external clock distributor. The clock buffer/distributor can be turned ON by the clock multiplier CLK_EN# pin, which is controlled by the CPLD. The clock distributor provides the clock frequencies to the PCI 6540 and secondary PCI devices by way of the S_CLKIN pin. The secondary bus interface clock trace routing connected to the backplane must comply with the Clock Routing Design rules mandated in the PICMG 2.0, R3.0, CompactPCI Specification (PICMG 2.0, R3.0). The following lists board clock-routing requirements:

- Total signal length for the cPCI Hot Swap board 32- or 64-bit signals (J1 and J2 cPCI Connectors) to be less than or equal to 63.5 mm (2.5 inches) from the connector pin to the PCI device.
- cPCI Hot Swap board PCI clock trace length to be 63.5 mm ±10.16 mm (2.5 inches ±0.4 inches) from the PCI device to the cPCI Edge Connector pin.
- Connect secondary clock outputs point-to-point from the clock distributor, and limit to no more than one PCI load.
- Secondary PCI Clock output clock traces must have equal length and impedance to the PCI 6540 and secondary PCI devices.
- Terminate or disable unused secondary clock outputs to reduce power dissipation and system noise.

In Non-Transparent mode, place the cPCI 6540 Hot Swap board into the cPCI backplane peripheral slot, with the secondary bus interface connected to the backplane. The cPCI backplane system host (SBC—Single Board Computer) provides the clock frequencies to all peripheral PCI devices, including the PCI 6540 secondary bus interface. The CPLD is programmed to disable the clock multiplier by way of the CLK_EN# pin to allow the SBC board to provide...
the clock frequency to the PCI 6540 secondary bus interface and other peripheral PCI devices. A detailed layout of the sample Secondary Clock routing is provided on page 6 of the cPCI 6540 Hot Swap Reference Schematics in Section 5. The Secondary Clock Trace layout closely adheres to PICMG 2.0 R3.0 requirements. Figure 4 illustrates the use of an external clock buffer and clock multiplier to provide secondary clock frequencies on the sample cPCI 6540 Hot Swap reference design.

Figure 4. Secondary Bus Interface Sample Clock Routing

3 Assumptions

The sample cPCI 6540 Hot Swap design provides useful information for Hot Swap applications using the PCI 6540. For additional PCI 6540 information, refer to the PCI 6540CB Data Book, Version 2.01, published May, 2004. The sample cPCI 6540 Hot Swap design components (such as boot and code memory, serial EEPROM, and pull-up- and pull down resistors) are not discussed in this application note. Designers are expected to add these components, as needed.
4 References

The following is a list of documentation to provide further details.

- **PCI 6540CB Data Book, Version 2.01, May, 2004**
  PLX Technology, Inc.
  870 Maude Avenue, Sunnyvale, CA 94085 USA
  Tel: 408 774-9060 or 800 759-3735, Fax: 408 774-2169, http://www.plxtech.com

- **PCI Local Bus Specifications, Revisions 2.3 and 3.0**
  PCI Special Interest Group (PCI-SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com/home

- **PCI-X Addendum to PCI Local Bus Specification, Revision 1.0b**
  PCI Special Interest Group (PCI-SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com/home

- **PCI to PCI Bridge Architecture Specification, Revision 1.2, June 9, 2003**
  PCI Special Interest Group (PCI-SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com/home

- **LTC1643L/LTC1643L-1/LTC1643H, PCI-Bus Hot Swap Controller Data Sheet**
  Linear Technology Corporation
  1630 McCarthy Boulevard, Milpitas, CA 95035-7417 USA
  Tel: 408-432-1900, Fax: 408-434-0507, http://www.linear.com

- **PICMG 2.0, R3.0, CompactPCI Specification, October 1, 1999**
  PCI Industrial Computer Manufacturers Group (PICMG)
  c/o Virtual Inc., 401 Edgewater Place, Suite 600, Wakefield, MA 01880 USA
  Tel: 781 246-9318, Fax: 781 224-1239, http://www.picmg.org

- **PICMG 2.1, R2.0, CompactPCI Hot Swap Specification, January 2001**
  PCI Industrial Computer Manufacturers Group (PICMG)
  c/o Virtual Inc., 401 Edgewater Place, Suite 600, Wakefield, MA 01880 USA
  Tel: 781 246-9318, Fax: 781 224-1239, http://www.picmg.org
5 Schematics
A PCI-to-PCI Bridge Interrupt Routing Application Note

A.1 IDSEL and INT[D:A]# Mapping

PCI to PCI Bridge Architecture Specification, r1.2 specifies that the system BIOS assumes an association between device location and which INT[D:A]# line it uses when requesting an interrupt. PLX PCI-to-PCI bridges do not route interrupts through the chip. For devices on the secondary bus, use the following tables for IDSEL and INT[D:A]# mapping.

Table A.1. IDSEL Connection

<table>
<thead>
<tr>
<th>Secondary Bus Device Number</th>
<th>IDSEL S_AD Line Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>S_AD16</td>
</tr>
<tr>
<td>1</td>
<td>S_AD17</td>
</tr>
<tr>
<td>2</td>
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</tr>
<tr>
<td>9</td>
<td>S_AD25</td>
</tr>
<tr>
<td>10</td>
<td>S_AD26</td>
</tr>
<tr>
<td>11</td>
<td>S_AD27</td>
</tr>
<tr>
<td>12</td>
<td>S_AD28</td>
</tr>
<tr>
<td>13</td>
<td>S_AD29</td>
</tr>
<tr>
<td>14</td>
<td>S_AD30</td>
</tr>
<tr>
<td>15</td>
<td>S_AD31</td>
</tr>
</tbody>
</table>

Note: Some systems may be unable to handle IDSEL in the lower or upper Address bits. It is recommended to use S_AD[27:20] for IDSEL on secondary PCI devices.

Table A.2. Interrupt-Device Number Binding

<table>
<thead>
<tr>
<th>IDSEL S_AD Line Assignment</th>
<th>Interrupt Pin on Device</th>
<th>Interrupt Pin on Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_AD[16, 20, 24, 28]</td>
<td>INTA#</td>
<td>INTA#</td>
</tr>
<tr>
<td></td>
<td>INTB#</td>
<td>INTB#</td>
</tr>
<tr>
<td></td>
<td>INTC#</td>
<td>INTC#</td>
</tr>
<tr>
<td></td>
<td>INTD#</td>
<td>INTD#</td>
</tr>
<tr>
<td>S_AD[17, 21, 25, 29]</td>
<td>INTA#</td>
<td>INTB#</td>
</tr>
<tr>
<td></td>
<td>INTC#</td>
<td>INTD#</td>
</tr>
<tr>
<td></td>
<td>INTD#</td>
<td>INTA#</td>
</tr>
<tr>
<td>S_AD[18, 22, 26, 30]</td>
<td>INTA#</td>
<td>INTC#</td>
</tr>
<tr>
<td></td>
<td>INTB#</td>
<td>INTD#</td>
</tr>
<tr>
<td></td>
<td>INTC#</td>
<td>INTA#</td>
</tr>
<tr>
<td></td>
<td>INTD#</td>
<td>INTB#</td>
</tr>
<tr>
<td>S_AD[19, 23, 27, 31]</td>
<td>INTA#</td>
<td>INTD#</td>
</tr>
<tr>
<td></td>
<td>INTB#</td>
<td>INTA#</td>
</tr>
<tr>
<td></td>
<td>INTC#</td>
<td>INTB#</td>
</tr>
<tr>
<td></td>
<td>INTD#</td>
<td>INTC#</td>
</tr>
</tbody>
</table>

A.2 Add-In Board Interrupt Pin Usage for PCI Devices behind PCI-to-PCI Bridge

For Add-In boards with multiple PCI devices behind PCI-to-PCI bridges, the S_ADx signal used for IDSEL by the secondary PCI device dictates the corresponding interrupt pin of that secondary PCI device. The INTx# and S_ADx IDSEL relationship is dictated by the first row of the “Interrupt pin on connector” column in Table A-2. For example, if S_AD23 is used for a secondary PCI device, use INTD# for that PCI device. The number of PCI-to-PCI bridges used is irrelevant.