High Speed Deserialization Board (HSDB)

HSC-ADC-FPGA

FEATURES
Used with buffer memory board for capturing and converting high speed serial LVDS digital data to parallel CMOS logic levels
Used with high speed ADC evaluation boards that have serial LVDS outputs
Features Xilinx® XC2V250-5FG256C FPGA, Virtex-II FPGA
Can switch up to four channels of output data (two at a time)
Easily configurable, supporting 8-bit to 14-bit ADCs
Allows standard JTAG user connection for additional code modifications

EQUIPMENT NEEDED
Any high speed ADC evaluation board that supports serial LVDS digital output format
HSC-ADC-EVALA/B-DC, ADI data capture FIFO board

GENERAL DESCRIPTION
The high speed deserialization board (HSDB) captures up to four channels of serial LVDS digital outputs and converts the outputs to standard parallel CMOS format. It supports quad analog-to-digital converter (ADC) evaluation boards, enabling the user to connect to the Analog Devices FIFO board (HSC-ADC-EVALA/B-DC). Together, these boards can be connected to a PC through a USB port and used with the ADC Analyzer™ to evaluate the performance of high speed quad ADCs. Users can view both time and frequency information for a specific analog input and encode rate and analyze SNR, SINAD, SFDR, and harmonic information.

The evaluation kit, which includes a wall-mount switching power supply, is easy to set up. Additional equipment required: an Analog Devices high speed quad ADC evaluation board, dual-channel FIFO board, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

The HSC-ADC-FPGA supports up to four ADC channels, providing two parallel CMOS outputs simultaneously.

PRODUCT HIGHLIGHTS
1. Easy to set up.
   - Connect the power supply and signal sources to the two evaluation boards. Then connect to the PC and evaluate the performance instantly.
2. JTAG user interface.
   - With the supplied JTAG connection, users can implement unique features in the FPGA.
3. Up to 840 MBPS available on each channel.
   - 14-bit quad ADCs with encode rates as high as 60 MSPS can be used with the deserialization board.
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# REVISION HISTORY

11/05—Rev. A to Rev. B
Changed HSC-ADC-EVALA-DC to HSC-ADC-EVALA/B-DC Universal
Changes to Figure 1 ......................................................................................... 1
Changes to Table 1 ............................................................................................ 4
Changes to the Theory of Operation Section and Figure 3 .............. 5
Added the SPI Interface Section ................................................................. 7
Changes to Figure 5 ......................................................................................... 8
Changes to Figure 6 ......................................................................................... 9
Updated Schematic and Layout to Rev D ....................................................... 9-17
Changes to Table 6 .......................................................................................... 17
Changes to Ordering Guide ......................................................................... 20

02/05—Rev. 0 to Rev. A
Updated Bill of Materials ............................................................................. 15
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10/04—Revision 0: Initial Version
HSDB QUICK START

The HSDB is used to create an interface from a quad ADC evaluation board that has serial LVDS outputs to the FIFO data capture board.

REQUIREMENTS

The following equipment is needed to set up the HSDB:

- FIFO evaluation board, ADC Analyzer, USB cable, and FIFO data sheet
- High speed ADC evaluation board and ADC data sheet
- Power supply for ADC evaluation board, HSDB, and FIFO
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically <1 ps rms
- PC with Windows® 98 (2nd edition), Windows 2000, Windows ME, or Windows XP for the ADC Analyzer
- PC with a USB 2.0 port recommended for FIFO connection

ADDITIONAL INFORMATION AND UPDATES

For more information on the ADC Analyzer and the FIFO data capture board, and for software updates, visit www.analog.com/FIFO.

For more information on LVDS data output, see the LVDS Data Outputs for High Speed Analog-to-Digital Converters Application Note (AN-586) on www.analog.com.

QUICK START STEPS

Connect the quad ADC evaluation board to the high speed backplane connector side of the HSDB. Then connect the other side of the HSDB to the 120-pin connector header that mates to the FIFO board.

1. Connect the USB cable to the FIFO evaluation board and to a USB port on the PC.
2. Set the FIFO jumper settings in dual-channel configuration as shown in the HSC-ADC-EVALA/B-DC datasheet, located at www.analog.com/FIFO.
3. Verify and connect the appropriate power supplies to the FIFO, HSDB, and ADC evaluation boards.
4. Apply power to the evaluation boards and check the voltage levels at the board level. Separate supplies may be necessary.
5. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal.
6. Start the ADC Analyzer to begin the evaluation.
SUPPORTED ADC EVALUATION BOARDS

The evaluation boards in Table 1 can be used with the high speed ADC deserialization board.

Table 1. Supported ADC Evaluation Boards

<table>
<thead>
<tr>
<th>Evaluation Board Model</th>
<th>Description of ADC</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9289-65EB</td>
<td>8-bit, 65 MSPS quad ADC</td>
<td>Requires HSC-ADC-FPGA-9289 and HSC-ADC-EVALA/B-DC (dual-channel)</td>
</tr>
<tr>
<td>AD9229-65EB</td>
<td>12-bit, 65 MSPS quad ADC</td>
<td>Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)</td>
</tr>
<tr>
<td>AD9287-100EB</td>
<td>8-bit, 100 MSPS quad ADC</td>
<td>Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)</td>
</tr>
<tr>
<td>AD9219-65EB</td>
<td>10-bit, 65 MSPS quad ADC</td>
<td>Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)</td>
</tr>
<tr>
<td>AD9228-65EB</td>
<td>12-bit, 65 MSPS quad ADC</td>
<td>Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)</td>
</tr>
<tr>
<td>AD9259-50EB</td>
<td>14-bit, 50 MSPS quad ADC</td>
<td>Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)</td>
</tr>
</tbody>
</table>
THEORY OF OPERATION

The HSDB, featuring the Xilinx Virtex™ II FPGA, accepts four ADC channels of LVDS serial data and the data output and frame align clocks (DCO and FCO). The FPGA then converts all of these signals from LVDS to single-ended CMOS signals.

The HSDB can support 8-bit to 14-bit ADCs. The DCO signal is used to clock the incoming data through 14 shift registers. Seven of these registers are clocked on the rising edge of DCO, and the other seven are clocked on the falling edge (DDR), as shown in Figure 3. The ADC resolution is selectable using Jumper Connection JP101 and Jumper Connection JP102.

Both the DCO and FCO are used inside the FPGA to set up all necessary clock edges to take the parallel data from the shift registers to the output of the FPGA. The DLL/Timing Reset button (PB101) is used to set the data capture timing to the default setting (see Table 4).

Once the parallel data has been transferred completely to the FCO clock domain, the data is multiplexed for use with the 2-channel FIFO board (HSC-ADC-EVALA/B-DC). ADC Channel A and Channel B are selected using the JP104 jumper connection. Channel C and Channel D are selected using the JP103 jumper connection. Data clock outputs (CLK_AB and CLK_CD) are also provided to clock the FIFO board.

CODE DESCRIPTION

The FPGA on the HSDB comes with Verilog code preinstalled and tested. It is designed to help evaluate the performance of an Analog Devices quad ADC quickly and easily by providing the user with familiar CMOS logic-level outputs.

MANUAL INSTALLATION AND CUSTOMIZATION

Users can manually customize or update the necessary code through a JTAG connector provided on the deserialization board, as shown in Figure 2. However, Analog Devices provides no guarantee of performance if the code is customized.

A Zip file containing all of the necessary default configuration files to implement manual changes or to add custom module blocks for further computation is at www.analog.com/FIFO.

Figure 3. Internal FPGA Functional Block Diagram
JUMPERS

RESOLUTION SETTINGS

The HSDB supports ADCs with 8 bits to 14 bits of resolution. Use Table 2 to configure the appropriate jumpers. In Table 2, 0 indicates an open jumper, and 1 indicates a shorted jumper.

Table 2. Resolution Jumper Settings

<table>
<thead>
<tr>
<th>Number of Bits</th>
<th>JP101</th>
<th>JP102</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

CHANNEL SELECTION SETTINGS

The ADC Channel A and Channel B are associated with the top IDT FIFO chip, the one closest to the Analog Devices logo; Channel C; or ADC Analyzer Channel B. ADC Channel C and Channel D are associated with the bottom IDT FIFO chip, Channel A, or ADC Analyzer Channel A. Use Table 3 to configure the jumper settings for channel selection. In Table 3, 0 indicates an open jumper, and 1 indicates a shorted jumper.

Table 3. Channel Selection Jumper Settings

<table>
<thead>
<tr>
<th>ADC Channel</th>
<th>FIFO Channel/ADC Analyzer Channel</th>
<th>Channel Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Channel B/Channel B</td>
<td>JP104 = 0</td>
</tr>
<tr>
<td>B</td>
<td>Channel B/Channel B</td>
<td>JP104 = 1</td>
</tr>
<tr>
<td>C</td>
<td>Channel A/Channel A</td>
<td>JP103 = 0</td>
</tr>
<tr>
<td>D</td>
<td>Channel A/Channel A</td>
<td>JP103 = 1</td>
</tr>
</tbody>
</table>

DATA ALIGNMENT

The DLL/Timing Reset button (PB101) must be pressed to operate the HSDB after initial power-up. Data alignment is automatic; however, the DLL/Timing Reset button must be pressed any time the ADC sample clock rate is changed, or data outputs become corrupted.

After pressing the DLL/Timing Reset button, the FPGA digital clock manager (DCM) DLL is reset to its default setting. This value (PHASE_SHIFT) is defined in the user constraints file of the FPGA software and is shown in Table 4.

Table 4. Default PHASE_SHIFT User Constraint Settings

<table>
<thead>
<tr>
<th>Product</th>
<th>PHASE_SHIFT User Constraint</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9289</td>
<td>+50</td>
</tr>
<tr>
<td>AD9229</td>
<td>−10</td>
</tr>
<tr>
<td>AD9219/AD9228/AD9259/AD9287</td>
<td>−10</td>
</tr>
</tbody>
</table>

DCO PHASE ALIGNMENT

The DCO Phase Shift button (PB100) can be used in conjunction with the DCO Phase Shift jumper (JP100) to adjust the phase relationship between the incoming DCO signal and the FPGA DLL signal.

The output of the FPGA DLL is used to capture the incoming serial data streams. The rising edge and falling edge of this signal must be aligned, so that they occur during the center of the data eye as shown in Figure 4.

After activating the DLL/Timing Reset button (PB101), the phase of the DLL is set to its default value. If this phase alignment setting is not compatible with the current configuration of the ADC under test, it can be adjusted.

The phase shift operation is activated by pressing the DLL Phase Shift button (PB100). The direction of this adjustment is determined by the setting of the DLL Phase Shift jumper (JP100); see Table 5.

Table 5. DCO Phase Shift Alignment Settings

<table>
<thead>
<tr>
<th>DCO Phase Shift</th>
<th>JP100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increment</td>
<td>0</td>
</tr>
<tr>
<td>Decrement</td>
<td>1</td>
</tr>
</tbody>
</table>

While the DLL Phase Shift button is clicked, the phase is adjusted continuously over the range of the PHASE_SHIFT user constraint. The PHASE_SHIFT variable can be set to any integer value between ±255. The actual setting of this variable is lost when using this function. However, an out-of-range condition is indicated by LED CR100. If the phase has gone out of range, it can be set back in range either by using the DLL/Timing Reset button (PB101) or by changing the adjustment direction using Jumper JP100 and clicking the PB100 button again.

The rate of phase change while the PB100 button is clicked is determined by multiplying the FCO clock period by $2^{27}$ (256 steps × $2^{19}$). This gives the amount of time in seconds that it takes to slew from PHASE_SHIFT = 0 to the minimum or maximum value. For example, if FCO = 65 MHz, it takes approximately 2 sec to slew from PHASE_SHIFT = 0 to out-of-range ($2^{27} \times 1/65M$). Refer to the Xilinx Virtex-II datasheet for further details on DCM phase shifting.
**SPI® INTERFACE**

The HSDB fully supports ADCs that have an SPI interface. The HSDB does not interact with any of the SPI signals; it provides a path for the SPI interface to be connected from the HSC-ADC-EVALB-DC data capture board to the corresponding product evaluation board.

**FIFO JUMPER SETTINGS**

The HSDB requires the interface of the HSC-ADC-EVALA/B-DC (dual-channel FIFO4 or FIFO4.1) for data to be captured and displayed in the ADC Analyzer. The default settings for the FIFO dual-channel configuration can be found in the HSC-ADC-EVALA/B-DC datasheet at www.analog.com/FIFO. To align the timing properly, some evaluation boards require modifications to these settings. For proper operation, the FIFO timing setting should be configured for dual-channel configuration. For more details, see the Theory of Operation section in the HSC-ADC-EVALA/B-SC/HSC-ADC-EVALA/B-DC data sheet at www.analog.com/FIFO.

Another easy way to determine if the proper jumper settings between the HSDB, FIFO, and ADC Analyzer have already been installed is to consult the help menu in the ADC Analyzer software:

1. From the Help menu, select **About HSC_ADC_EVALA**.
2. Click **Setup Default Jumper Wizard**.
3. Click **Dual Channel**. A picture of the FIFO board for that application appears, showing the correct jumper settings already in place.
EVALUATION BOARD

The HSDB (HSC-ADC-FPGA, Rev. D) provides all of the support circuitry required to accept quad ADC digital serial LVDS outputs. Each of the various functions and configurations can be selected by proper connection of various jumpers (see Figure 6 to Figure 8). When using this in conjunction with an ADC evaluation board and FIFO, it is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 6 to Figure 8 for complete schematics and layout plots.

POWER SUPPLIES

The HSDB board is supplied with a wall mount switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 to 240 ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J300. On the PC board, the 6 V supply is then fused and conditioned before connecting to two low dropout linear regulators that supply the proper bias to each of the various sections on the board (see Figure 5).

When operating the evaluation board in a nondefault condition, L302 and L303 can be removed to disconnect the switching power supply. This enables the user to individually bias each section of the board. Use P301 to connect a different supply for each section. The 3.3 V supply is needed with a 1 A current capability to bias the FPGAs I/O supply ring pins. The 1.5 V supply will also be needed in addition to the other 3.3 V supply to bias the FPGAs core supply pins. The 1.5 V supply should have a 1 A current capability, as well.
HSDB SCHEMATICS AND PCB LAYOUT

Figure 6. PCB Schematic
Figure 7. PCB Schematic (Continued)
POWER SUPPLY INPUT
6V
2A MAX

DECOUPLING CAPACITORS

Figure 8. PCB Schematic (Continued)
Figure 9. Layer 1—Primary Side (Top)
Figure 10. Layer 2—Ground Plane
Figure 11. Layer 3—+1.5 V Power Plane and Signal
Figure 12. Layer 4—+3.3V Power Plane and Signal
Figure 13. Layer 5—Ground Plane
Figure 14. Layer 6—Secondary Side (Bottom)
### ORDERING INFORMATION

#### BILL OF MATERIALS

**Table 6.**

<table>
<thead>
<tr>
<th>Item</th>
<th>QTY</th>
<th>REFDES</th>
<th>Device</th>
<th>Package</th>
<th>Value</th>
<th>Manufacturer and Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>HSC-ADC-FPGA</td>
<td>PCB</td>
<td>PCB</td>
<td>REV D</td>
<td>Panasonic, ECJ-0EB1A104K</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td>C309, C310, C311, C312, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327</td>
<td>Capacitor</td>
<td>402</td>
<td>0.1 μF, ceramic, X5R, 10 V, 10% tolerance</td>
<td>AVX, 08056D106KAT2A</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>C305, C307</td>
<td>Capacitor</td>
<td>805</td>
<td>10 μF, 6.3 V ±10%, ceramic, X5R</td>
<td>Kemet, C0603C104K4RACTU</td>
</tr>
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<td>4</td>
<td>2</td>
<td>C306, C308</td>
<td>Capacitor</td>
<td>603</td>
<td>0.1 μF, ceramic, X7R, 16 V, 10% tolerance</td>
<td>Kemet, C0402C102K3RACTU</td>
</tr>
<tr>
<td>5</td>
<td>15</td>
<td>C313, C314, C315, C316, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338</td>
<td>Capacitor</td>
<td>402</td>
<td>1 nF, ceramic, X7R, 25 V, 10% tolerance</td>
<td>Panasonic, ECJ-0EB1A104K</td>
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<td>6</td>
<td>1</td>
<td>C300</td>
<td>Capacitor</td>
<td>1206</td>
<td>10 μF, tantalum, 16 V, 10% tolerance</td>
<td>Panasonic, ECJ-0EB1A104K</td>
</tr>
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<td>7</td>
<td>4</td>
<td>C301, C302, C303, C304</td>
<td>Capacitor</td>
<td>603</td>
<td>1 μF, ceramic, X5R, 6.3 V, 10% tolerance</td>
<td>Panasonic, ECJ-0EB1A104K</td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>CR100, CR200, CR300</td>
<td>LED</td>
<td>SMT</td>
<td>Green, 4 V, 5 m candela</td>
<td>Panasonic, LN314G8TRA</td>
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<td>9</td>
<td>1</td>
<td>D301</td>
<td>Diode</td>
<td>DO-214AB</td>
<td>30 V, 3 A, SMC</td>
<td>Micro Commercial Co., SK33MSCT</td>
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<tr>
<td>10</td>
<td>1</td>
<td>D300</td>
<td>Diode</td>
<td>DO-214AA</td>
<td>50 V, 2 A, SMC</td>
<td>Micro Commercial Co., S2A</td>
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<tr>
<td>11</td>
<td>1</td>
<td>F300</td>
<td>Fuse</td>
<td>1210</td>
<td>6.0 V, 2.2 A trip current resettable fuse</td>
<td>Tyco/Raychem, NANOSMDC110F-2</td>
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<td>12</td>
<td>1</td>
<td>FER300</td>
<td>Ferrite bead</td>
<td>2020</td>
<td>10 μH, 5 A, 50 V, 100 MHz</td>
<td>Murata, DLWSM1919S2L</td>
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<tr>
<td>13</td>
<td>1</td>
<td>J200</td>
<td>Connector</td>
<td>HEADER</td>
<td>TSW-140-08-G-T-RA, 120-pin header assembly</td>
<td>Samtec, TSW-140-08-G-T-RA</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>J201</td>
<td>Connector</td>
<td>HEADER</td>
<td>87832-1420, 14-pin dual ROM shrouded header</td>
<td>Molex, 87832-1420</td>
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<tr>
<td>15</td>
<td>1</td>
<td>J300</td>
<td>Connector</td>
<td>0.1&quot;, PCMT</td>
<td>RAPC722, power supply connector</td>
<td>Switchcraft, SC1153</td>
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<tr>
<td>17</td>
<td>4</td>
<td>L300, L301, L302, L303</td>
<td>Ferrite bead</td>
<td>1210</td>
<td>10 μH, BEAD CORE</td>
<td>Panasonic, EXC-CL3225U1</td>
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<tr>
<td>18</td>
<td>1</td>
<td>P200</td>
<td>Connector</td>
<td>HEADER</td>
<td>1469028-1, right angle 2 pair, 25 mm, header assembly</td>
<td>Tyco, 1469028-1</td>
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<td>19</td>
<td>2</td>
<td>PB100, PB101</td>
<td>Switch</td>
<td>SMT</td>
<td>SPST, 20 mA, push-button switch</td>
<td>Panasonic, EVQ-PHP03T</td>
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<tr>
<td>20</td>
<td>6</td>
<td>R100, R101, R103, R104, R105, R106</td>
<td>Resistor</td>
<td>402</td>
<td>100 Ω, 1/16 W, 5% tolerance</td>
<td>Panasonic, ERJ-2GJ101X</td>
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<td>21</td>
<td>1</td>
<td>R117</td>
<td>Resistor</td>
<td>603</td>
<td>1 kΩ, 1/10 W, 5% tolerance</td>
<td>Panasonic, ERJ-3GEY102V</td>
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<td>22</td>
<td>18</td>
<td>R107, R108, R109, R110, R111, R112, R113, R115, R116, R122, R123, R124, R125, R126, R127, R201, R203, R204</td>
<td>Resistor</td>
<td>402</td>
<td>1 kΩ, 1/16 W, 1% tolerance</td>
<td>Panasonic, ERJ-2RFK1001X</td>
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<td>3</td>
<td>R114, R200, R300</td>
<td>Resistor</td>
<td>402</td>
<td>261 Ω, 1/16 W, 1% tolerance</td>
<td>Panasonic, ERJ-2RFK2610X</td>
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<td>10</td>
<td>R118, R119, R120, R121, R128, R129, R130, R131, R132, R133</td>
<td>Resistor</td>
<td>402</td>
<td>49.9 Ω, 1/16 W, 1% tolerance</td>
<td>Panasonic, ERJ-2RFK49R9X</td>
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<td>25</td>
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<td>R134</td>
<td>Resistor</td>
<td>402</td>
<td>10 kΩ, 1/16 W, 1% tolerance</td>
<td>Yageo America, 9C04021A1002JLHF3</td>
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<td>ADP33339AKC-3.3, 1.5 A, 3.3 V LDO regulator</td>
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<td>BGA</td>
<td>XC2V250-5FG256C, FPGA</td>
<td>Xilinx, XC2V250-5FG256C</td>
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<td>SSOT</td>
<td>XCF02SV020, EPROM</td>
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<td>MP101-104</td>
<td>Part of assembly</td>
<td>CBSB-14-01A-RT, 7/8” height, standoffs for circuit board support</td>
<td>Richco, CBSB-14-01A-RT</td>
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<td>31</td>
<td>5</td>
<td>MP105-108</td>
<td>Part of assembly</td>
<td>SNT-100-BK-G-H, 100 mil jumpers</td>
<td>Samtec, SNT-100-BK-G-H</td>
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### ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Package Description</th>
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<tr>
<td>HSC-ADC-FPGA-9289</td>
<td>Quad-Channel High Speed Serial LVDS to Parallel CMOS Converter for the AD9289 only</td>
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<tr>
<td>HSC-ADC-FPGA-4</td>
<td>Quad-Channel High Speed Serial LVDS to Parallel CMOS Converter for the AD9287, AD9219, AD9228, AD9229, AD9259</td>
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</table>

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.