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ST-NXP Wireless

AN10023

Interfacing ISP1160x to Fujitsu SPARClite RISC processor

Rev. 02 — 7 April 2008 Application note

Document information

Info	Content
Keywords	isp1160; host controller; usb; universal serial bus
Abstract	This application note explains interfacing the ISP1160x to Fujitsu SPARClite RISC processor. **Remark**: ISP1160x denotes any NXP embedded USB host controller whose name starts with 'ISP1160'.

Revision history

Rev	Date	Description
02	20080407	Ported to the NXP template. Updated Fig 2.
01	20030107	First release.

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Remark: ISP1160x denotes any NXP embedded USB host controller whose name starts with 'ISP1160'.

1. Overview

When the ISP1160x is integrated into a PDA or Handheld Personal Computer (HPC), it is usually connected to the external bus interface of a Reduced Instruction Set Computer (RISC) processor. This application note explains some of the important issues in such a design, using a concrete example of the Fujitsu SPARClite RISC.

2. ISP1160x processor interface signals

The processor bus interface of the ISP1160x is designed for a simple direct connection with a RISC processor. The data transfer can be done in Programmed I/O (PIO) or Direct Memory Access (DMA) mode. The estimated maximum data transfer rate on the generic processor bus of the ISP1160x is approximately 15 MB/s. This is based on an ISP1160x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, the ISP1160x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal host controller. The host controller uses 2 kB of the ping memory and 2 kB of the pong memory in its allocated memory.

The main ISP1160x signals to consider when connecting to a Fujitsu SPARClite RISC processor are:

- A 16-bit data bus D[15:0] for the ISP1160x. The ISP1160x is little endian compatible.
- An address line A0, which is necessary for the complete addressing of the ISP1160x internal registers:
  - **A0 = 0**, Selects the data port of the host controller
  - **A0 = 1**, Selects the command port of the host controller
- A CS_N line used for selection of the ISP1160x in a certain address range of the host system. This input signal is active LOW.
- RD_N and WR_N are common read and write signals. These signals are active LOW.
- A set of DMA channel standard control lines DREQ, DACK_N and EOT are used. Because the SPARClite processor does not contain a DMA controller, these signals will not be used in a minimal hardware implementation.
- Interrupt line INT, which is programmable as active on level or edge and HIGH or LOW.
- The CLKOUT signal has a maximum value of 48 MHz.
- The RESET_N signal is active LOW.

3. Fujitsu SPARClite

The SPARClite processor is part of the 32-bit RISC Fujitsu family.

The external bus interface of the SPARClite processor is a non-multiplexed address and data bus. It has a big endian architecture. An internal programmable chip select logic and an on-chip address decoder allow easy interfacing to EPROM, DRAM (EDO/FPM), UART, or general ASIC without additional glue logic. The integrated DRAM controller can generate all the signals necessary to provide a direct interface to various types of

memory; FPM and EDO DRAMS. The address decoder of the SPARClite processor can generate six programmable chip select signals. One of the CS0–CS5 signals will be asserted when the selected address matches the value programmed in the Address Range Specifier register. The Address Mask register is used to mask certain bits of the address.

To select the properties of each area, set certain values in internal control registers:

- Bus size: 8 bits, 16 bits or 32 bits can be independently set for each area, and is determined by the value of the bus width or cacheable register of the SPARClite processor.
- Number of wait cycles: Can be independently set for each selected area by setting the Wait States Specifier register of SPARClite.
- Setting the type of space: SRAM, DRAM and EPROM. The SPARClite processor will generate the necessary signals to control any of these types of memory.

Each addressed area of the SPARClite processor can be used only in big endian mode. For correct data alignment, there must be matching data widths and matching endians. During the design phase of a system using SPARClite and ISP1160x, take extra care when developing schematics and software because the ISP1160x connection requires a 16-bit or little endian configuration of the selected memory area.

4. Considerations in timing diagrams and WAIT states

The following is a short study of the timing diagrams of the ISP1160x.

According to the ISP1160x data sheet specifications, a read cycle requires the following main timing parameters (the requirements of the write cycle are similar):

- t_{RL}= 33 ns (RD_N LOW pulse width; minimal value required by the ISP1160x)
- t_{RHRL}= 110 ns (RD_N HIGH to next RD_N LOW; minimal value required by the ISP1160x)
- t_{RHDZ}= 3 ns (RD_N hold time, minimal value that can be expected from the ISP1160x)
- t_{RC} = 143 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SHSL} = 300 ns (first RD_N/WR_N after command)

For a detailed analysis of a timing diagram, consider the access of an ISP1160x internal register (for example, the Control register of the host controller). It requires two phases: writing the address of the selected register to the command port; then only data transfer access (RD/WR) takes place.

The timing diagram in Fig 1 describes the two phases of accessing the ISP1160x:

- The first phase is to access the ISP1160x command (control) port of the ISP1160x to write the address (index) of the data port that will be accessed. In this phase, CS_N is active. Data lines D[15:0] contain the desired address. The WR_N pulse will be activated and will latch data. Note the value of t_{SHSL} that represents the minimum time required between the occurrence of the first phase and the second phase. As an example of the host controller Control register, a value of 01h will be transferred during an RD_N operation and 81h during a WR_N operation.
- The second phase consists of the access (read or write) to the data port selected by the address latched in the previous phase. Two timing diagrams are combined again in this second phase: one for the read access and one for the write access. A series

of RD_N and WR_N pulses are shown in the diagram to define timing requirements between two consecutive accesses to the ISP1160x: t_{RHRL}, t_{WHWL}, t_{RC}, t_{WC}, t_{RLDV}, as specified in the data sheet.

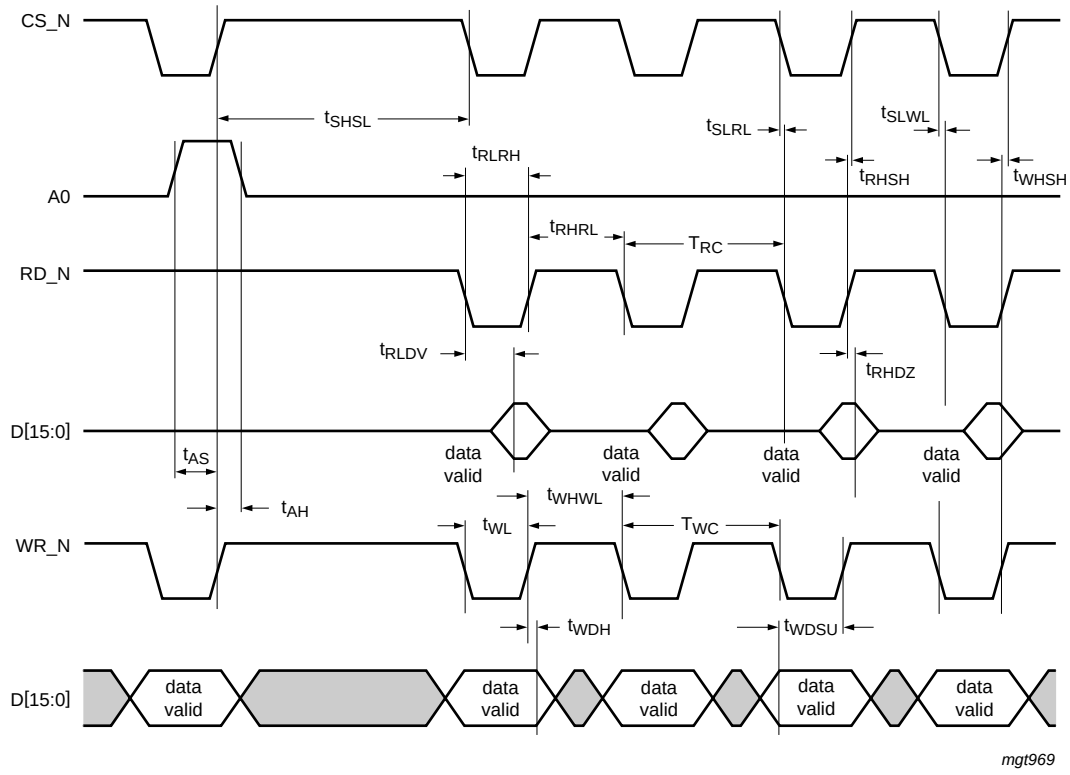

Fig 1. Programmed interface timing (16-bit read/write)

When the ISP1160x connection area is defined as SRAM, the ISP1160x will operate correctly when bus clock CKIO = 33 MHz. Timing measurements show that inserting wait-states in the standard bus cycles of SPARClite is unnecessary. Nevertheless, wait-state insertion is described, to cater for cases when faster bus cycles are used to access the ISP1160x.

Wait states insertion may be achieved using two solutions: hardware or software implementation. Both solutions will delay the rising edge of RD_N or WR_N to the next CKIO cycle and will determine an elongation of the RD_N or WR_N LOW pulse that can be calculated as:

t_W = W x T(CKIO); where: W is the number of wait states desired or selected.

T(CKIO) is the cycle length of CKIO.

Remark: The value of t_{RHRL} will not be modified by the number of wait states inserted by any of the solutions mentioned earlier. The value of this parameter must be calculated and correctly adjusted according to the number and length of instructions executed by the SPARClite processor between two successive accesses to the ISP1160x. The software solution for wait-state insertion in a bus cycle is simple and is preferred in a minimal configuration, if additional wait states are necessary.

5. Using interrupts

The ISP1160x generates an interrupt on the INT pin. This INT signal can be directly connected to any of the available IRQ signals of the SPARClite processor. The INT of the ISP1160x can be programmed as active on level or edge and HIGH or LOW, as specified in the HcHardwareConfiguration register.

6. Schematics

Fig 2 shows the connection of the ISP1160x to a Fujitsu SPARClite processor in a minimal hardware configuration. For a detailed description on connecting the ISP1160x to a RISC processor and a study of each category of signals and timing diagrams, refer to application note *Interfacing ISP1160x to Hitachi SH7709 RISC processor (AN10024)*.

In this configuration, the ISP1160x is simply selected by CS5#, which is asserted according to the values programmed in the Address Range Specifier register and the Address Mask register.

To correctly access the ISP1160x, it is assumed that area 5 is programmed for the SRAM memory type for 16-bit accesses. Data lines D[15:0] of the SPARClite processor will be used in this configuration, and pull-up resistors must be connected to the data bus lines that are not used (D[31:16]); according to SPARClite data sheet specifications. In this configuration, the RD_N input signal of the ISP1160x is generated by negating the RD_N/WR_N signal generated by the SPARClite processor. Therefore, the RD_N input signal of the ISP1160x will be active most of the time because the SPARClite RD_N/WR_N signal is HIGH during a read or idle cycle. This will not create any conflicts on the system data bus because the ISP1160x will enable its internal output buffers only when CS_N is also active in the same time.

Interrupt INT is arbitrarily connected to the IRQ8 line of the SPARClite processor. The interrupt controller of the Fujitsu SPARClite processor allows independent setting of interrupt trigger mode for each input, by programming its Trigger Mode 0 and 1 registers. The ISP1160x also allows programming of polarity (LOW or HIGH) and signaling mode (level or pulse) for the generated interrupt INT by correctly setting the bits of HcHardwareConfiguration registers.

Input signals H_OC1_N and H_OC2_N are used by the ISP1160x to detect an overcurrent on downstream facing ports. Because separate overcurrent detection and protection circuits are implemented for each downstream port of the ISP1160x, detection of overcurrent on a downstream port will cause power to be turned off at that port only. Connecting the voltages of two downstream ports VBUS_DN1 and VBUS_DN2 to the H_OC1_N and H_OC2_N pins enable detection of the current value by sensing the voltage drop on Q1 and Q2 that are MOS transistors with very low switch-on resistance R_{DSon}. Q1 or Q2 is selected, depending on the desired maximum current value and this determines the value of R_{DSon}. For example, if the allowed maximum current is about 0.5 A, a voltage drop of 75 mV will trigger the overcurrent circuitry and an approximate value of R_{DSon} = 150 MΩ will result. Connecting ISP1160x input pins H_OC1_N and H_OC2_N to +5 V will disable the internal overcurrent protection of the ISP1160x; an external overcurrent protection circuit may also be used.

The RESET_N input signal of the ISP1160x is connected to the RESET# input signal of the SPARClite processor, and both are connected to the system RESET generation circuitry.

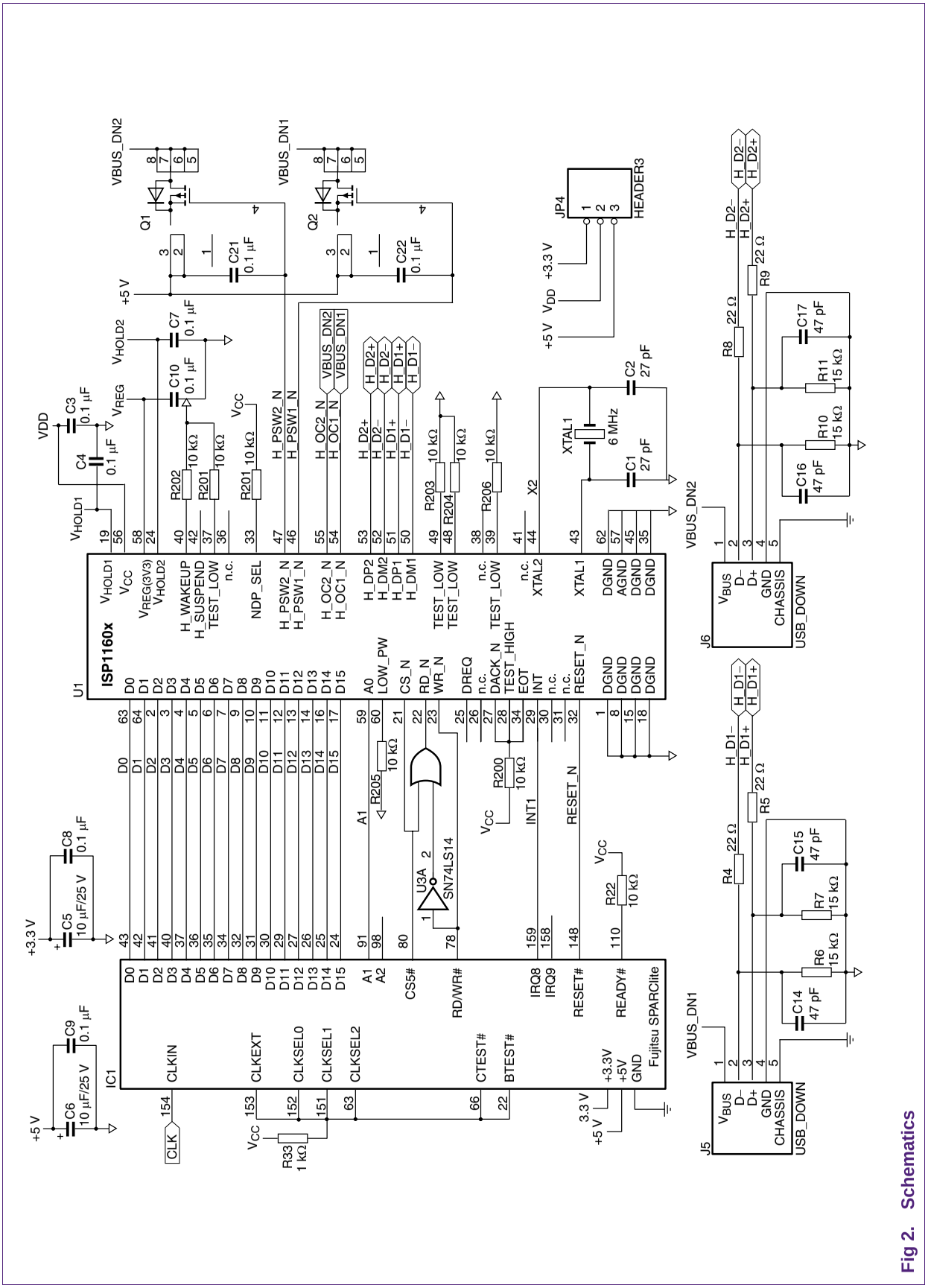

Fig 2. Schematics

7. Abbreviations

Table 1. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
DMA	Direct Memory Access
EDO	Extended Data Out
FPM	Fast Page Mode
HPC	Handheld Personal Computer
PIO	Programmed I/O
RISC	Reduced Instruction Set Computer
UART	Universal Asynchronous Receiver-Transmitter

8. References

- Universal Serial Bus Specification Rev. 2.0
- ISP1160 Embedded Universal Serial Bus Host Controller data sheet
- ISP1160A1 Embedded Universal Serial Bus Host Controller data sheet
- Interfacing ISP1160x to Hitachi SH7709 RISC Processor (AN10024) application note

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