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ST-NXP Wireless

AN10048

Interfacing to the ISP1504, ISP1505 and ISP1506

Rev. 03 — 6 November 2007 Application note

Document information

Info	Content
Keywords	isp1504; isp1505; isp1506; ip4359; usb; ulpi; universal serial bus; transceiver; utmi+ low-pin interface; host; peripheral; otg; phy, murata cstce26m0xk2
Abstract	This document describes how a link can interface to the ISP1504/5/6 for a host, a peripheral or an OTG application. This document also includes the PCB design guidelines when integrating the transceiver into a system.

Revision history

Rev	Date	Description
03	20071106	Third release. Replaced IP4059 with IP4359. Updated Section 3.3, Section 4.2, Section 4.3, Fig 2, and kept last three figures. Removed all instances referring to “input mode”.
02	20061213	Second release. Updated Section 3.3.
01	20060601	First release.

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1. Introduction

The ISP1504, ISP1505 and ISP1506 are Hi-Speed Universal Serial Bus (USB) host and peripheral transceivers that are fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. The ISP1504 and ISP1506 are also On-The-Go (OTG) transceivers that are fully compliant with *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*.

These transceivers support high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates. The internal architecture of the ISP1504/5/6 is a highly optimized ULPI-compliant interface operating at 60 MHz. The ISP1504/5/6 interfaces to USB ASIC, FPGA or any system chip set through an 8-pin or 12-pin ULPI interface. All static UTMI signals are accessed through the ULPI compliant register set. The ULPI interface includes a 4-bit or 8-bit data bus, three control signals and a 60 MHz clock signal for synchronization. The bidirectional data bus with control signals can synchronously transmit and receive USB packets, and access register data.

Table 1 summarizes various specifications of the ISP1504, ISP1505 and ISP1506 transceivers.

Table 1. ISP1504/5/6 specifications

Feature	ISP1504	ISP1505	ISP1506
Embedded charge pump	Yes	No	Yes
Digital I/O interface	1.65 V to 3.6 V	1.65 V to 3.6 V	1.65 V to 1.95 V
OTG support	Full	SRP	Full
Number of interface pins with a link	12	12	8
Data bus	8	8	4
Packaging	HVQFN32	HVQFN24	HVQFN24

The ISP1504/5/6 is ideal for use in portable electronic devices, such as digital cameras, Personal Digital Assistants (PDAs) and mobile phones.

This application note describes how a link can interface to the ISP1504/5/6 for host, peripheral or OTG applications. Guidelines to design the ISP1504/5/6 transceiver with good USB high-speed quality signal are also given in this document.

2. Features of the ISP1504/5/6

- Fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*; in addition, the ISP1504/6 fully complies with *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
- 12-pin interface to host, peripheral and OTG device cores for the ISP1504/5; 8-pin interface for the ISP1506
- Flexible system integration and very low power consumption
- Integrated 3.3 V and 1.8 V regulators, supplying internal analog and digital circuits
- Integrated charge pump for the ISP1504/6 to supply up to 50 mA current to V_{BUS}
- Supports wide range (1.65 V to 3.6 V) I/O interface voltage for the ISP1504/5; separate supply pins, minimizing crosstalk

3. ISP1504/5/6 basic configuration

3.1 Powering the ISP1504/5/6

There are two power supplies for the ISP1504/5/6: V_{CC} and $V_{CC(I/O)}$. The V_{CC} pin supplies power to two on-chip regulators that generate 1.8 V and 3.3 V outputs. The 1.8 V regulator supplies power to digital circuits while the 3.3 V regulator supplies to analog circuits. ULPI interface I/Os are powered by $V_{CC(I/O)}$ to reduce crosstalk between digital I/Os and analog USB signals. The integrated charge pump for the ISP1504/6 directly draws power from the V_{CC} input. Fig 1 illustrates the internal powering strategy for the ISP1504/5/6.

REG3V3 and REG1V8 are output pins from internal regulators. It is not recommended that you use these regulator outputs to drive external circuits. Filtering and bypassing capacitors must be connected to these pins to obtain stable DC voltage as given in Fig 1. It is recommended that you select a 4.7 µF capacitor with low Equivalent Serial Resistance (ESR) to achieve low ripple voltage on the output of these regulators.

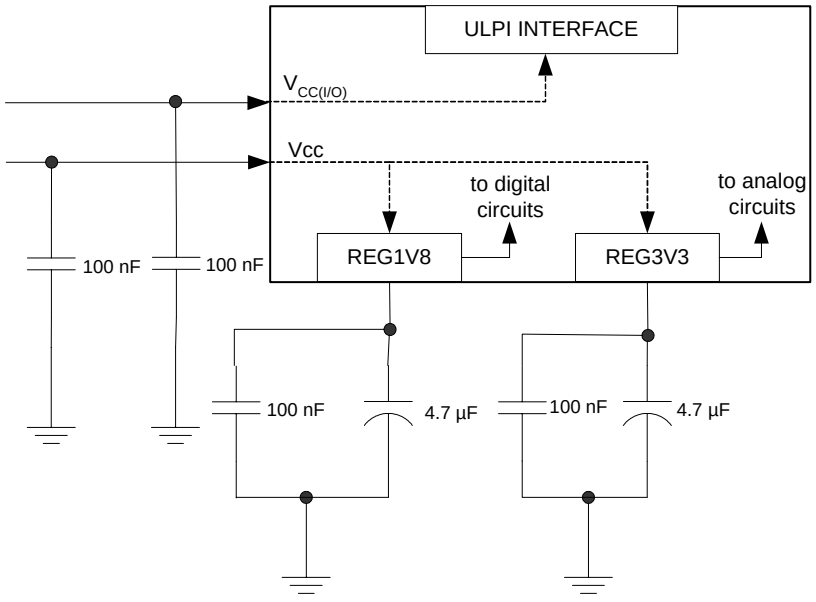

Fig 1. Powering the ISP1504/5/6

3.2 Biasing the ISP1504/5/6

A 12 kΩ ± 1 % resistor must be chosen to connect the RREF pin of the ISP1504/5/6 to the ground. This resistor is used as a reference for the internal band gap circuit, which generates a stable band gap voltage to bias the analog circuitry. A less accurate resistor cannot be used and may render the ISP1504/5/6 unstable.

When troubleshooting the ISP1504/5/6 transceiver, always check the voltage at the RREF pin to ensure that it is around 1.22 V. A correct voltage indicates that the transceiver is alive and correctly biased. Bad soldering and improper grounding may result in abnormal voltage at RREF.

3.3 Clock for the ISP1504/5/6

The clock source for the ISP1504/5/6 can be provided through various ways (see Fig 2):

- A crystal connected between pins XTAL1 and XTAL2 of the ISP1504/5/6 to provide a clock to the chip (called output clock mode). Table 2 lists the crystal frequency for various versions of the ISP1504/5/6. The recommended crystal must have:
  - Frequency tolerance: 50 ppm
  - Shunt capacitance: not greater than 7 pF
  - Load capacitance: 10 pF
  - Crystal ESR: less than 80 Ω
- A ceramic resonator can also be used to provide a 26 MHz clock to the chip. The resonator CSTCE26M0XK2 from Murata has been tested and verified working with the ISP1505. This resonator has a body size of only 3.2 mm × 1.3 mm and does not need external load capacitors, which means much less PCB space is required than if a crystal is used. For more information about the resonator, please contact Murata directly.
- A square wave clock signal driven into pin XTAL1 to provide a clock to the chip (called output clock mode). Leave pin XTAL2 open. Table 3 lists the clock frequency for various versions of the ISP1504/5/6. The clock must be a $1.8V_{(p-p)}$ square wave signal with 50 % duty cycle. The jitter tolerance of the clock signal must be less than 200 ps. A 47 kΩ pull-up resistor on pin XTAL1 to regulator REG1V8 is required to avoid floating input. A 100 pF capacitor is required in series, if there is a DC offset voltage on the clock.

Table 2. Crystal or clock frequency for the ISP1504/5/6

Chip version	Crystal frequency or clock signal frequency
ISP1504A	19.2 MHz
ISP1505A	19.2 MHz
ISP1506A	19.2 MHz
ISP1504C	26 MHz
ISP1505C	26 MHz
ISP1506B	26 MHz

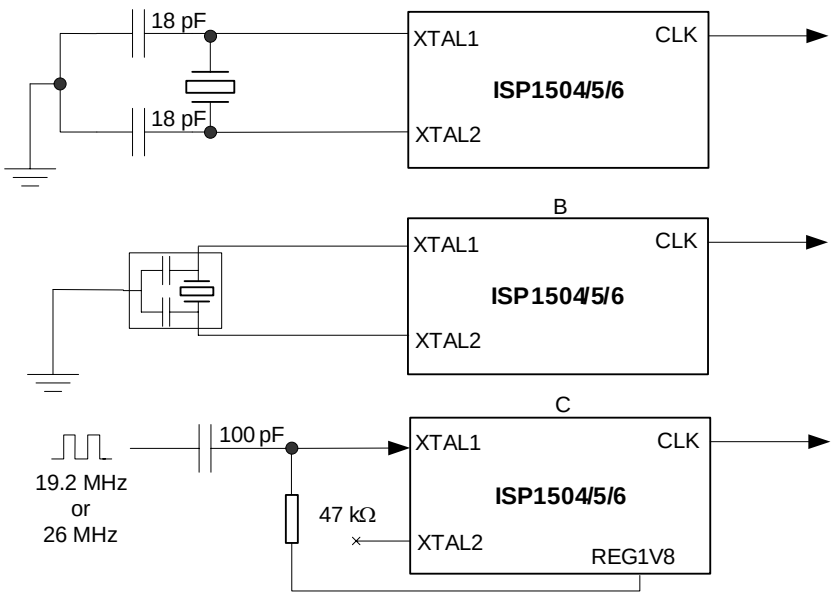

Fig 2. Clock for the ISP1504/5/6

In output clock mode, pin CLOCK will stop 60 MHz output when the transceiver goes into low-power mode (also called suspend mode). Stopping the 60 MHz clock will reduce the power consumption and the transceiver will only draw minimum current from the V_{CC} supply.

4. USB interfacing

The ISP1504/5/6 USB interface consists of the V_{BUS}, DP and DM pins. The ISP1504/6 has an extra ID pin for OTG applications. This section describes the design guidelines for the USB interface to improve the robustness of products.

4.1 V_{BUS} protection

It is recommended that you connect filtering capacitors between V_{BUS} and ground on the PCB. These capacitors ensure that the device is not damaged and that the device functions properly when the USB cable is plugged or unplugged.

Table 3 summarizes recommended capacitor values to filter V_{BUS} for various applications.

For host applications, it is recommended that you connect a capacitor of 120 µF to V_{BUS}. This ensures that the voltage on V_{BUS} does not suddenly drop below its minimal operating level when a device is attached. For peripheral or OTG applications, the capacitance between V_{BUS} and ground must be kept small so that the device does not draw a large inrush current when attached. It is recommended that you connect a minimum of 1 µF capacitor to V_{BUS} on the PCB so that the flyback voltage at the device is properly bypassed to ground. For details, refer to Section 7.2.4 of *Universal Serial Bus Specification Rev. 2.0*.

Table 3. Recommend capacitor value filtering V_{BUS}

C_{VBUS}	Min	Max	Unit
Host	120	-	µF
OTG	1	6.5	µF
Peripheral	1	10	µF

It is also recommended that you insert a 1 kΩ resistor between pin V_{BUS} of the ISP1504/5/6 and the USB connector, if the internal charge pump is not used. This helps to improve the Electrical Overstress (EOS) performance of the ISP1504/5/6 so that the system will be more robust when working with hubs and hosts from various vendors.

4.2 DP and DM

The PCB design for the DP and DM lines are critical to the high-speed signal quality of the product. The PCB routing and layer stack must ensure the 90 Ω differential trace impedance for DP and DM. The parallelism between the DP and DM lines must be maintained and traces must be of the same length. For details, refer to *High Speed USB Platform Design Guidelines Rev. 1.0*.

4.3 Pin ID in the ISP1504/6

In OTG applications, the ID pin is implemented to detect whether the device must function as an A-device or a B-device, when the USB cable is initially plugged in. An OTG controller must enable the pull-up resistor on the ID pin by setting the ID_PULLUP bit in the OTG Control register. When a mini-A cable is plugged into the receptacle, the ID pin will be pulled to LOW. When a mini-B cable is plugged into the receptacle, the ID pin will remain at HIGH. Therefore, the device will know what role it must play.

For host and peripheral applications, the ID pin is not used. It is recommended that you connect the ID pin to REG3V3.

5. ULPI interfacing

5.1 Reset for the ISP1504/5/6

A link can reset the ISP1504/5/6 by driving the asynchronous RESET_N pin to LOW. The link must hold the reset at LOW for at least eight clock cycles. The ULPI data bus and the STP pin must be driven to LOW throughout the reset process. Otherwise, the behavior of the ISP1504/5/6 is undefined.

For the ISP1505/6, the asynchronous reset input is multiplexed with the PSW_N output as the RESET_N/PSW_N pin. Designers must ensure that the DRV_VBUS_EXT bit in the OTG Control register and the IGNORE_RESET bit in the Power Control register are cleared (power-on default value), before asserting the reset signal.

After resetting the transceiver, the link must set the RESET bit in the Function Control register to reset the ULPI state machine. Any RXCMDs received before this will be ignored.

5.2 Chip select in the ISP1504

The ISP1504 can share its ULPI interface pins with other chips. When the CHIP_SELECT_N pin of the ISP1504 is driven to LOW, ULPI pins are used by the

ISP1504. When the CHIP_SELECT_N pin is driven to HIGH, the ISP1504 will 3-state the ULPI data bus, NXT and DIR outputs so that other chips can use these pins. The STP input is ignored in this case. It is recommended that you perform software reset to reset the ULPI state machine after the ISP1504 is re-selected.

5.3 Synchronizing ULPI interface

The ULPI interface is a synchronous interface. The bus traffic is synchronized with the CLOCK pin. To reliably transmit and receive USB packets, the setup and output delay timing must be met with reasonable margin to ensure that the system functions properly even under worst-case conditions. This is especially critical for the DDR interface (ISP1506). As a general guideline, 18 cm of the outer PCB trace or 14 cm of the inner PCB trace introduces 1 ns delay. It is recommended that you limit the PCB trace to less than 5 cm to minimize transmission line effect and increase timing margin.

6. ISP1504/5/6 in applications

The ISP1504/6 can be used as a host, peripheral or OTG transceiver. The ISP1505 can be used as a host or peripheral transceiver. The following subsections describe how a link can interface to the ISP1504/5/6 in host, peripheral and OTG applications.

6.1 Host application

The ISP1504/5/6 can be used as a USB physical layer transceiver for host applications. The host must supply current to V_{BUS}. A standard PC host must supply at least 500 mA current whereas the current capability for an embedded host depends on the targeted application. In this section, it is assumed that the host must supply more than 50 mA current to V_{BUS}. Therefore, an external V_{BUS} power switch or a charge pump is required to supply this current. The external power switch or the charge pump must preferably have an overcurrent or a fault output and must thermally shut itself down for safety reasons.

Table 4 describes register bits related to the operation of the external power switch or the charge pump.

Table 4. Registers settings for the external V_{BUS} power switch

Register bit	Remark
DRV_VBUS_EXT	Set to enable the PSW_N open-drain output; cleared to disable the output
USE_VBUS_IND	Set to detect overcurrent or other fault condition
IND_PASSTHRU	If set, the A_VBUS_VLD bit in RXCMD depends only on the FAULT input; if cleared, it depends on both the FAULT input and the V_{BUS} pin
IND_COMPL	If the fault output from the power switch is active LOW, this register bit must be cleared; otherwise this register bit must be set

In Fig 3, the ISP1504 operates in output clock mode with crystal connected between XTAL1 and XTAL2. V_{BUS} is supplied using an external power switch that is controlled by the ISP1504. The PSW_N pin for the ISP1504 is a 5 V tolerant open-drain output that is pulled up to 5 V.

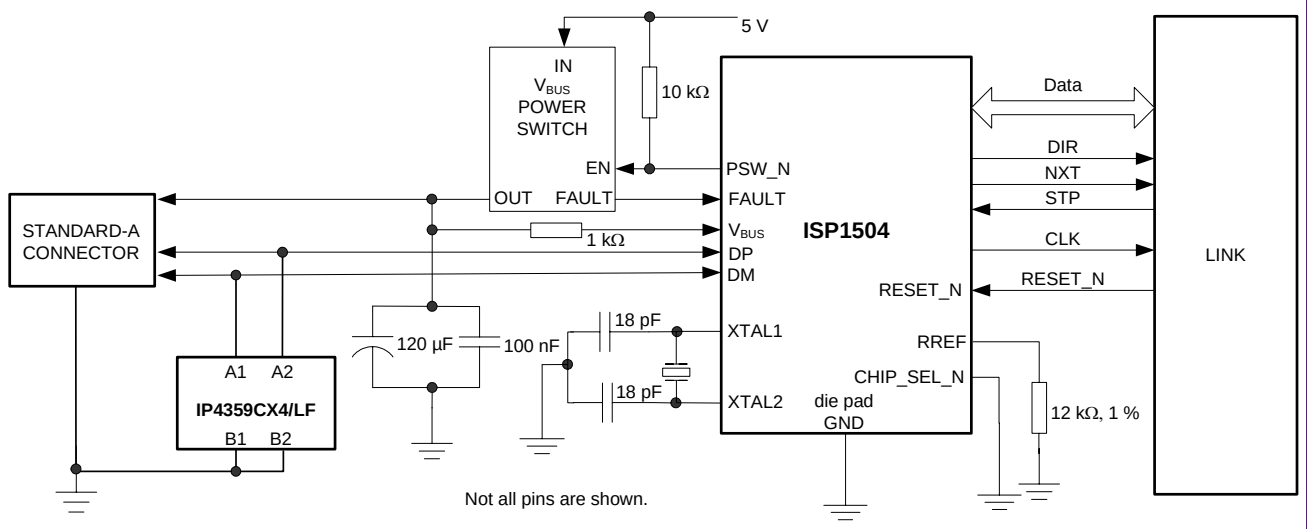

Fig 3. Host applications for the ISP1504

Table 5. Register settings for the external charge pump

Register bit	Remark
DRV_VBUS_EXT	Set to turn on the external charge pump; cleared to turn off the external charge pump
USE_VBUS_IND	Set to detect overcurrent or other fault condition
IND_PASSTHRU	Set, bit A_VBUS_VLD in RXCMD depends only on the fault input
IND_COMPL	If set, the FAULT input is internally inverted; if cleared, the FAULT input is feed without inverting

For some applications, both the PSW_N and RESET_N functions may be utilized. Designers must ensure that no contention condition occurs. Note that when the DRV_VBUS_EXT bit in the OTG control register is set to turn on the external power switch or the charge pump, the IGNORE_RESET register bit will automatically be set. The IGNORE_RESET register bit will not automatically be cleared when the DRV_VBUS_EXT register bit is cleared. The IGNORE_RESET register bit must manually be cleared after the external power switch or charge pump is disabled.

6.2 Peripheral application

The ISP1504/5/6 can be used as a USB physical layer transceiver for peripheral applications. As a peripheral, the ISP1504/5/6 must sense the voltage on V_{BUS}. When the voltage on V_{BUS} is above the $V_{A\_VBUS\_VLD}$ threshold, the peripheral must start to function.

The RESET_N input is optional because the ISP1504 has an internal Power-On Reset (POR) circuit. When the voltage on the REG1V8 regulator output rises above $V_{POR(trip)}$, a reset signal will be generated to reset the chip. When the link does not need to reset the transceiver, the RESET_N input must be pulled to HIGH. RESET_N for the ISP1504 is 5 V tolerant and can be pulled up to 5 V.

Fig 4 depicts another example to implement the ISP1505/6 as a peripheral transceiver. The RESET_N/PSW_N pin functions as a RESET_N input only, and the V_{BUS}/FAULT pin functions as a V_{BUS} input only because the peripheral device does not need to supply current to V_{BUS}. In Fig 4, the RESET_N/PSW_N pin is pulled up to 3.3 V through a resistor because RESET_N/PSW_N is only 3.3 V tolerant.

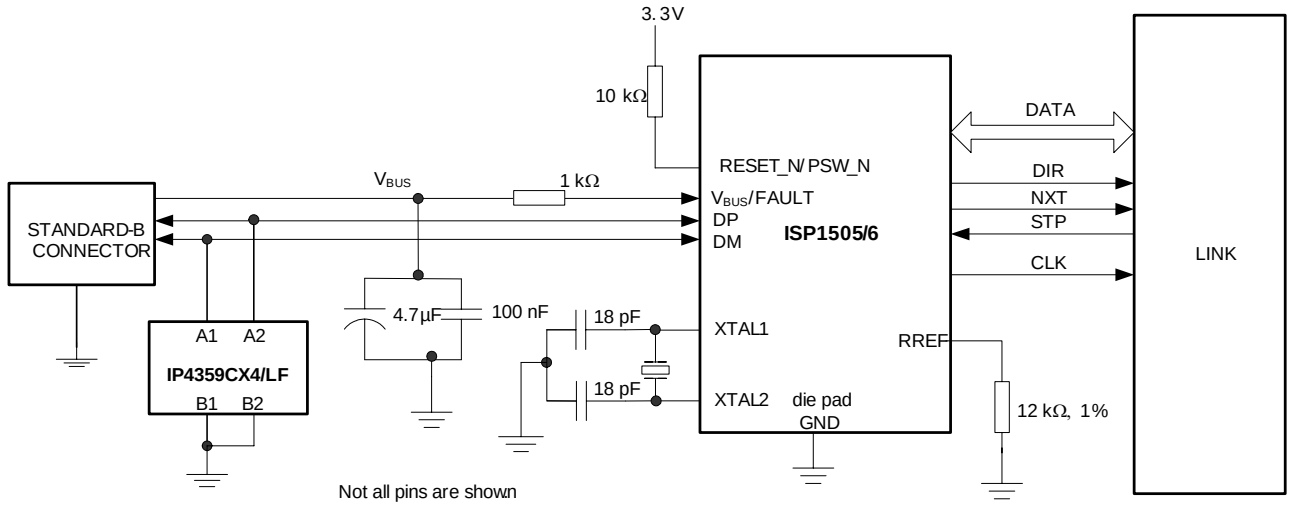

Fig 4. Peripheral applications for the ISP1505/6

6.3 OTG application

An OTG A-device provides V_{BUS}. The current that the A-device supplies to V_{BUS} depends on the application. For the ISP1504/6, an integrated charge pump is designed for OTG applications, which can source up to 50 mA current to V_{BUS}. In Fig 5, it is assumed that the current capability of an OTG A-device is less than 50 mA and the internal charge pump is utilized to supply to V_{BUS}. The current capability of the internal charge pump depends on the value of the external flying capacitor connected between C_A and C_B. As a general guideline, 22 nF will result in a drive capability of 8 mA, while 270 nF will result in a drive capability of 50 mA. Table 6 lists the register setting related to the internal charge pump.

Table 6. Register setting for the internal charge pump

Register bit	Remark
DRV_VBUS	Set to turn on the internal charge pump; cleared to turn off the internal charge pump
DRV_VBUS_EXT	This bit must be cleared (power-on default value).
USE_VBUS_IND	This bit must be cleared (power-on default value).

Fig 5 shows an example to interface the ISP1504/6 to a link for OTG applications.

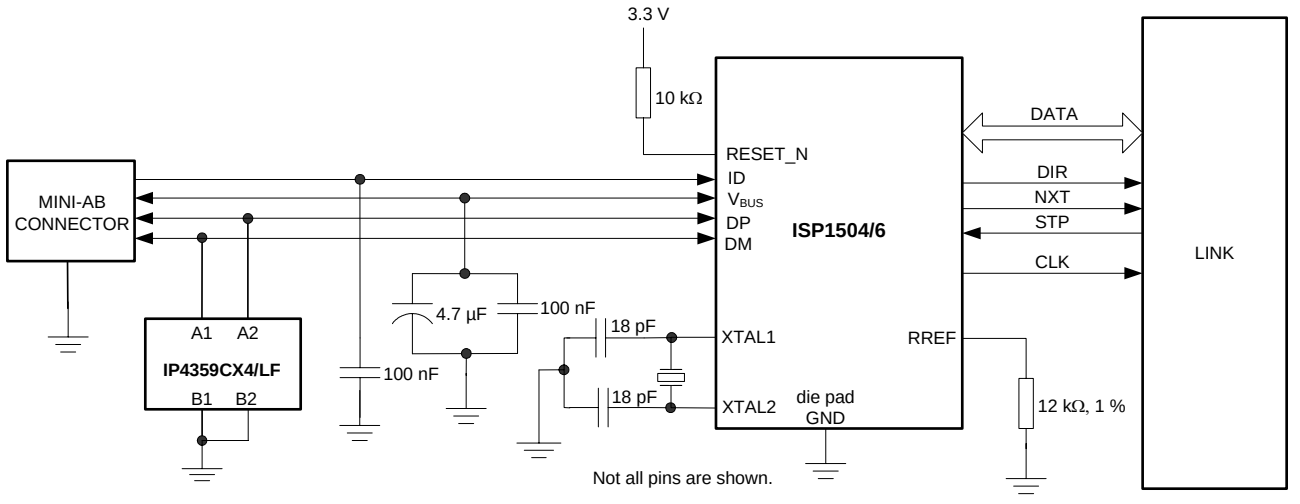

Fig 5. OTG application for the ISP1504/6 with internal charge pump

For the ISP1504/6, an external charge pump or a V_{BUS} switch is required if more than 50 mA current needs to supply V_{BUS} for OTG applications. Similarly, the ISP1505 can also be used in OTG applications if an external charge pump or a V_{BUS} switch is provided.

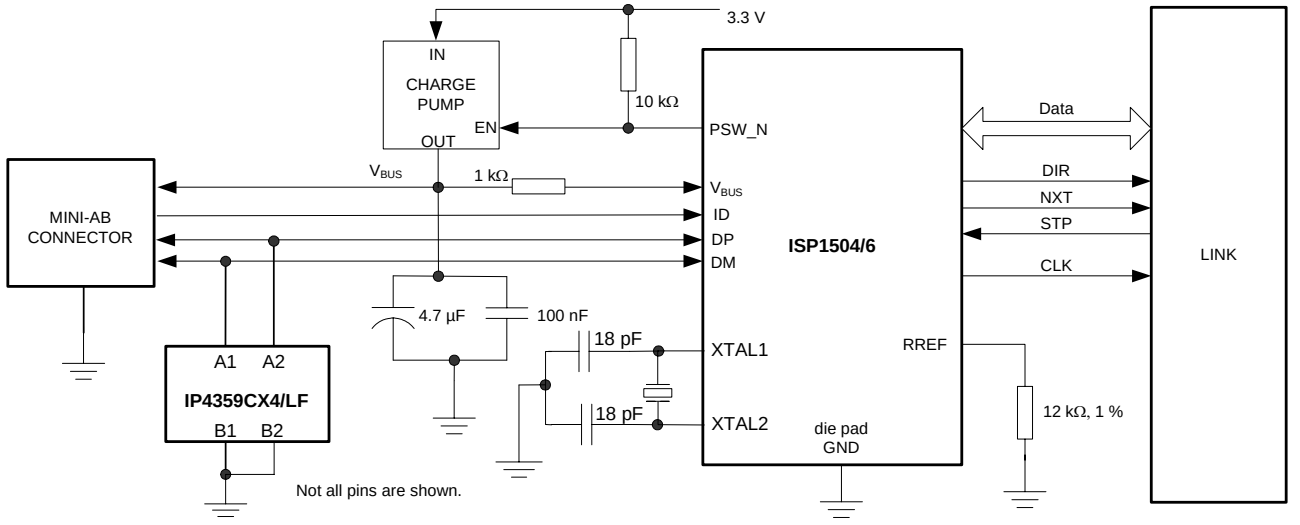

Fig 6. OTG application for the ISP1504/6 with an external charge pump

7. Guidelines for designing a PCB

This section describes PCB design guidelines when integrating the ISP1504/5/6 into a system.

- The PCB routing for the DP and DM lines must follow *High Speed USB Platform Design Guidelines Rev. 1.0*, to achieve high-speed signal quality.
- The exposed die pad at the bottom of the ISP1504/5/6 is a ground and therefore, must be grounded on the PCB board for the transceiver to function properly.
- The crystal must be connected as close as possible to the XTAL1 and XTAL2 pins of the transceiver. Loops must be made as small as possible to keep the noise coupled in through the PCB low.
- Place flying capacitor connected between pins C_A and C_B close to the pins.
- The 12 kΩ ± 1 % reference resistor must be placed close to the RREF pin and the other terminal is preferably via to the ground layer directly.
- Filtering capacitors connected to internal regulator outputs must have low ESR.
- Generally, ULPI interface pins can directly be routed to the USB controller. A serial termination resistor may be added to the clock line to attenuate reflection, which causes EMI problems. A 33 Ω resistor is usually chosen and placed close to the clock source.
- Bypass capacitors for power supplies must be placed close to the transceiver. Ferrite beads can be used to filter supplies to the transceiver, if the system supply is too noisy. Ferrite beads used in the application can be between 50 Ω and 120 Ω at 100 MHz, with a current rating of about 200 mA.
- The ISP1504/5/6 has built-in ESD protection. It is, however, strongly recommended that you use external ESD protection device to protect USB pins that are externally exposed on the end product. NXP recommends IP4359 for enhanced ESD protection. Designers must ensure that high-speed quality signals are not degraded when adding protection on the DP and DM lines.

8. Abbreviations

Table 7. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
FPGA	Field Programmable Gate-Array
DDR	Double Data Rate
EOS	Electrical OverStress
ESR	Equivalent Serial Resistance
ESD	ElectroStatic Discharge
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
POR	Power-On Reset
RXCMD	Receive Command
SRP	Session Request Protocol
OTG	On-The-Go
ULPI	UTMI+ Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
USB	Universal Serial Bus

9. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] ISP1504 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet

[4] ISP1505 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet

[5] ISP1506 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet

[6] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[7] USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2

[8] High Speed USB Platform Design Guidelines Rev. 1.0

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