AND8260/D

NCP1381/82 Demonstration Board 120 W Notebook Adapter with Power Factor Correction

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APPLICATION NOTE

Overview

The NCP1381 and NCP1382 are quasiresonant controllers developed to ease the design of 80 to 200 W switching power supplies requiring a Power Factor Correction (PFC) stage. One of its typical applications is notebook adapter power supply, in which high−efficiency, low standby power and low EMI are the key requirements.

This demonstration board has been designed in order to demonstrate NCP1381/82 capabilities. It thus gives the choice to implement various options, while offering enough space to plug scope probes.

Features

To help designers quickly developing a notebook adapter, the NCP1381/82 has been introduced. This SOIC−14 package hosts a high performance controller with all necessary features to build a rugged and reliable switching power supply:

- **Current−mode operation with Quasi−Resonant operation**: implementing peak current mode control, the NCP1381/82 waits until the drain−source voltage crosses a minimum level. This is the quasi−resonance approach, minimizing both EMI radiations and capacitive losses.
- **Over Power Protection**: using a voltage image of the bulk level, via the Brown−Out divider, the designer can select a resistor which, placed in series with the current sense information, provides an efficient line compensation method.
- **Frequency clamp**: the controller monitors the sum of T_{ON} and T_{OFF}, providing a real frequency clamp. Also the T_{ON} maximum duration is safely limited to 50 μs in case the peak current information is lost. If the maximum T_{ON} limit is reached, then the controller stops all pulses and enters a safe auto−recovery burst mode.
- **Go−to−standby signal for PFC front stage**: The NCP1381/82 includes an internal low impedance switch connected between pin 10 (V_{CC}) and pin 11 (GTS). The signal delivered by pin 11 being of low impedance, it becomes possible to connect PFC's V_{CC} directly to this pin and thus avoid any complicated interface circuitry between the PWM controller and the PFC front−end section. In normal operation, pin 11 routes the PWM auxiliary V_{CC} to the PFC circuit which is directly supplied by the auxiliary winding. When the SMPS enters skip−cycle at low output power levels, the controller detects and confirms the presence of the skip activity by monitoring the signal applied on its pin ADJ_GTS (typically FB signal) and opens pin 11, shutting down the front−end PFC stage. When this signal level increases, e.g. when the SMPS goes back to a normal output power, pin 11 immediately (without delay) goes back to a low impedance state. Finally, in short−circuit conditions, the PFC is disabled to lower the stress applied to the PWM main switch.
- **Skip−cycle capability**: a continuous flow of pulses is not compatible with no−load standby power requirements. Slicing the switching pattern in bunch of pulses drastically reduces overall losses but can, in certain cases, bring acoustic noise in the transformer. Thanks to a skip operation taking place at low peak currents only, no mechanical noise appears in the transformer. This is further strengthened by ON Semiconductor soft skip technique, which forces the peak current in skip to gradually increase. In case the default skip value would be too large, connecting a resistor to the pin 6 will reduce or increase the skip cycle level. Adjusting the skip level also adjusts the maximum switching frequency before skip occurs.
- **Over Voltage Protection**: by sensing the plateau level after the power switch has opened, the controller can detect an over voltage condition through the auxiliary reflection of the output voltage. If an OVP is sensed, the controller stops all pulses and permanently stays latched until the V_{CC} is cycled down below 4 V.
- **External latch input**: by permanently monitoring pin 5, the controller detects when its level rises above 3.5 V, e.g. in presence of a fault condition like an OTP. This fault is permanently latched−off and needs the V_{CC} to go down below 4 V to reset, for instance when the user un−plugs the SMPS.

- **Brown−out detection**: by monitoring the level on pin 2 during normal operation, the controller protects the SMPS against low mains condition. When the pin 2 level falls below 240 mV, the controller stops pulsing until this level goes back to 500 mV to prevent any instability. During Brown−Out conditions, the PFC is not activated.
- **Short−circuit protection**: short−circuit and especially over−load protection is difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8 V maximum peak current limit is activated, an error flag is asserted and a time period starts, thanks to an external timing capacitor. If the voltage on the capacitor reaches 4 V (after 90 ms for a 220 nF capacitor) while the error flag is still present, the controller stops the pulses and goes into a latch−off phase, operating in a low−frequency burst−mode. As soon as the fault disappears, the SMPS resumes its operation. The latch−off phase can also be initiated, more classically, when V_{CC} drops below V_{CCOFF} (10 V typical).

DESIGN DESCRIPTION

To be close to a real notebook adapter, the board will deliver 120 W on a 19.5 V output while correcting the power factor, but its consumption in no−load conditions will be lower than 500 mW. In addition the board includes several protections like brown−out or overpower, and provides the possibility to build an overvoltage protection.

Schematic

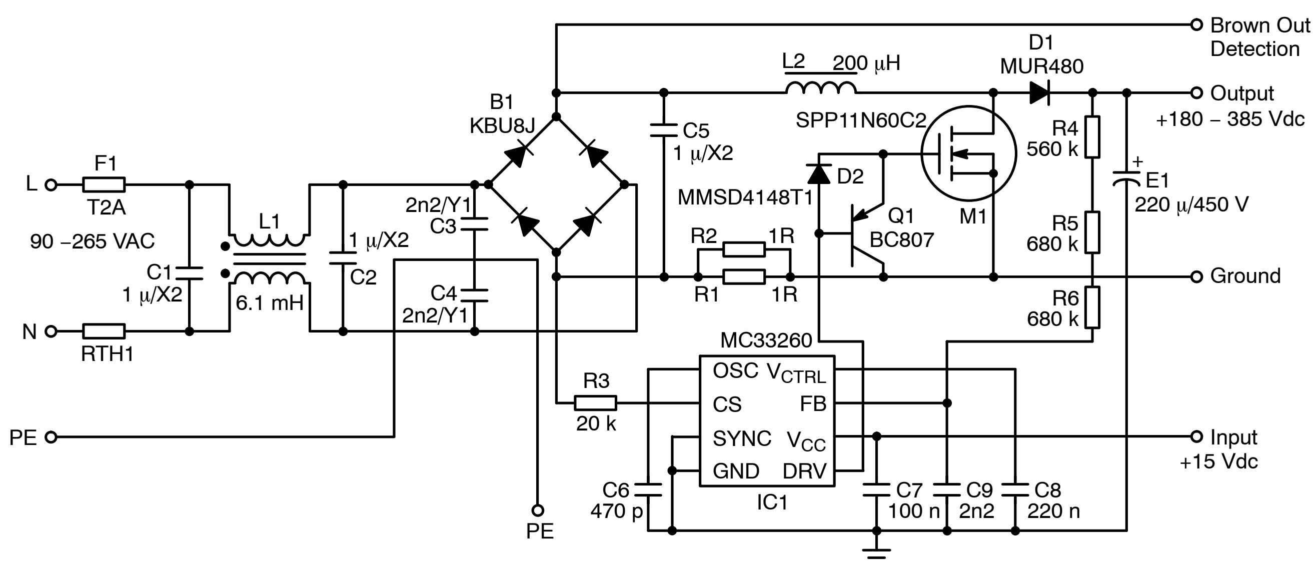


Figure 1. PFC Stage

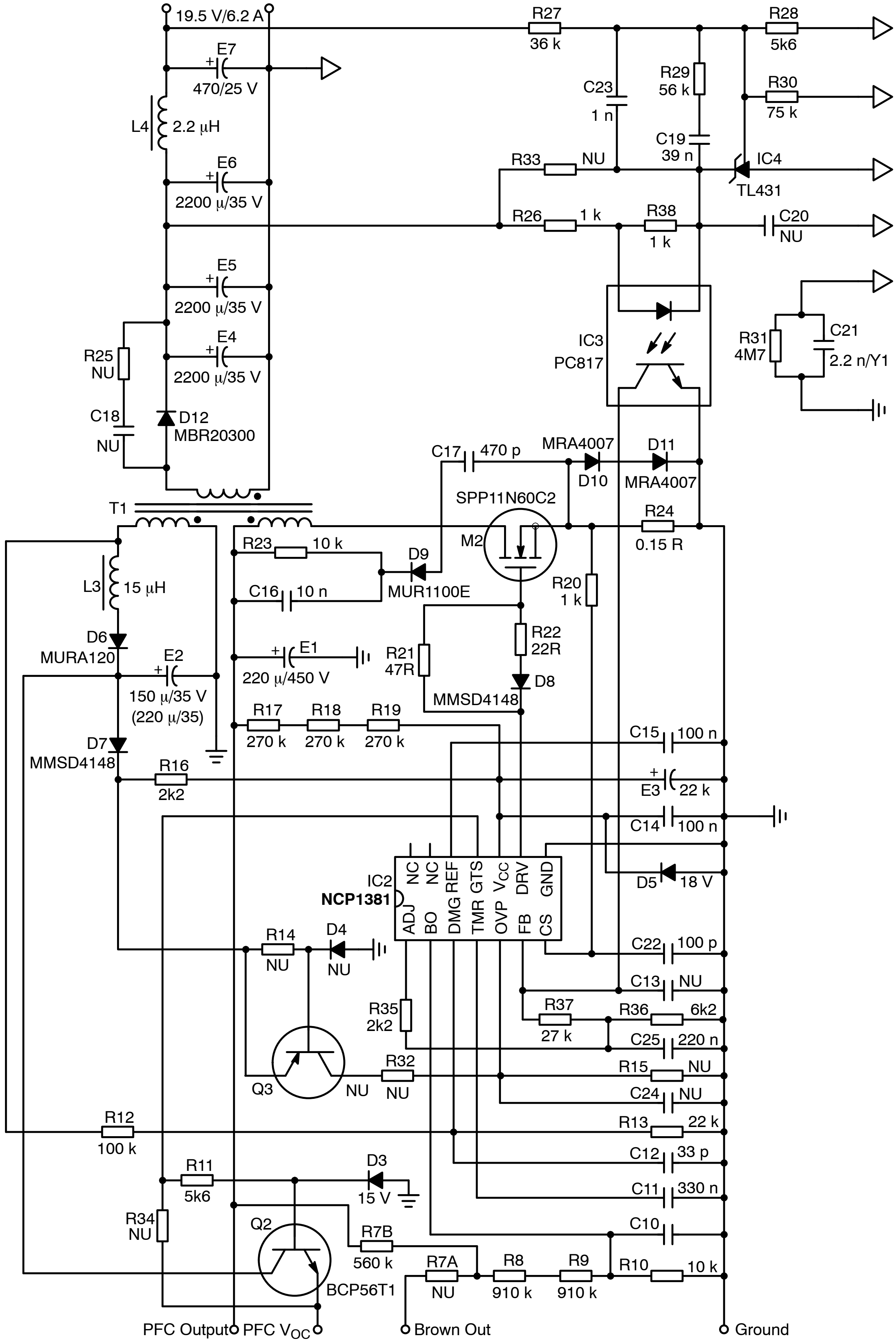


Figure 2. Valley Switching Comverter

DESIGN STEPS

PFC Stage

The PFC controller used is the MC33260, a controller for boost PFC stage featuring follower−boost capability. For the design of the PFC stage, please refer to the application notes AND8016 and AND8123.

Downstream Converter

Please refer to the application note AND8240 for the implementation of the NCP1381/82. Details of some design choices are described below.

Transformer

The primary inductance has been chosen in order to ensure a switching frequency lower than 130 kHz at high line when the output load is equal to 50% of the maximum load. An additional constraint is the turn ratio between primary and secondary inductors that must ensure that the voltage appearing across the switching MOSFET during OFF time is lower than 600 V with some margin.

Low line full load freq: 30 kHz

High line full load freq: 70 kHz

Valley jumping: < 50% load at high line

L_P = 240 μH

I_{Pmax} at low line: 6 A

Turn ratio primary / secondary is equal to 4.4 (2.75 for the auxiliary winding), ensuring a reflected voltage from secondary to primary $V_{REFLECT}$ < 100 V (exactly 90 V).

(See “Transformer construction” paragraph at the end of this document)

R_{SENSE}

The sense resistor is designed to allow the maximum peak current of 6 A. Knowing that the current sense comparator threshold is 800 mV, R_{SENSE} should then be smaller than 130 mW.

Brown−out

The voltage sensing for brown−out protection can either be taken in front of the PFC stage, for a true brown−out protection, or after the PFC stage for a better overpower protection (see below). With the second solution, there is a minimum start−up voltage, but not any more minimum operating voltage, so it is not a true brown−out protection.

OPP

When OPP resistor is added, R_{SENSE} must be adjusted. In order to set the overpower protection for an output power of 130 W, R_{SENSE} is changed to 120 mW, and R_{OPP} is set to 2.7 kW.

PFC Control (GTS)

The board provides two ways of connecting the PFC controller to the GTS signal: directly, or through a buffer (made with a bipolar transistor).

The power levels at which PFC turn on and off are set by R35, R36, R37 and C25: these levels are currently 25 W (turn−off) and 40 W (turn−on), but can easily be adjusted depending on the needs.

Auxiliary Winding

In order to ensure a V_{CC} higher than 10 V in no−load conditions, auxiliary voltage is 30 V, and V_{CC} capacitor is split. A Zener diode is added to protect the controller. Splitting the tank capacitor allows to increase the stored energy (in capacitor E2), while keeping a small V_{CC} capacitor (capacitor E1) that ensures a fast start−up time.

Clamp

The MOSFET used cannot sustain voltages above 600 V, we thus need to add a clamping network to protect it. The RCD clamp made of D9, R23 and C16 give a sufficient protection without degrading too much the standby power. If a lower standby power is needed, R23 and C16 can be replaced by a 200 V TVS.

Secondary Side

For the simplicity of the demonstration board, a Schottky diode will be used as a rectifier, and not a synchronous rectifier as it would be in a real application.

The regulation is made around a TL431.

MEASUREMENTS: Power Factor and Efficiency

Current Harmonic THD	Voltage Harmonic THD	Power Factor	I_{IN} (Adc)	U_{IN} (Vdc)	I_{OUT} (Adc)	U_{OUT} (Vdc)	P_{IN} (W)	P_{OUT} (W)	Eff. (%)
6.959	20.134	0.995	1.65	89.03	6.307	19.56	146.68	123.4	83.65
8.267	0.142	0.992	1.27	114.25	6.307	19.56	145.52	123.4	84.07
9.851	0.072	0.985	0.99	149.38	6.307	19.56	147.67	123.4	82.28
10.631	0.060	0.976	0.84	179.48	6.307	19.56	150.67	123.4	79.92
11.983	0.056	0.960	0.72	209.52	6.307	19.56	151.77	123.4	78.06
13.377	0.053	0.937	0.646	239.54	6.307	19.56	154.80	123.4	74.70
15.065	0.051	0.912	0.600	264.52	6.307	19.56	158.59	123.4	70.98

No−load Power:

140 mW at 90 Vac

450 mW at 230 Vac.

Start−up

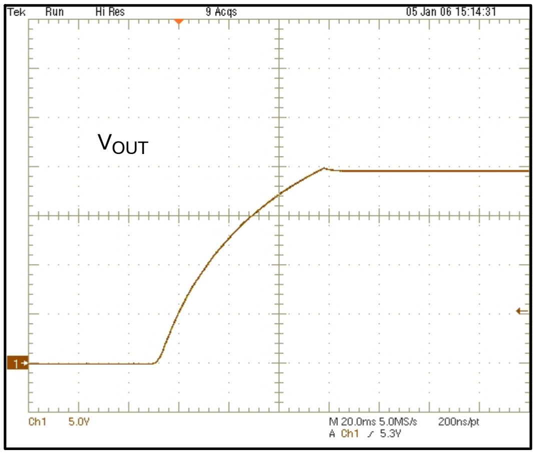


Figure 3. Start−up at 230 VAC

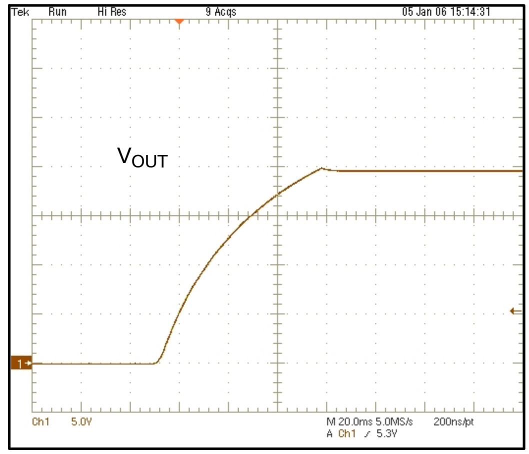


Figure 4. Start−up at 110 VAC

Load Transient

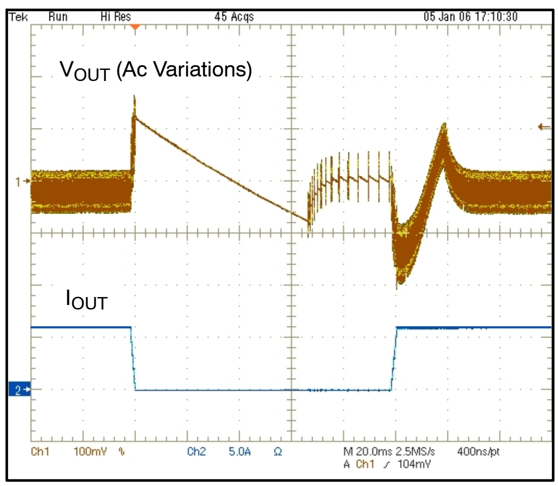


Figure 5. Load Dump from 100% to No−load

Short−circuit

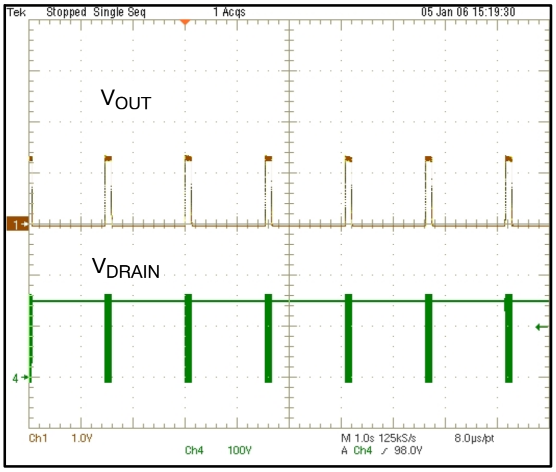


Figure 6. Short−circuit Burst Mode

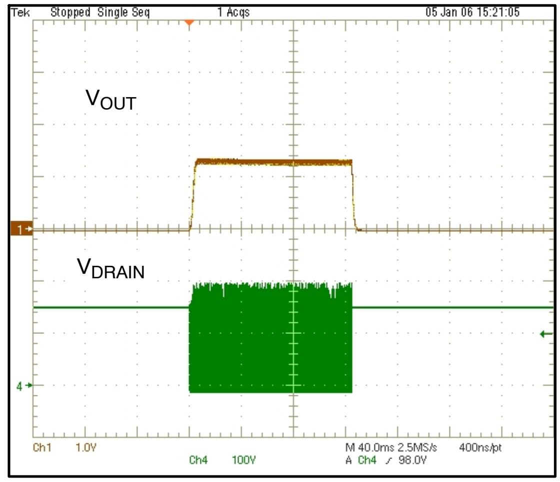


Figure 7. Detail of a Short−circuit Burst

Skip

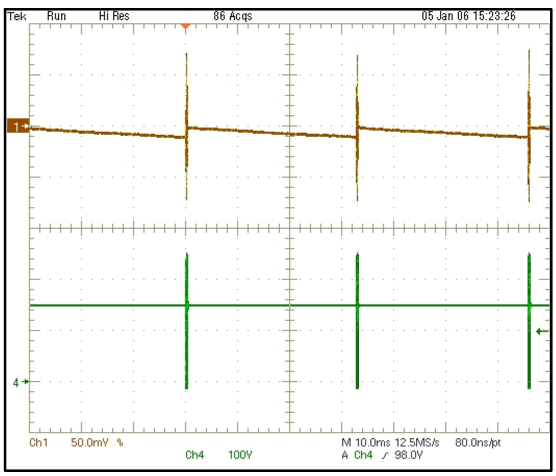


Figure 8. Skip Mode

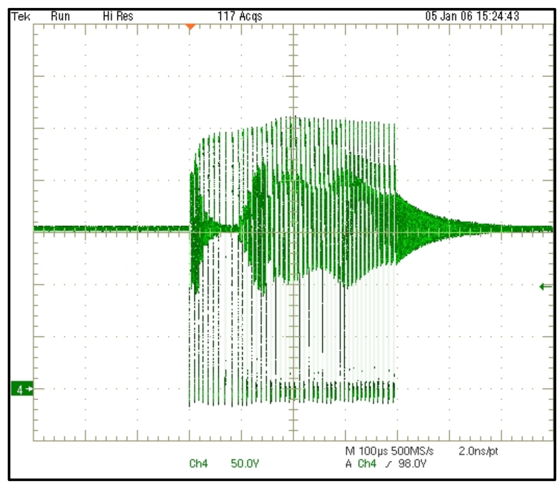


Figure 9. Detail of a Skip Burst

PCB Layout

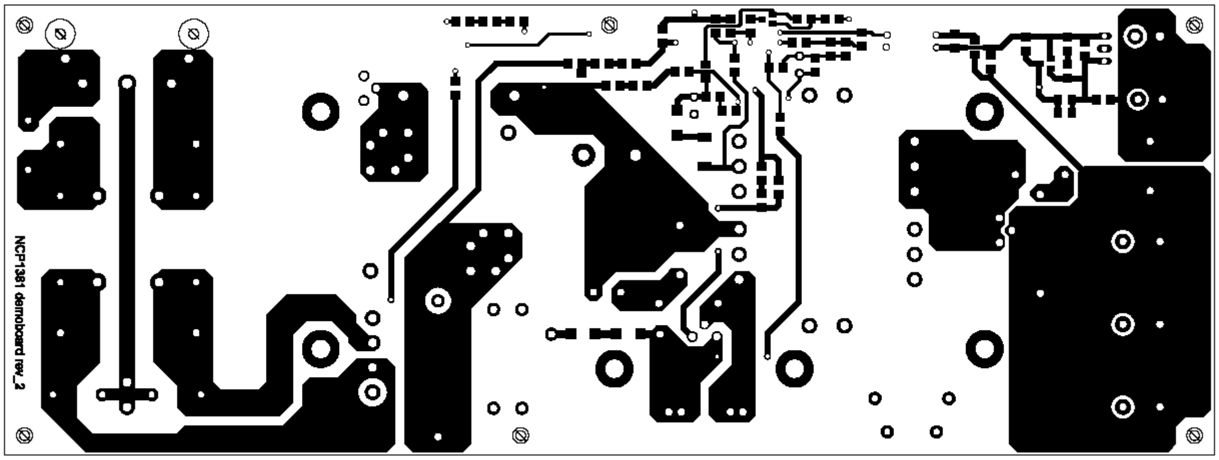


Figure 10. Solder Side (bottom view)

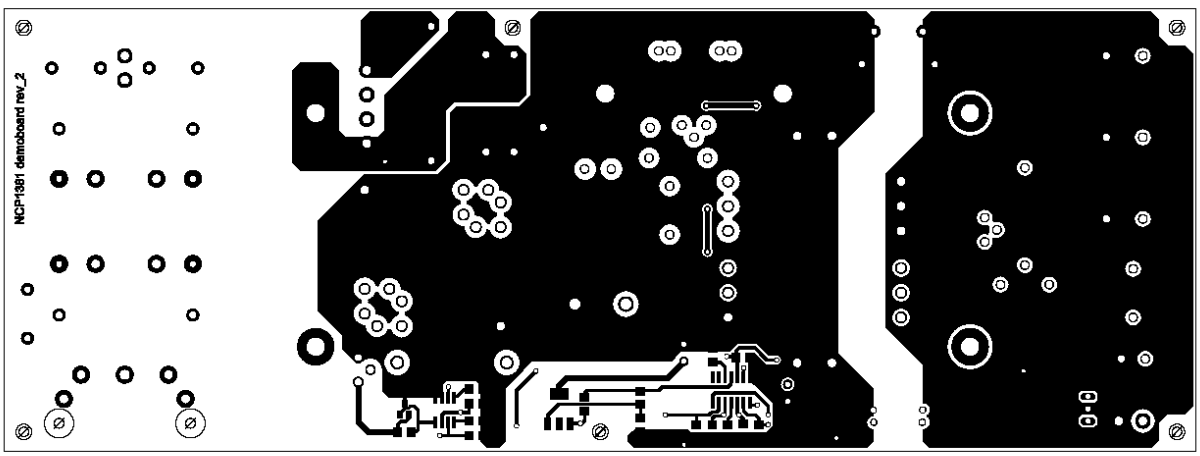


Figure 11. Top Side (top view)

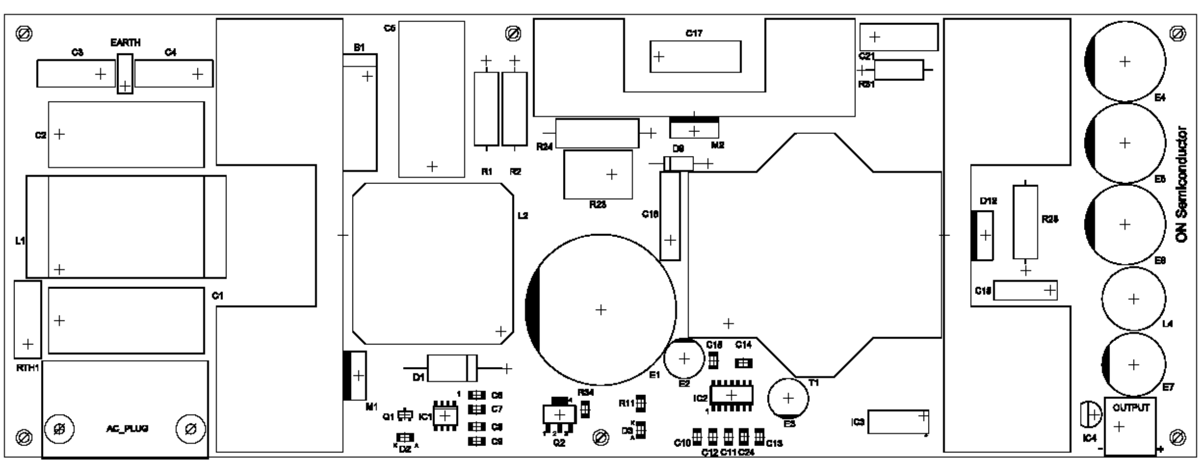


Figure 12. Top View of Component Side

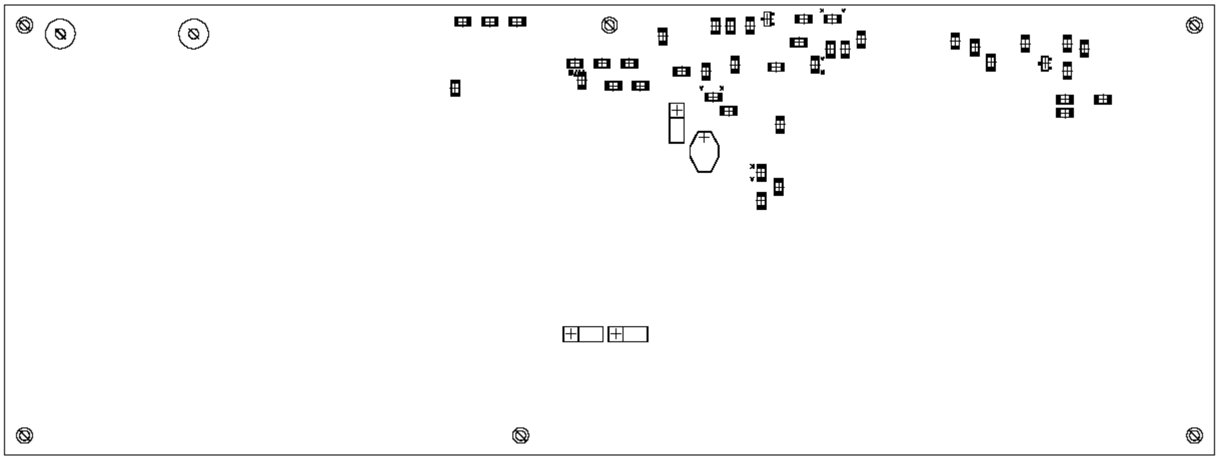


Figure 13. Bottom View of Solder Side (SMD Components)

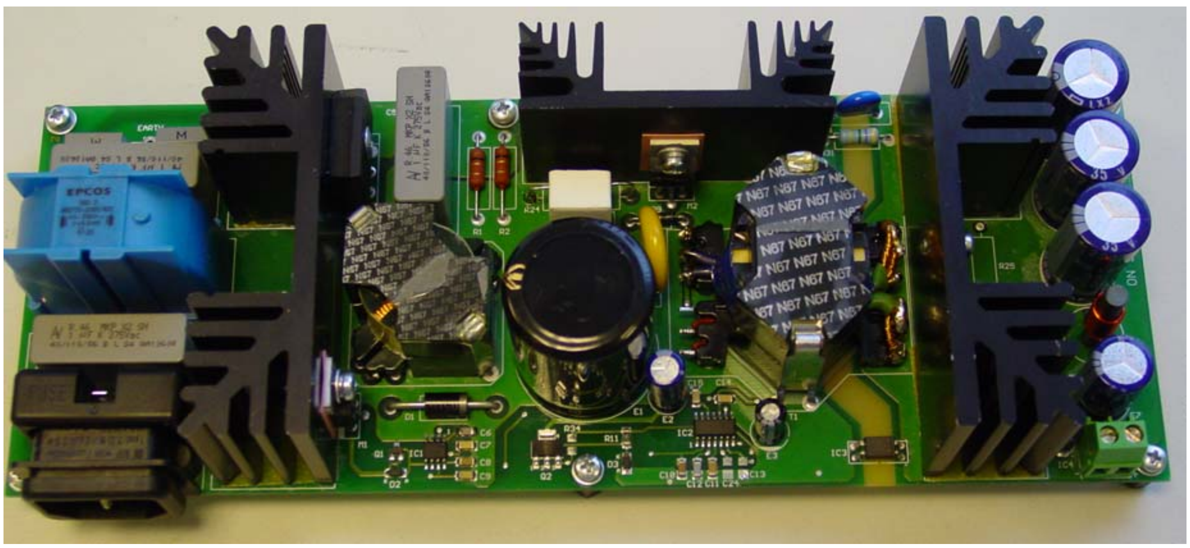


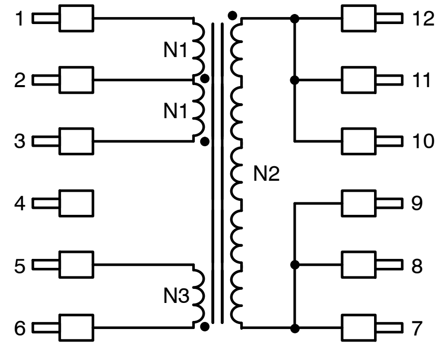
Figure 14. Board Picture

Table 1. BILL OF MATERIALS

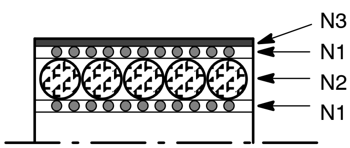
Part	Value	Package
B1	KBU810	
C01	1 μ/X2	
C02	1 μ/X2	
C03	2n2/Y2/X1	
C04	2n2/Y2/X1	
C05	1 μ/X2	
C06	470 p	C1206
C07	100 n	C1206
C08	220 n	C1206
C09	2n2	C1206
C10	1 μ	C1206
C11	330 n	C1206
C12	33 p	C1206
C13	NU	C1206
C14	100 n	C1206
C15	100 n	C1206
C16	10 n	
C17	470 p	
C18	NU	
C19	39 n	C1206
C20	NU	
C21	2n2n/Y1/X1	
C22	100 p	
C23	1 n	
C24	NU	
C25	220 n	
D01	MUR460	
D02	MMSD4148T1	
D03	15 V	
D04	NU	
D05	18 V	
D06	MURA120	
D07	MMSD4148	
D08	MMSD4148	
D09	MUR1100E	
D10	MRA4007	
D11	MRA4007	
D12	MBR20200	
E1	220 μ/450 V	
E2	220 μ/35 V	
E3	33 μ/63 V	
E4	2200 μ/35 V	
E5	2200 μ/35 V	
E6	2200 μ/35 V	
E7	220/63 V	
F1	T2A	
IC1	MC33260	
IC2	NCP1381/82	
IC3	PC817	
IC4	TLV431	

Part	Value	Package
L1	6,3 mH	
L2	200 μH	
L3	15 μH	
L4	2,2 μH	
M1	SPP11N60C2	
M2	SPP11N60C2	
Q1	BC807	
Q2	BCP56T1	
Q3	NU	
R01	1R	2W
R02	1R	2W
R03	20 k	R1206
R04	560 k	R1206
R05	680 k	R1206
R06	680 k	R1206
R07A	NU	
R07B	560 k	R1206
R08	910 k	R1206
R09	910 k	R1206
R10	10 k	R1207
R11	5k6	R1206
R12	100 k	R1206
R13	22 k	R1207
R14	NU	
R15	NU	
R16	2k2	R1206
R17	270 k	R1206
R18	270 k	R1206
R19	270 k	R1206
R20	2k7	R1206
R21	47R	R1206
R22	22R	R1206
R23	10 k	R1206
R24	0,12R	
R25	NU	
R26	1 k	R1206
R27	36 k	R1206
R28	5k6	R1206
R29	56 k	R1206
R30	75 k	R1206
R31	4M7	
R32	NU	
R33	NU	
R34	NU	
R35	2k2	R1206
R36	6k2	R1206
R37	27 k	R1206
R38	1 k	R1206
RTH1	strapped	
T1	Transformer	

TRANSFORMER CONSTRUCTION



Transformer Type: RM14
Material: N67
Marking: B65888−C1512−T1



N1 — 11 turns of multiwire 20 x ϕ0,2 mm 3 kV isolation
N2 — 5 turns of 5 paralleled multiwires 25 x ϕ0,2 mm 3 kV isolation
N1 — 11 turns of multiwire 20 x ϕ0,2 mm 1.5 kV isolation
N3 — 8 turns of wire ϕ0,2 mm

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