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Low Latency Driver to Access External EEPROM Using PIC18 Family Devices

Authors: *Obul Reddy and Ganesh Krishna S.M*
Microchip Technology Inc.

INTRODUCTION

This application note is developed based on low latency design. It provides an algorithm, which is designed to use the SPI/I^{2}C™ interrupts, to achieve the required communication and enable optimum processor usage. The algorithm is developed based on the PIC18 Master Synchronous Serial Port (MSSP) module with external Serial Peripheral Interface (SPI) EEPROMs and I^{2}C EEPROMs, respectively. The algorithm uses an interrupt driven approach.

OVERVIEW OF LOW LATENCY DESIGN

The low latency design relies on the communication interrupts provided by the PIC® MCUs to extract maximum performance from the microcontroller. This design can be better understood by first investigating the conventional approach and its disadvantages in the following sections.

Existing Conventional Approach

The conventional approach is to write blocking routines that do not relinquish control when they are awaiting an external event. The blocking routines are merely polling for flags to get triggered by the hardware. Therefore, the microcontroller is always busy with execution while waiting for a flag to get triggered.

In SPI mode, the microcontroller is always busy monitoring the Buffer Full (BF) flag/status bit of the MSSP Status (SSPSTAT) register during communications between the PIC MCU and external serial EEPROMs. In I^{2}C mode, the BF status bit gets cleared during transmission, and gets set during reception.

Disadvantages of Conventional Approach

External EEPROM chips, connected via SPI or I^{2}C, tend to consume a lot of microcontroller throughput to communicate. The routines accessing the EEPROM will have to wait until the communication is reliably completed. During this period, the microcontroller remains idle when it can actually be performing other tasks. The applications developed using the conventional approach do not allow the microcontroller to perform other tasks parallely. As this approach requires continuous and dedicated monitoring of the task, it degrades the performance and throughput of the microcontroller by wasting clock cycles.

LOW LATENCY DESIGN

The limitations of the conventional approach can be overcome by following the low latency approach. As the MSSP module comprises both SPI and I^{2}C modes, the microcontroller can operate in one of the two modes (either in SPI or I^{2}C). There is no need to poll the BF status bit continuously as this design uses the interrupt flag (i.e., MSSP Interrupt Flag bit – SSPIF) provided by the MSSP hardware module.

Note:	The MSSP module in PIC18 can be configured to use either the SPI or I^{2}C module.

As soon as the transmission/reception is completed, the SSPIF interrupt flag gets triggered by the hardware and vectors to the Interrupt Service Routine (ISR). To achieve this, the MSSP module interrupt must be enabled along with the global interrupt enable. Thus, communication happens in the background inside the ISR. This, in turn, reduces the load on the microcontroller and enables other tasks to run in a pseudo parallel control flow.

The low latency design is comprised of the following software stacks:

- SPI Software Stack – Comprises Application Layer, EEPROM Driver Layer, SPI Driver Layer and Hardware Layer
- I^{2}C Software Stack – Comprises Application Layer, EEPROM Driver Layer, I^{2}C Driver Layer and Hardware Layer

IMPLEMENTATION

SPI Software Stack

In this implementation, the MSSP module is configured as SPI and is interfaced with Microchip's 25XXX series SPI serial EEPROM device.

Figure 1 displays the layer-wise SPI software stack implementation.

Figure 2 displays the hardware schematic for the interface between the PIC18 MCU and Microchip's 25XXX series devices. The schematic provides the necessary connections between the microcontroller and the tested serial EEPROM; the software is written assuming these connections. The $\overline{WP}$ and $\overline{HOLD}$ pins are tied to V_{CC}, since these are not used in the software stack.

FIGURE 1: SPI SOFTWARE STACK

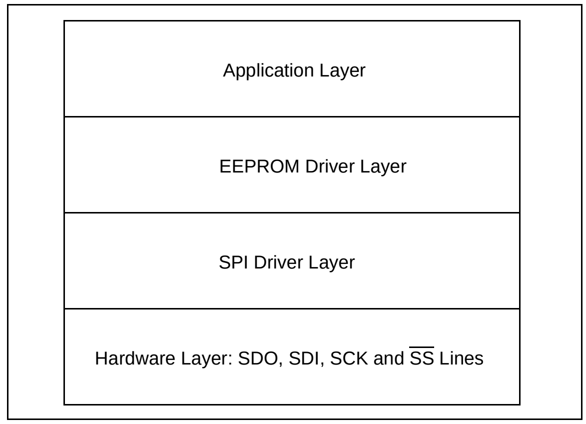
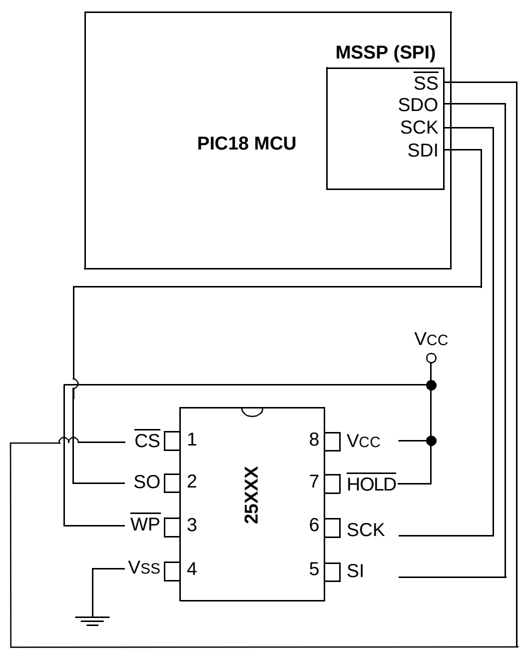


FIGURE 2: CIRCUIT FOR PIC18 MCU AND 25XXX SERIES DEVICE



I²C Software Stack

The MSSP module is configured as I²C and is interfaced with Microchip's 24XXX series' I²C serial EEPROM device.

Figure 3 displays the hardware schematic for the interface between the PIC18 MCU and Microchip's 24XXX series devices. The schematic provides the connections necessary between the microcontroller and the serial EEPROM; the software is developed assuming these connections. As the SDA and SCL pins are open-drain terminals, they require pull-up resistors to VCC (typically, 10 kΩ for 100 kHz and 2 kΩ for 400 kHz and 1 MHz). The $\overline{WP}$ pin is tied to ground as the write-protect feature is not used in the software stack provided.

FIGURE 3: CIRCUIT FOR PIC18 MCU AND 24XXX SERIES DEVICE

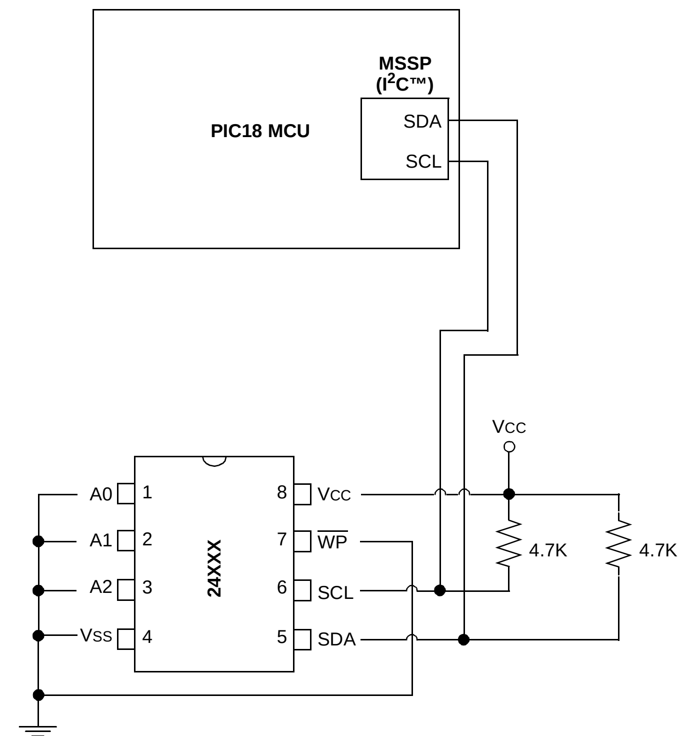
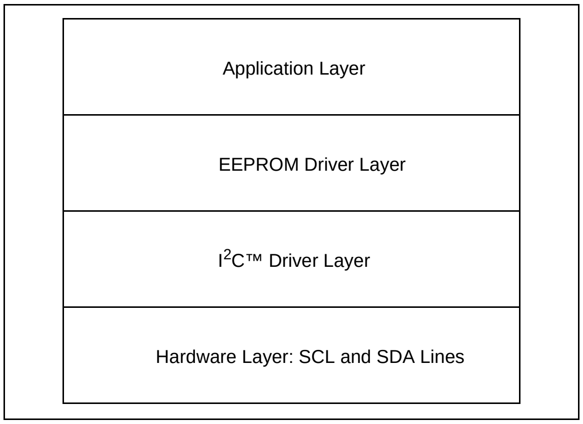


Figure 4 displays the layer-wise I^{2}C software stack implementation.

FIGURE 4: I^{2}C™ SOFTWARE STACK



FIRMWARE

- SPI Module – The source code consists of three files (`main.c`, `ee_drv.c` and `spi_drv.c`), which fit into the corresponding layers based on file operation.
- I^{2}C Module – The source code consists of three files (`main.c`, `ee_drv.c` and `i2c_drv.c`), which fit into the corresponding layers based on file operation.

APPLICATION LAYER

The application layer (`main.c`), in both SPI and I^{2}C modes, consists of API calls to initialize, write, read and verify the SPI and I^{2}C EEPROM devices. The main API calls are `EE_Init()`, `EE_Write()`, `EE_Read()` and `EE_Verify()`. The other two APIs associated with the main APIs are `EE_Status()` and `EE_Task()`. API `EE_Status()` returns the current status of the EEPROM operation. API `EE_Task()` updates the EEPROM with respect to the operation of the main API and the current status of EEPROM.

EEPROM DRIVER LAYER

The application APIs are defined in the EEPROM driver layer (`ee_drv.c`). API, `EE_Init()`, initializes the EEPROM, `EE_Write()` writes the requested number of bytes to the given EEPROM address, `EE_Read()` reads the requested number of bytes from the given EEPROM address and `EE_Verify()` verifies the number of bytes against the contents of EEPROM at the given address. API, `EE_Status()`, returns the current status of the EEPROM operation and must be called before each read/write to ensure that the driver is free. It must be called after every read to ensure that the data has been successfully copied to the user's space.

API, `EE_Task()`, is implemented as the main (high-level) EEPROM driver. The driver runs through different states to get the SPI/I^{2}C EEPROM read/write done using the low-level SPI/I^{2}C driver.

- SPI Driver

  The SPI driver chops the EEPROM writes into page sizes. The driver waits until the EEPROM chip is ready between consecutive page writes by reading the Write-In-Process (WIP) bit of the status register in the EEPROM. The WIP bit indicates whether the EEPROM is busy with an internal write operation. The driver resets the EEPROM in case of errors.

- I^{2}C Driver

  The I^{2}C driver chops the EEPROM writes into page sizes. The driver waits until the EEPROM chip is ready between consecutive page writes by polling the EEPROM device. The Acknowledgement (ACK) polling between page writes is required to determine whether the external EEPROM device is busy with its internal write operation. The driver also resets the EEPROM device in case of errors.

LOW-LEVEL DRIVER LAYER

- SPI Driver Layer (`spi_drv.c`) – It initializes the SPI module (`SPI_Init()`), disables the module and re-enables it in case of errors (`Reset_EE_Chip()`), and implements the low-level SPI driver. The low-level SPI driver is a semi-generic state machine implemented as an ISR, which goes through the necessary states to construct an SPI frame. In case the interrupts are shared among different modules, this routine must be called when the root ISR spots that SSPIF is set.
- I^2C Driver Layer (`i2c_drv.c`) – It initializes the I^2C module (`I2C_Init()`), disables the module and re-enables it in case of errors (`Reset_EE_Chip()`), and implements the low-level I^2C driver. Like the SPI driver, the low-level I^2C driver is a semi-generic state machine implemented as an ISR, which goes through the necessary states to construct an I^2C frame. If the interrupts are shared among different modules, this routine must be called when the root ISR spots that SSPIF is set.

HARDWARE LAYER

- SPI Module – Whenever the MSSP module is enabled and configured for SPI mode in the device, it configures the SCK, SDO, SDI and $\overline{SS}$ pins as serial port pins. These pins are used by the MSSP hardware module during SPI communications.
- I^2C Module – Whenever the MSSP module is enabled and configured for I^2C Master mode in the device, it configures the SCL and SDA pins as serial port pins. In Master mode, the SCL and SDA lines are used by the MSSP hardware during I^2C communications.

LATENCY DETAILS

- SPI Driver – Table 1 provides the latency details based on an oscillator frequency of 10 MHz for 1-byte write, read and verify.

TABLE 1: LATENCY DETAILS FOR SPI DRIVER

Fosc = 10 MHz			
API	**Performance Time (μs)**	**Performance Time (μs) (Fosc with PLL)**	**Comments**
`EE_Init()`	18	4.4	Main API
`EE_Task()`	11.2	2.8	Associated API
`EE_Write()`	296	74	Main API
`EE_Task()`	20	5	Associated API
`EE_Read()`	168	42	Main API
`EE_Task()`	12.6	3.2	Associated API
`EE_Verify()`	180	46	Main API
`EE_Task()`	12.8	3.2	Associated API

- I²C Driver – Table 2 provides the latency details based on an oscillator frequency of 10 MHz for 1-byte write, read and verify.

TABLE 2: LATENCY DETAILS FOR I²C™ DRIVER

FOSC = 10 MHz			
API	**Performance Time (μs)**	**Performance Time (μs) (FOSC with PLL)**	**Comments**
`EE_Init()`	15.6	3.9	Main API
`EE_Task()`	28.8	7.2	Associated API
`EE_Write()`	94	23.2	Main API
`EE_Task()`	11.6	2.9	Associated API
`EE_Read()`	94	23.6	Main API
`EE_Task()`	10.8	2.7	Associated API
`EE_Verify()`	110	27.2	Main API
`EE_Task()`	10.8	2.7	Associated API

API DETAILS

EE_Init()

Initializes the MSSP module and the external EEPROM chip.

Syntax

```
void EE_Init (void)
```

Parameters

None

Return Values

None

Example

```
void main(void)
{

    // Function to initialize the MSSP and external EEPROM
    EE_Init();
    while (EE_Status() == EE_BUSY)
    {
        EE_Task();
        // Perform any other task here
    }
}
```

EE_Write()

Writes the requested number of bytes to the given EEPROM address.

Syntax

```
void EE_Write(unsigned int address, unsigned char *data, unsigned int numbytes)
```

Parameter

`address` – Address on EEPROM chip to write to

`data` – Location from where data must be copied

`numbytes` – Number of bytes to be written

Return Values

None

Example

```
unsigned int Address = 0x0000;
unsigned int Length = 6
unsigned char WriteString[6] = {0x1,0x2,0x3,0x4,0x5,0x6};

void main(void)
{
    // Function to write data into EEPROM
    EE_Write(Address, WriteString, Length);
    while (EE_Status() == EE_BUSY)
    {
        EE_Task();
        // Perform any other task here
    }
}
```

EE_Read()

Reads the requested number of bytes from the given EEPROM address.

Syntax

```
void EE_Read(unsigned char *data, unsigned int address, unsigned int numbytes)
```

Parameter

`data` – Location where the read data will be copied
`address` – Address on EEPROM chip to read from
`numbytes` – Number of bytes to read

Return Values

None

Example

```
unsigned int Address = 0x0000;
unsigned int Length = 6
unsigned char ReadString[6]   = {0,0,0,0,0,0};

void main(void)
{
   // Function to read data from EEPROM
   EE_Read(ReadString, Address, Length);
   while (EE_Status() == EE_BUSY)
   {
      EE_Task();
      // Perform any other task here
   }
}
```

EE_Verify()

Verifies contents of a buffer against the contents of the EEPROM.

Syntax

```
void EE_Verify(unsigned char *data, unsigned int address, unsigned int numbytes)
```

Parameter

`data` – Location of data bytes to verify against EEPROM contents
`address` – Address on EEPROM chip to verify from
`numbytes` – Number of bytes to verify

Return Values

None

Example

```
unsigned int Address = 0x0000;
unsigned int Length = 6
unsigned char VerifyString[6] = {0x1,0x2,0x3,0x4,0x5,0x6};

void main(void)
{
   EE_Verify(VerifyString, Address, Length);
   while (EE_Status() == EE_BUSY)
   {
      EE_Task();
      // Perform any other task here
   }
}
```

EE_Status()

Returns the current status of the EEPROM operation.

Syntax

`EE_Result_Type EE_Status (void)`

Parameter

None

Return Values

Returns current state of EEPROM module.

Example:

```
unsigned int Address = 0x0000;
unsigned int Length = 6
unsigned char WriteString[6] = {0x1,0x2,0x3,0x4,0x5,0x6};
typedef enum {EE_BUSY,EE_ERROR,EE_VERIFY_FAIL,EE_FREE}EE_Result_Type;

void main(void)
{
   EE_Write(Address, WriteString, Length);
   while (EE_Status() == EE_BUSY)
   {
      EE_Task();
      // Perform any other task here
   }
}
```

EE_Task()

This API runs through different states to get the SPI/I^{2}C EEPROM reads/writes done using the low-level SPI/I^{2}C driver, respectively.

Syntax

`void EE_Task (void)`

Parameter

None

Return Values

None

Example

```
unsigned int Address = 0x0000;
unsigned int Length = 6
unsigned char WriteString[6] = {0x1,0x2,0x3,0x4,0x5,0x6};

void main(void)
{
   EE_Write(Address, WriteString, Length);
   while (EE_Status() == EE_BUSY)
   {
      EE_Task();
      // Perform any other task here
   }
}
```

SPI Software Stack Control Flow

See Figure 5 for EEPROM driver control flow and Figure 6 for SPI driver control flow.

FIGURE 5: EEPROM DRIVER CONTROL FLOW

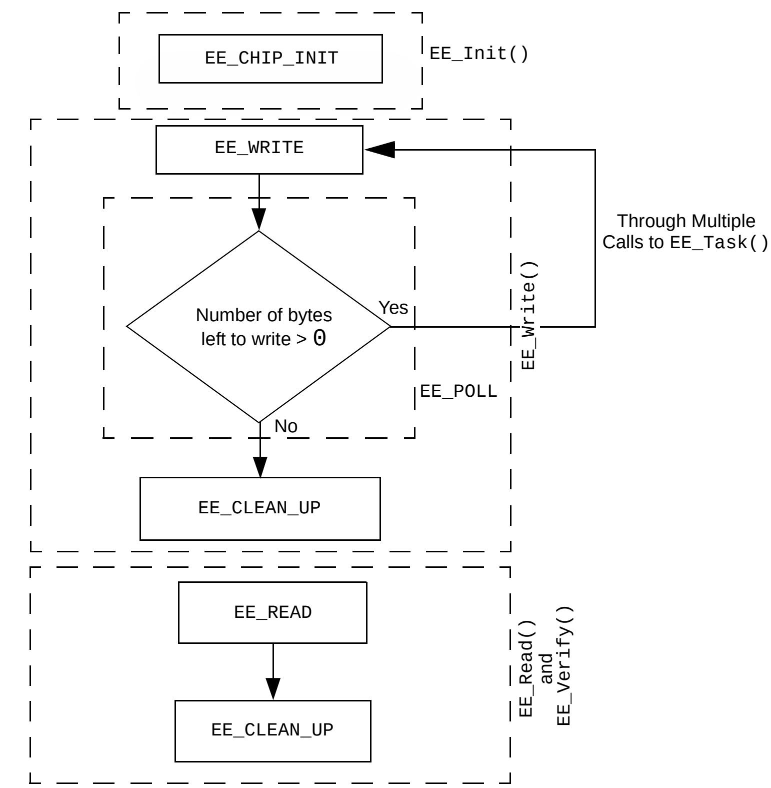
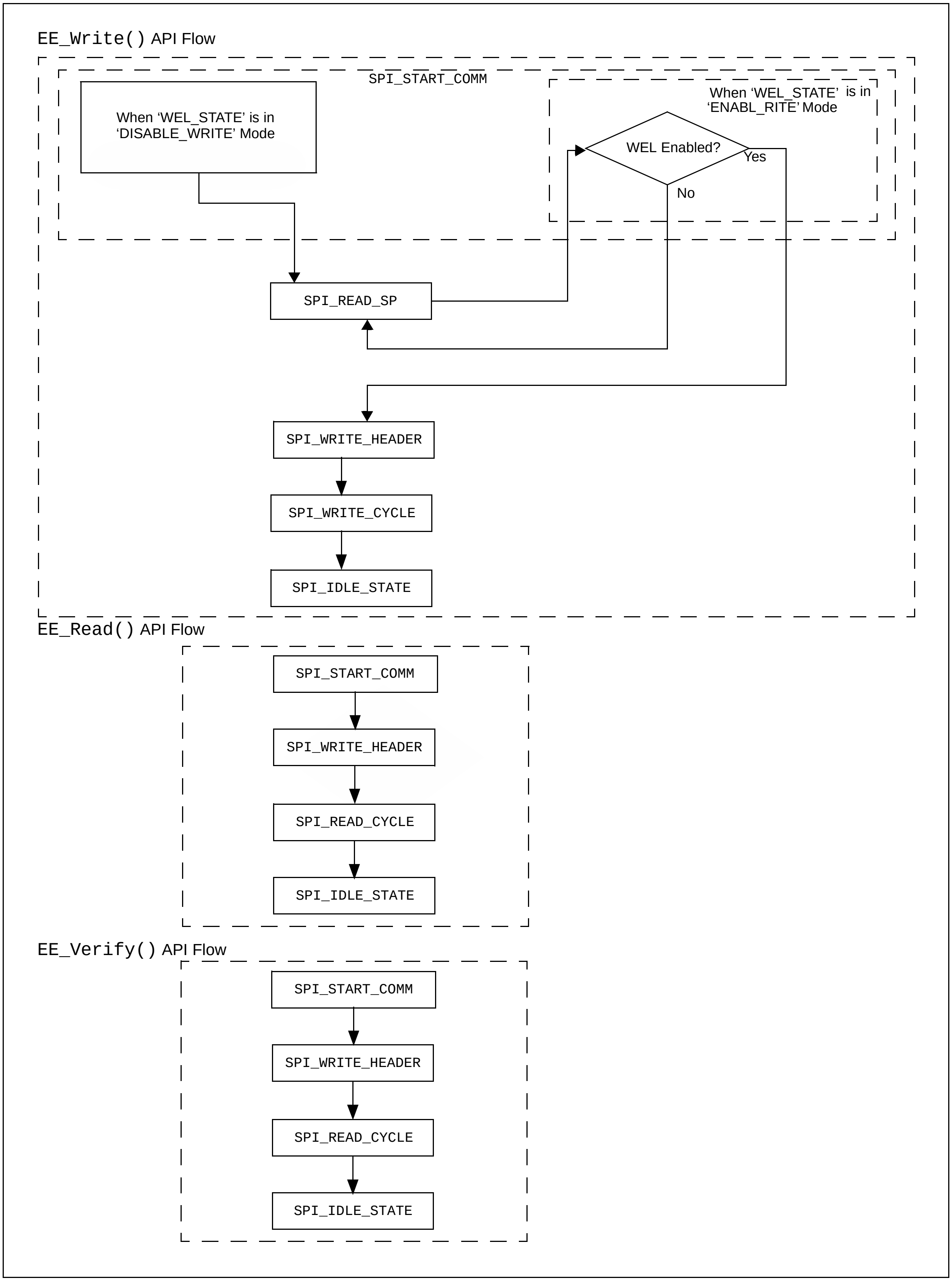


FIGURE 6: SPI DRIVER CONTROL FLOW



I²C Software Stack Control Flow

See Figure 7 for EEPROM driver control flow and Figure 8 for SPI driver control flow.

FIGURE 7: EEPROM DRIVER CONTROL FLOW

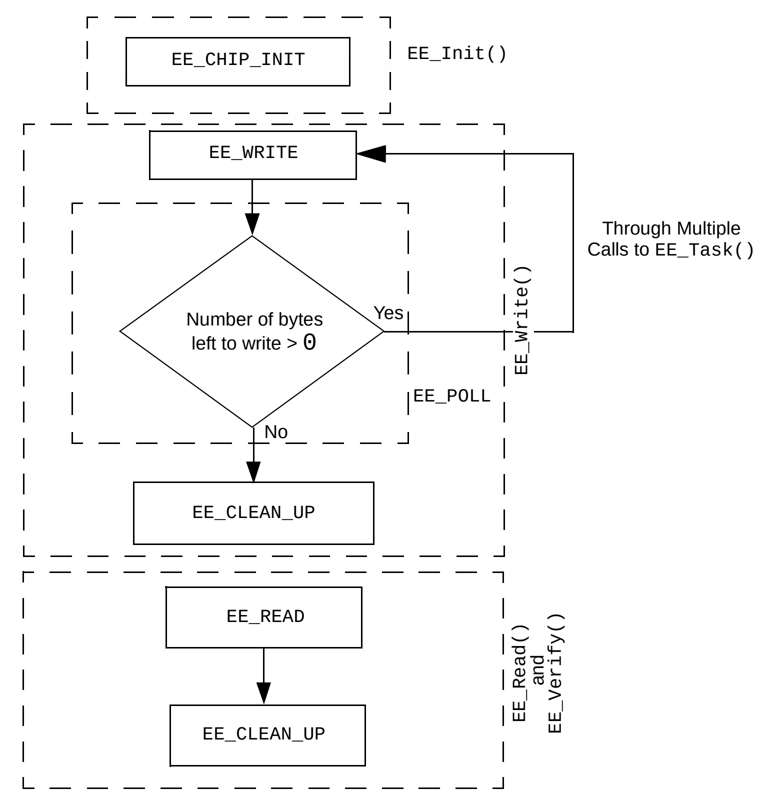
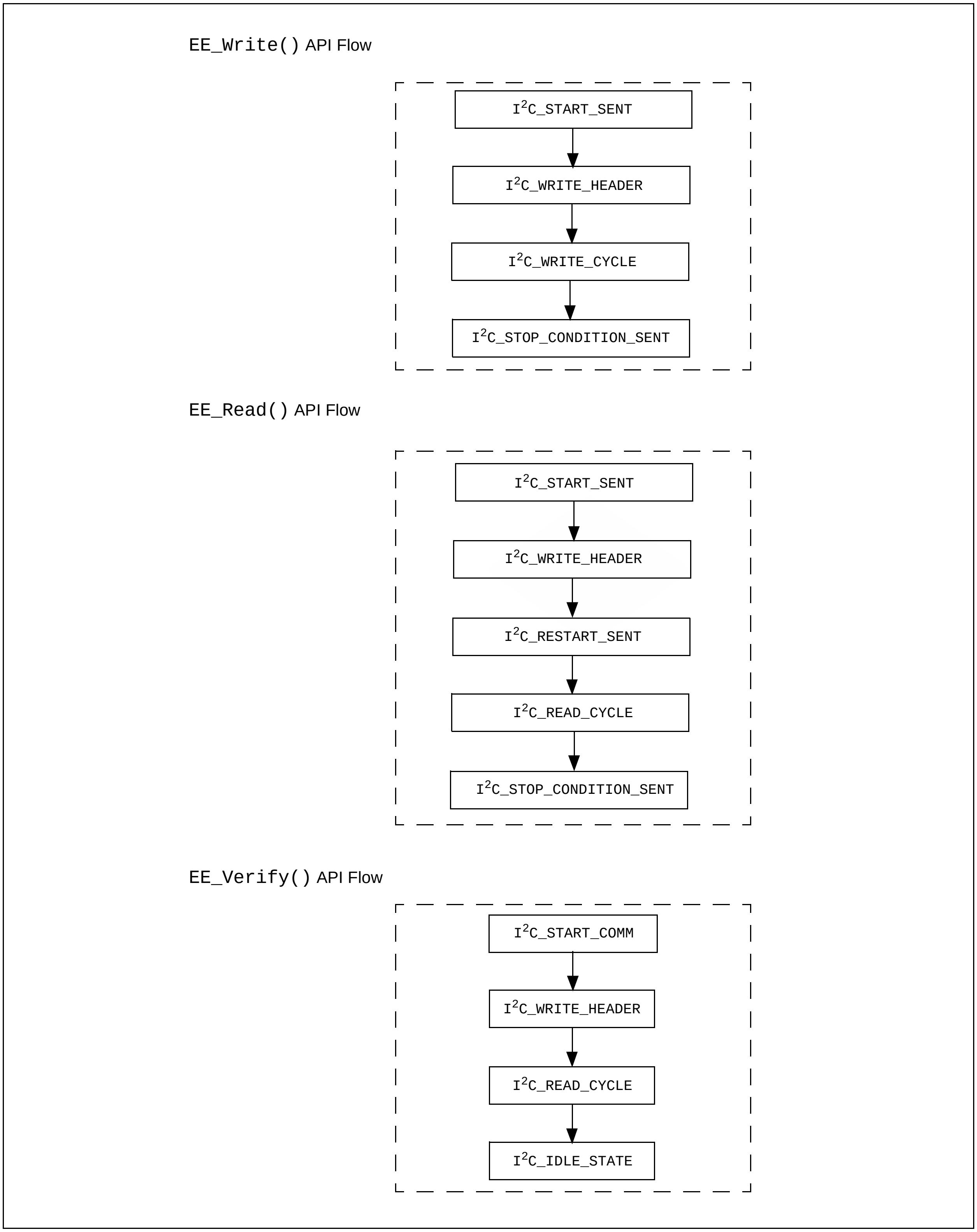


FIGURE 8: I^2C™ DRIVER CONTROL FLOW



CONCLUSION

This application note outlines an algorithm, which uses MSSP module interrupts available in the PIC18 family of devices, to overcome the limitations of the conventional approach by following the low latency design.

REFERENCES

- *AN1000, "Using the MSSP Module to Interface SPI Serial EEPROMs with PIC18 Devices"* – www.microchip.com
- *AN989, "Using the MSSP Module to Interface I^2C™ Serial EEPROMs with PIC18 Devices"* – www.microchip.com

APPENDIX A: LIBRARY DIRECTORY

TABLE A-1: LIBRARY DIRECTORY ORGANIZATION

Directory	Content
Low_Lat_DATAEE_soln:	
I^2C_solution	A Low Latency Data EEPROM Solution for I^2C™ EEPROM Chips
SPI_solution	A Low Latency Data EEPROM Solution for SPI EEPROM Chips

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