ST-NXP Wireless

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ST-NXP Wireless

AN10038

Interfacing the ISP1582 to the Intel PXA250 Processor

Rev. 03 — 14 August 2006 Application note

Document information

Info	Content
Keywords	isp1582, usb, universal serial bus, pxa250
Abstract	This document explains the interface between the ISP1582 and the Intel® Cotulla processor PXA250.

PHILIPS

Revision history

Rev	Date	Description
03	20060814	Third release. Updated Fig 1.
02	20050302	Second release. Updated Fig 1.
01	20040601	First release.

Contact information

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1. Introduction

This document explains interfacing the ISP1582 to the Intel Cotulla PXA250 processor.

2. Interfacing signals

The main ISP1582 signals to consider for connecting to an Intel Cotulla PXA250 processor are:

- A 16-bit data bus (DATA[15:0]) for the ISP1582.
- Eight address lines (A[7:0]) necessary for complete addressing of the ISP1582 internal registers.
- The CS_N line is used to select the ISP1582 in a certain address range of the host system. This input signal is active LOW.
- RD_N and WR_N are common read and write signals. These signals are active LOW.
- DMA channel standard control lines: DREQ, DACK, DIOR and DIOW.
- INT line: It is programmable type, level or edge, and polarity (active HIGH or LOW).
- The RESET_N signal is active LOW.

3. Interface block diagram

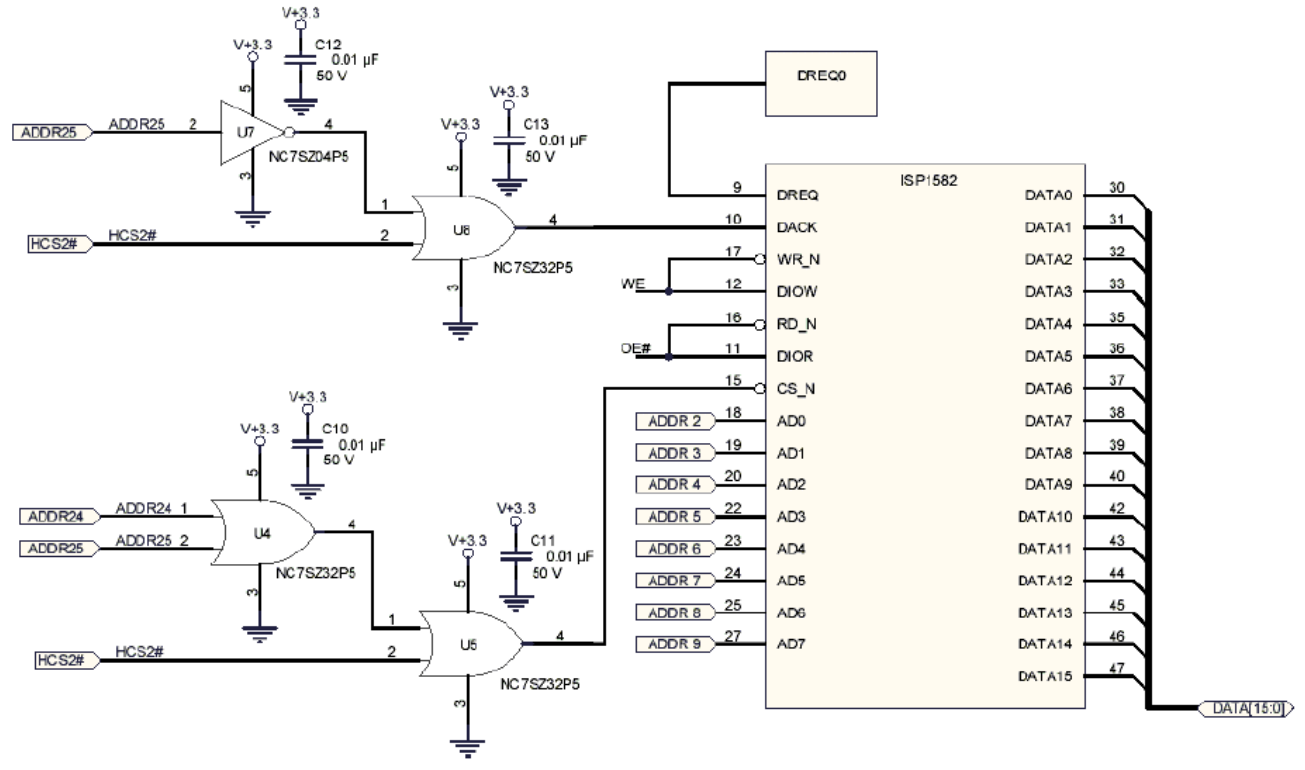

Fig 1. Interfacing block diagram

For Direct Memory Access (DMA) to the ISP1582 from the Cotulla chip, the following addresses are used. Using simple logic gates in between Cotulla and the ISP1582 can generate the required DACK signals.

Processor used: CS2#

PIO address map: 0000 0000h to 00FF FFFFh

DMA channel 0 address map: 0200 0000h to 02FF FFFFh

Remark: The DMA must be properly terminated before performing the PIO access, if there is an interrupt during DMA.

Remark: The ISP1582 register space is 8-bit aligned.

In Fig 1, it is assumed that Parallel I/O (PIO) and DMA use this memory spaces. You may choose a different configuration, depending on your requirement.

Fig 2 shows the PXA250 processor interface.

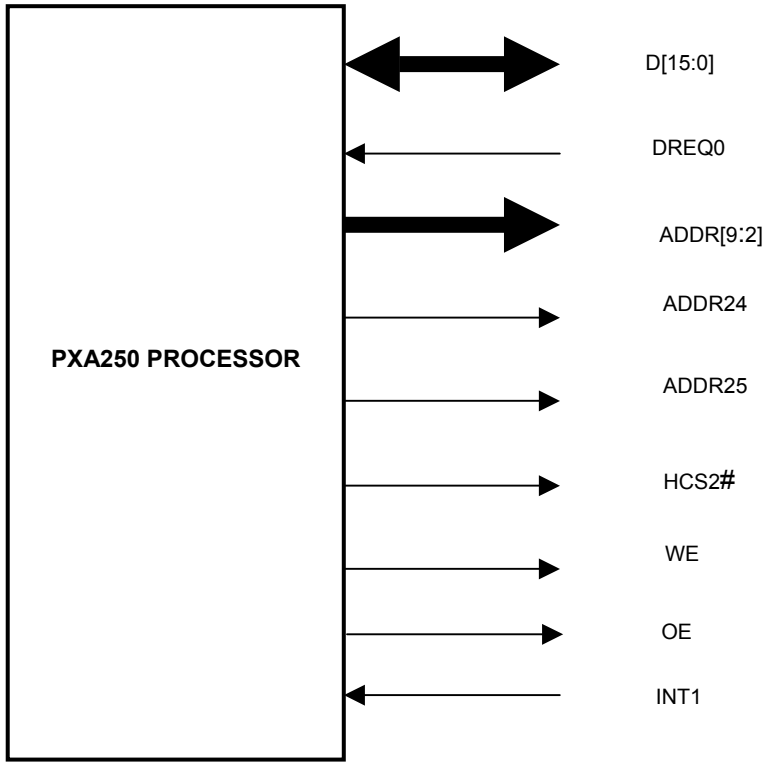

Fig 2. PXA250 processor

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Date of release: 14 August 2006
Document identifier: AN10038_3