AN1737
APPLICATION NOTE

PRIMARY OR SECONDARY MODE REGULATION PRINTER POWER SUPPLY USING VIPer53

John S. Lo Giudice

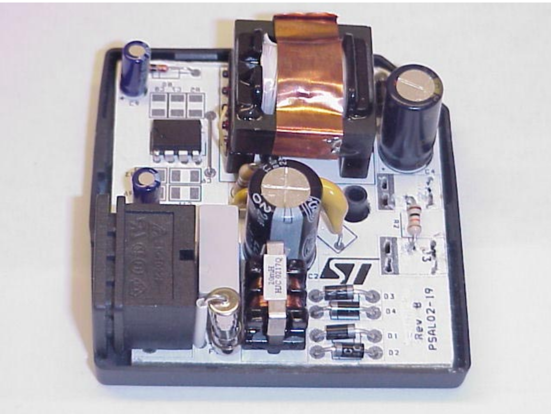
INTRODUCTION

The VIPer53 combines in the same package an enhanced current mode PWM controller with a high voltage MDMesh Power Mosfet. This application note describes the implementation of the VIPer53 in a printer power supply that has peak power requirements up to 45W. Since the VIPer53 has MOSFET that has a maximum R_{dson} of 1Ω max at 1A, the DIP-8 will handle the power requirements without an added heat sink. This can dramatically reduce the size of the power supply and increase reliability.

1. KEY FATURES OF THE VIPer53

- Switching frequency up to 300KHz
- Current mode control
- Soft start and shut down control
- Automatic burst control (Blue Angel Compliant)
- Auxiliary under voltage lockout with hysteresis
- High voltage startup current source
- Over temperature protection
- Overload control

Figure 1: Sample Board Layout



2. SCOPE

This paper will cover the design and the results for a universal input power supply for a printer application or similar device. It will describe two approaches.

One is primary mode regulation and the other secondary mode regulation.

Primary mode as pictured in figure 1 and schematic 1 uses the internal reference and error amplifier to regulate the output through the transformer coupling. For this method, transformer design is very critical to achieve good regulation of the output. The results reached for this application note were derived with the transformer designed by Cramer Coil and Transformer. This method achieved good regulation while saving the cost of an optocoupler and TL431 reference. Secondary mode gives excellent line, load regulation and transient response by directly sensing the output. This is shown in schematic 2. Depending on the design parameters and cost versus performance, a decision can be made after reviewing the results of this application note.

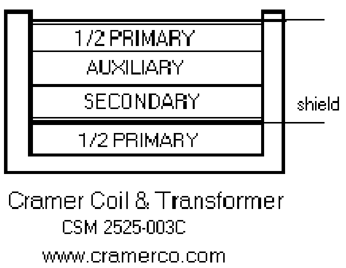
This application usually requires one DC output that provides power to the printer heads and motors. Then DC-DC converters step down that voltage to 5V for USB, 3.3V for logic and 2.5 or 1.8V for the microprocessor. The requirements for this power supply are for a 30V output at 0.8A continuous with peak currents of 1.5A while complying with Blue Angel.

Table 1: Electrical specification

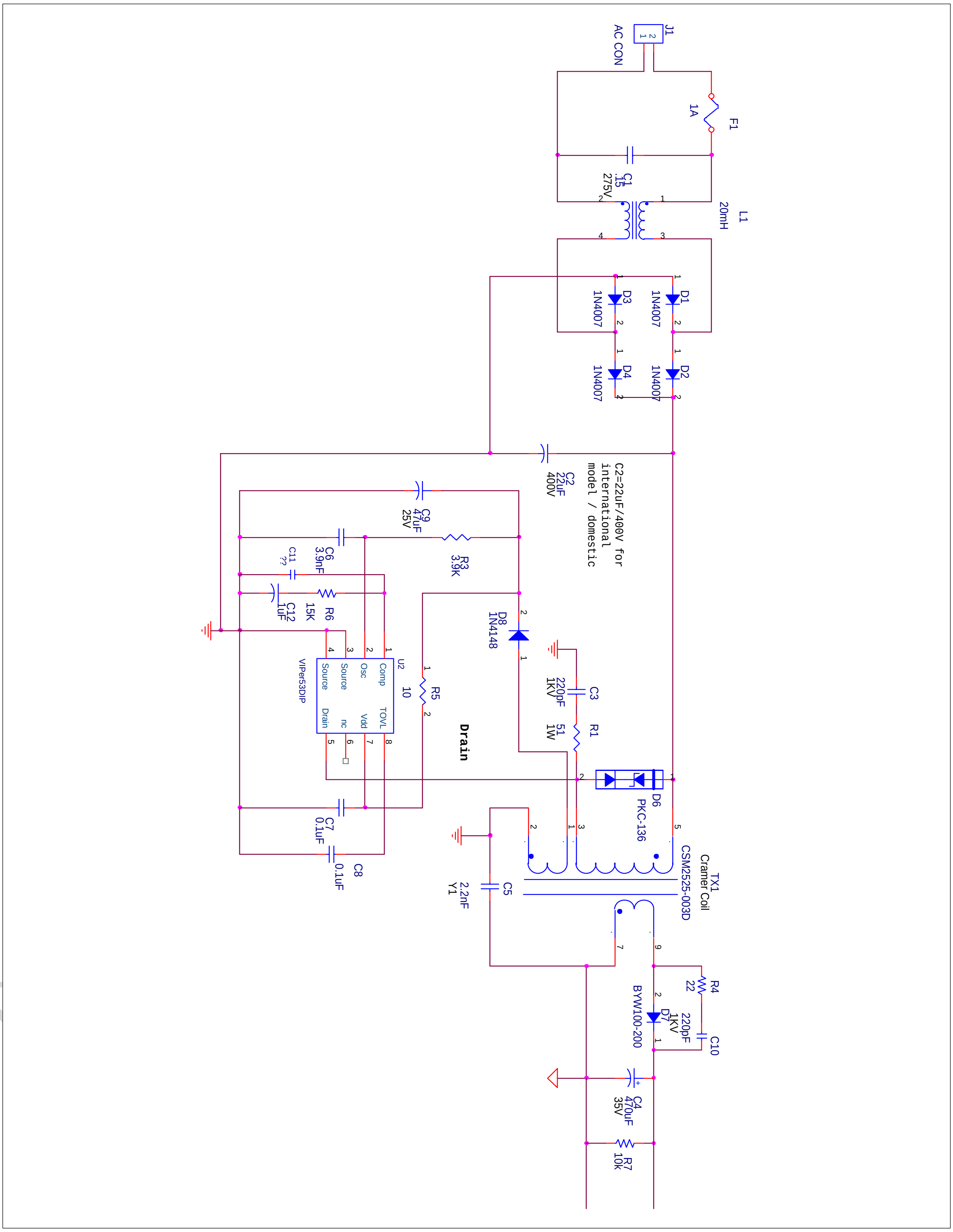
Parameter	Primary mode Results	Secondary mode Results
Input Voltage	90-264 Vac	90-264 Vac
Output	30V from 0 to 1.5A	30V from 0 to 1.5A
Line regulation from 110V to 230Vac	0.21%	0.00%
Load regulation from 0.1 to 0.8A	+/- 3.4%	0.0A to 0.8A +/- 0.02%
Load regulation from 0.1 to 1.5A	+/- 6%	0.0A to 1.5A +/- 0.05%
Efficiency	84.3%	83.5%
Output ripple voltage @ 0.8	100mv	100mv
Input power at no load (Blue Angel)	0.489 watts	0.496 watts
Output transient response 0.4A to 0.8A	+/- 730mv pk	+/- 87mv pk
EMI	EN55022 and FCC Class B	EN55022 and FCC Class B

Transformer Specification

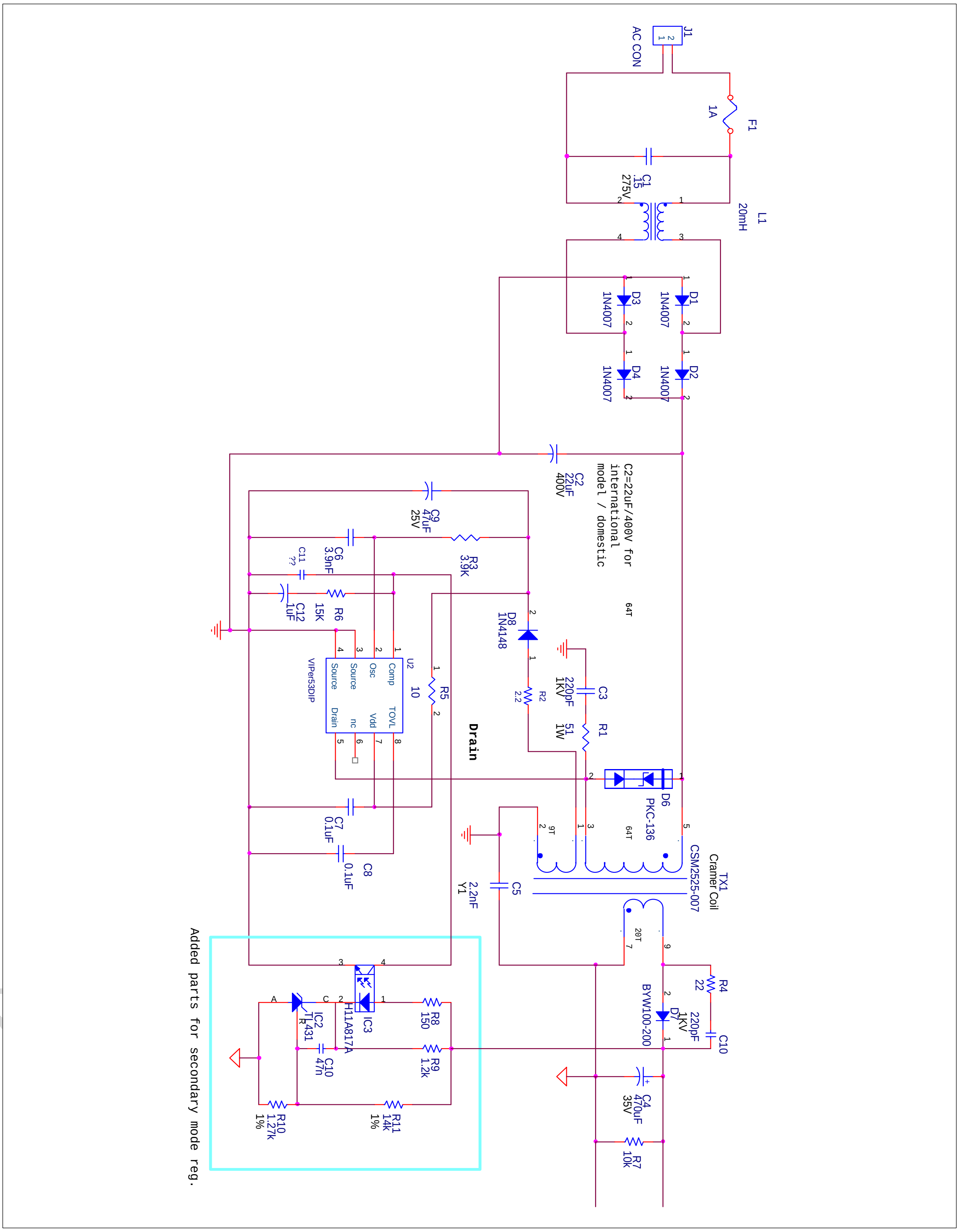
Primary inductance	410 µH
Primary Leakage inductance	6 µH typical
Core	EF25 PC40 Material



ELECTRICAL SCHEMATIC FOR PRIMARY MODE REGULATION



ELECTRICAL SCHEMATIC FOR SECONDARY MODE REGULATION



3. GENERAL CIRCUIT DESCRIPTION

The VIPer53 can be controlled with secondary mode regulation, using a reference and an optocoupler to close the loop and isolate primary to secondary. The VIPer53 can also be designed for primary regulation. Since this power supply is used to supply a bulk voltage for motors and print head where the regulation does not have to be very tight, primary mode regulation was chosen to save the cost of a TL431 and an optocoupler. By designing the transformer for tight coupling, good regulation results can be obtained.

Primary mode regulation works by regulating the voltage at pin 7, the V_{dd} pin. The pin serves several functions. It is the power supply for the control circuit. It also provides an internal current source to charge the external capacitor during start up.

V_{dd} is controlled by four thresholds:

- V_{ddon} Typically 11.5V, the device starts switching.
- V_{ddoff} Typically 8.4V, the device stops switching.
- V_{ddovp} Typically 18V, Triggers over voltage protection.
- V_{ddreg} Regulation point when working in primary feedback mode.

In primary mode regulation, the V_{dd} output is considered the main output. This is regulated at 15V by the internal error amplifier circuitry of the VIPer53. The regulation of the secondary output of the power supply is dependent on the tight coupling of the transformer and the output impedance of the diode and circuit path. The stack shown above gives the best cross regulation results by keeping the high current winding closer to the core. The primary is split between the first and last winding, (sandwiched), to reduce leakage inductance and improve regulation. Reduced leakage minimizes ringing on the drain of the internal MOSFET, thus reducing snubber dissipation and lowering conducted noise. Secondary mode regulation can be used by adding a TL431 and optocoupler. See schematic 2. The optocoupler is connected from the comp pin to ground. The output of the V_{dd} winding of the transformer is reduced by 1 turn to reduce the V_{dd} voltage lower than the internal 15V. The voltage should be centered on 12V. R2 is used to tweak the voltage between transformer turns. This lower V_{dd} voltage will saturate the internal error amplifier in the high state and because it is a transconductance amplifier, it will deliver a constant current of 600µA to the optocoupler transistor. A +/-0.02% regulation was achieved for a load change from 0.03A to 0.8A.

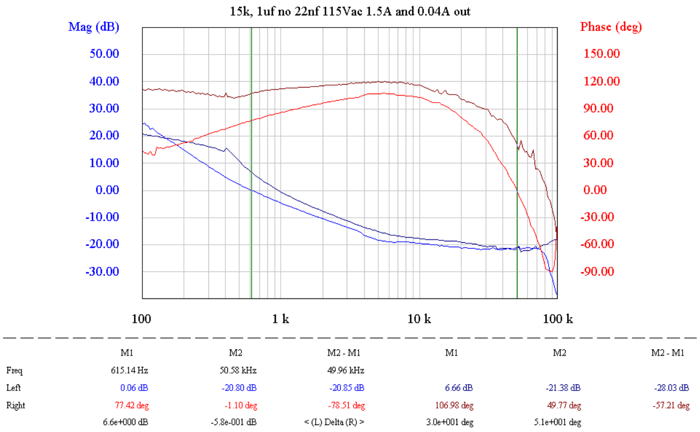
R3 and C6 set the switching frequency. In this case 100KHZ was chosen as a compromise for size, cost and temperature considerations.

A resistor and a capacitor in series, R6 and C12, are placed on the compensation pin, pin 1. This gives a zero to counteract the modulator output pole due to the output load and capacitor. Shown below in figure 2 is the Bode Plot of the primary mode regulation response taken at the V_{dd} output. The light blue is the gain, light red is the phase at 0.04A output. The dark blue is gain and the dark red is the phase for maximum load at 1.5A.

4. OPERATION AND TEST PERFORMANCE

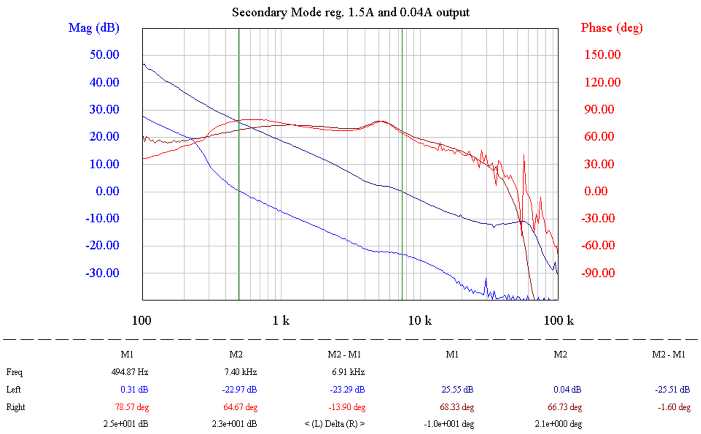
4.1 Bode plots

Figure 2: Bode plot for Primary mode regulation



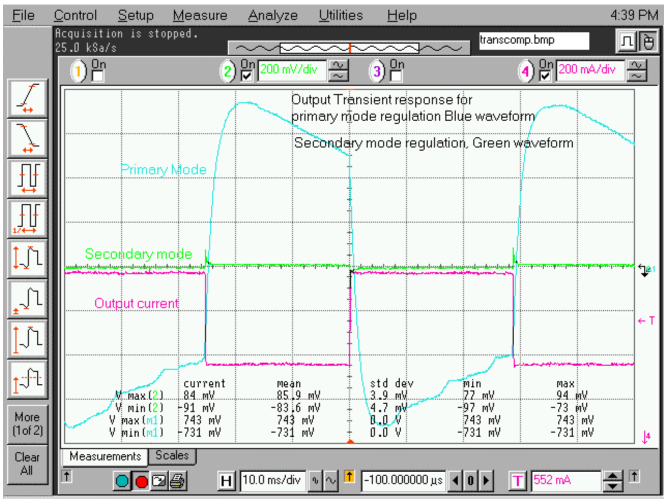
Load	Cross Over	Phase Margin	Gain Margin
Max Load	1 KHz	85°	20db
Min Load	615	77°	21db

Figure 3: Bode plot for Secondary mode regulation



Load	Cross Over	Phase Margin	Gain Margin
Max Load	7.4 KHz	64°	12db
Min Load	495	78°	40db

4.2 Transient Response



Primary mode resulted in a +/- 0.7V excursion for a 0.4A to 0.8A step load. For this 30V output it relates to a +/-2.3% over shoot.

Secondary mode regulation senses the output directly; it reacts more quickly and precisely. For the same excursion a +/- 0.09V was achieved with a settling time of 150 microseconds. Again performance versus cost must be weighed for the particular application. Figure 4 shows the output voltage swing for a current step from 0.4A to 0.8A. The blue waveform is the primary mode and on the same voltage scale the green is for secondary mode regulation.

4.3 Overload Protection

The T_{olv} pin allows the connection of an external capacitor for delaying the overload protection triggered when the comp pin is max, at 4.35V. When V_{comp} goes above this level, then C8, the capacitor connected to T_{olv} begins to charge. When it reaches 4V, the internal MOSFET driver is disabled and the power supply stops switching. V_{dd} pin does not receive any energy from the transformer and therefore starts discharging until it reaches V_{ddoff}, 8.4V, and the VIPer is reset. A new cycle begins by recharging the Vdd capacitor through the high voltage current source until it reaches 11.5V and the VIPer starts switching again. If the time duration for an overload exceeds the time set by the T_{olv} capacitor, then this cycle repeats indefinitely. This keeps the on time duty cycle small thus minimizing the dissipation during a short (see figure 4). The T_{olv} capacitor should be sized large enough to allow for the overload during start up when a lot of energy is pumped into charging the output capacitors. During startup, T_{olv} must have enough margin to keep it from reaching 4V (see figure 5).

Figure 4

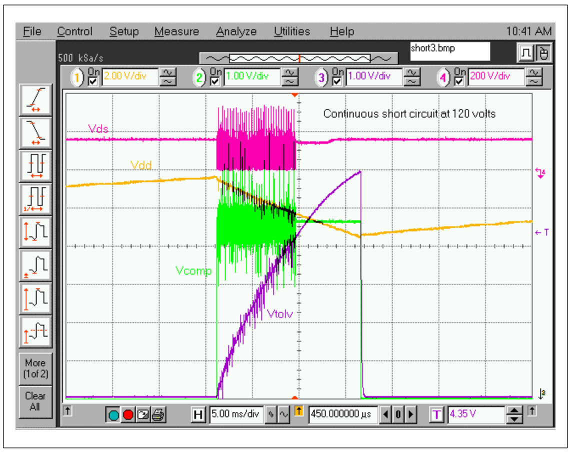
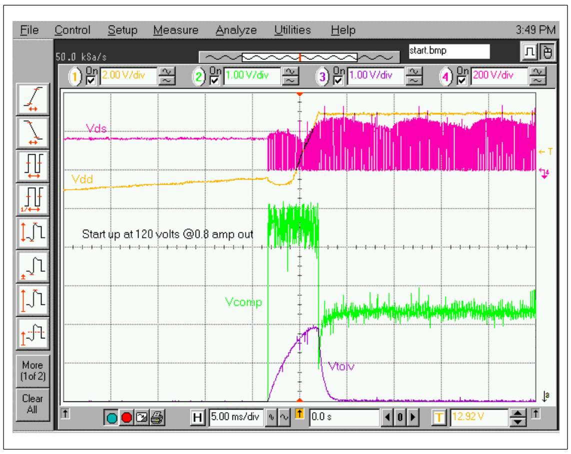


Figure 5



The transformer is designed for continuous mode. In discontinuous mode operation the transformer core is charged when the primary MOSFET is on. When the MOSFET turns off, the magnetic field reverses and current discharges through the secondary diode. The current reaches zero before the next cycle begins. In continuous mode, the transformer inductance is three times higher than the calculated discontinuous mode and therefore does not reach zero before the MOSFET turn on. This reduces the peak currents in the primary and secondary, reducing the RMS heating effect on the VIPer53, the transformer and output diode. This also helps in the ripple current of the output capacitor. An RC snubber is placed across the output diode to reduce the ringing and reduce the EMI noise. In this design at high line minimum load the power supply runs in discontinuous mode and at low line maximum load it runs in deep continuous mode. Because of this, we are able to supply 45W of output power for short duration limited not by peak current but by temperature. That is to say that the peak currents will be below the maximum VIPer53 specification to deliver a peak power even for seconds without any damage to the power supply. The VIPer53 has an internal over temperature protection that will protect the power supply in case it is left in an overload condition.

4.4 Mode of Operation

Figure 6: Discontinuous mode

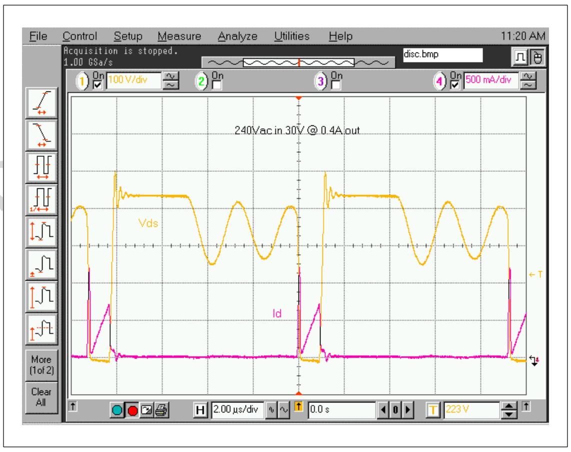
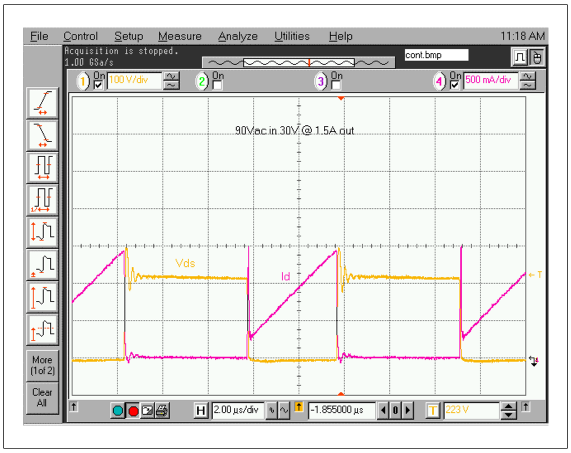


Figure 7: Continuous mode

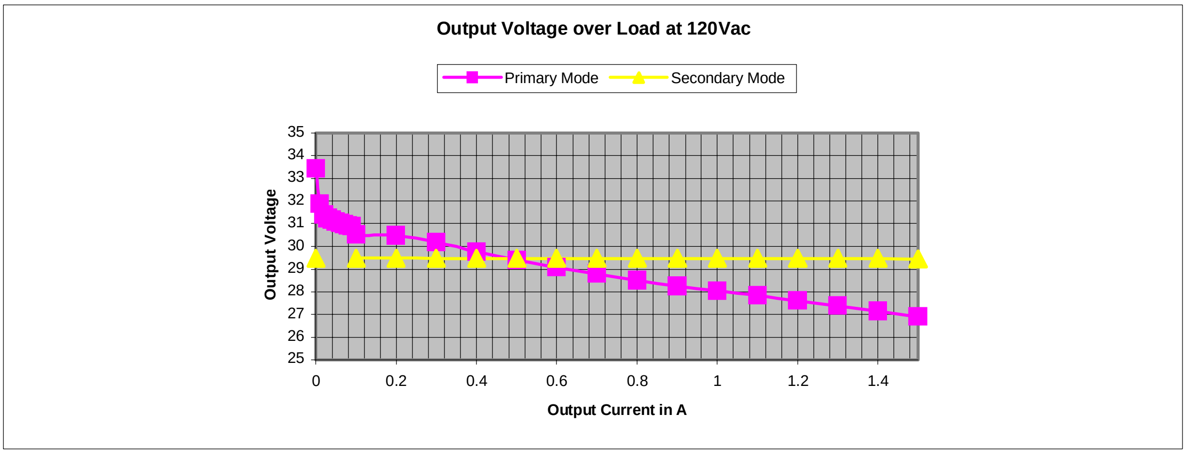


In figure 6 it can be seen that when the secondary current reaches zero, the transformer is left unloaded and rings out. This can be seen on the drain to source waveform. The first ringing after the MOSFET turns off is due to leakage inductance and the later is due to the discontinuous effect on the transformer.

5. PERFORMANCE COMPARISON

Following, is a comparison on the performance achieved for the two units. Again, keep in mind the cost saving for giving up a little bit of performance when supplying power to a load that is not critical such as motors, print heads, and relays.

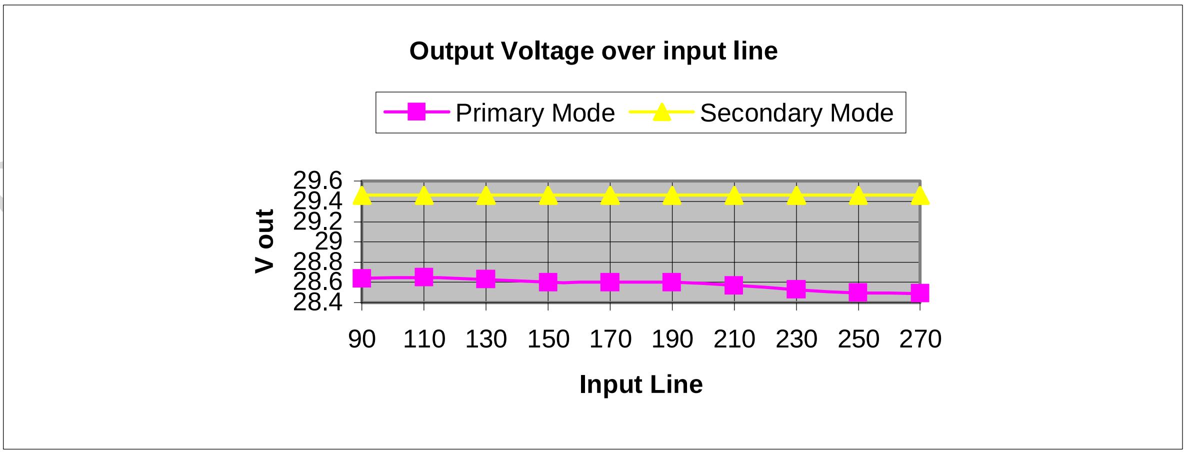
5.1 Output voltage regulation



For primary mode there is some peak charging below 30mA load. A load regulation of +/- 3.4% was achieved for a load span of 0.1A to 0.8A and +/-6% 0.1A to 1.5A.

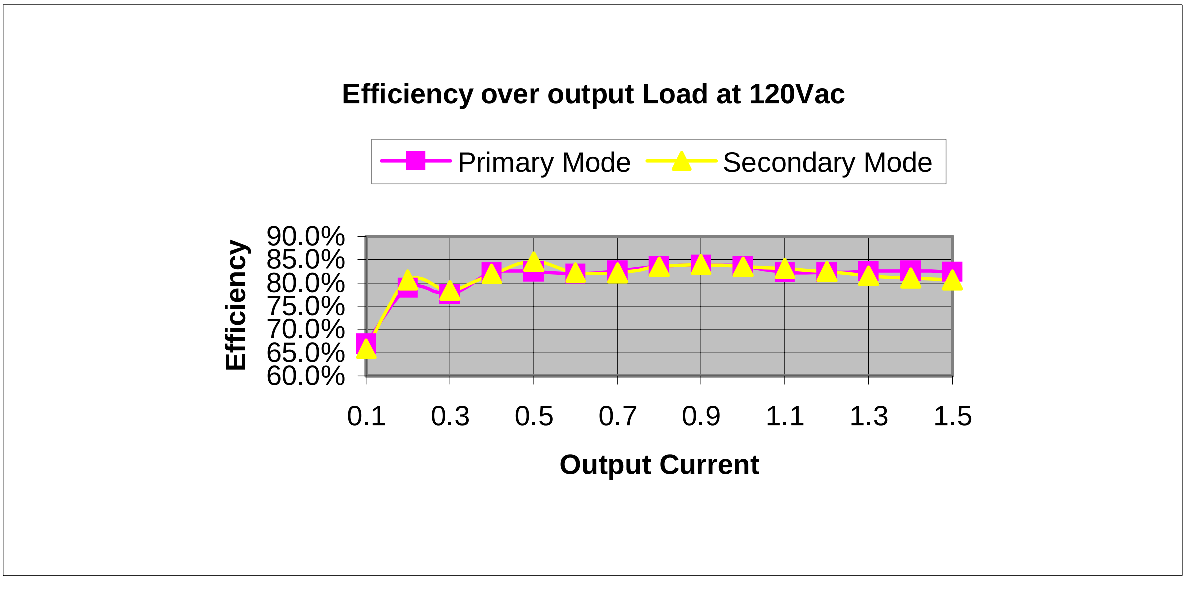
For secondary mode, a load regulation of +/- .02% was achieved for a load span of 0.1A to 0.8A and +/- 0.05% 0.1A to 1.5A.

5.2 Input Line regulation

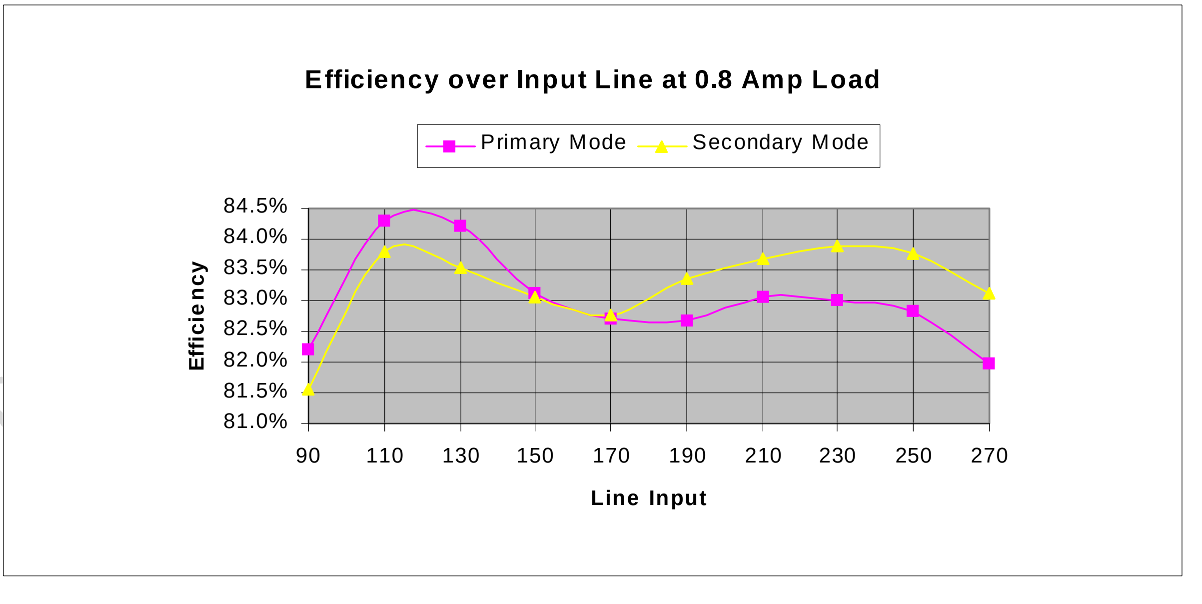


Primary mode line regulation for 110Vac to 230Vac is +/- 0.21%
Primary mode line regulation for 90Vac to 270Vac is +/- 0.26%
Line regulation for secondary mode is 0.0%

5.3 Efficiency versus load



5.4 Efficiency versus line



Secondary mode regulation efficiency is a little bit less because of the extra power in the TL431 and optocoupler circuitry.

6. BURST MODE

At no load or very light load, the VIPer53 goes into a burst mode. To reduce the switching losses and still allow regulation of the output voltage, the switching frequency is reduced by skipping cycles. The device is compliant to “Blue Angel” requiring around 0.5W of input power when in stand-by. This allows the regulation of the output even when the load corresponds to a duty cycle less than the minimum on time or internal blanking time. In primary mode, this is adjusted by the preload resistor R7. If the resistor is chosen as a compromise between input power at no load and a small peak charging at no load.

In secondary mode, a preload resistor value R7 is chosen and then R2 is chosen to adjust the V_{dd} voltage between 8.4V where the unit will shut down and 15V where primary mode regulation takes over. At no load V_{dd} will be at minimum, and at maximum load it will be at it’s highest. Depending on the coupling and turns ratio of the transformer, R2 is chosen to center the window around 12V. Figure 8 shows the good burst mode operating properly. Figure 9 shows the bad burst mode where V_{dd} falls to 8.4V where the device initiates a restart and there is a noticeable ripple on the output.

Figure 8

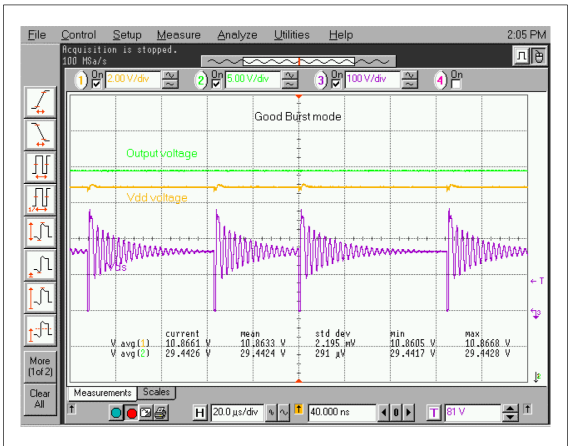
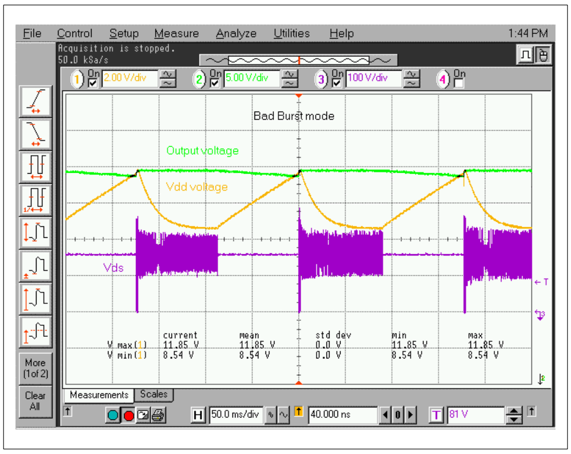
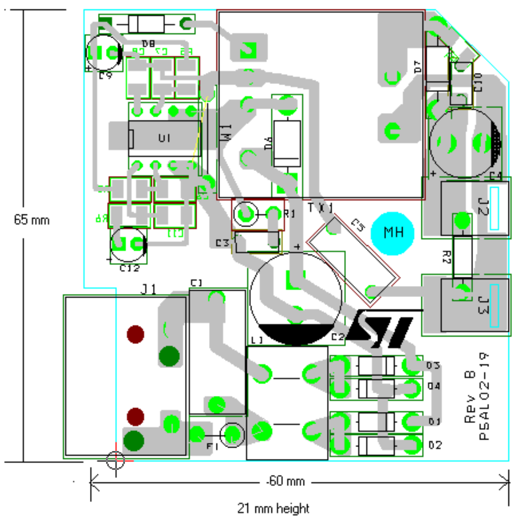


Figure 9

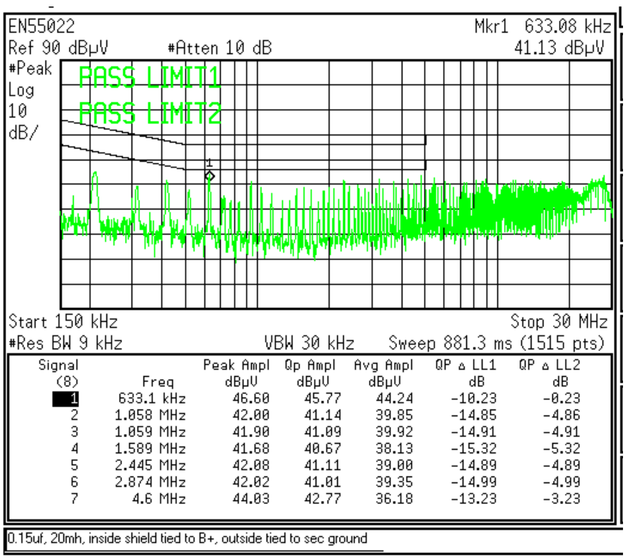


7. PC BOARD LAYOUT (not in scale)



Form factor given, allow for a tight layout with short current loops for primary mode regulation chosen by one customer.

8. EMI LINE CONDUCTED NOISE



The picture above shows a plot of an EMI scan for EN55022 class B Line conducted test. It also passes FCC class B. The numbers below show some of the peaks measured for average value and quasi-peak values.

9. COMPONENT LIST

Item	Qty	Ref	Part	Description	Part	Sec
1	1	C1	0.15uF	275V	X Cap	
2	1	C2	22uF	400V	SMR2DM470J200	
3	2	C10,C3	220pF	1KV		
4	1	C4	470uF	35V	LOW ESR	
5	1	C5	2.2nF	Y1	Y1	
6	1	C6	3.9nF		X7R	
7	2	C7,C8	0.1uF		X7R	
8	1	C9	47uF	25V	GP	
9	1	C10	47n			*
10	1	C11	NU			
11	1	C12	1uF	GP	GP	
12	4	D1,D2,D3,D4	1N4007			
13	1	D6	PKC-136	**STMicroelectronics**	ST	
14	1	D7	BYW100-200	**STMicroelectronics**	ST	
15	1	D8	1N4148			
16	1	F1	1A			
17	1	IC2	TL431		ST	*
18	1	IC3	H11A817A			*
19	1	J1	AC CON			
20	1	L1	20mH			
21	1	R1	51	1W		
22	1	R2	2.2			
23	1	R3	3.9K			
24	1	R4	22			
25	1	R5	10			
26	1	R6	15K			
27	1	R7	10k			
28	1	R8	150			*
29	1	R9	1.2k			*
30	1	R10	1.27k	1%		*
31	1	R11	14k	1%		*
32	1	TX1	CSM2525-007	Cramer coil	Secondary mode	*
33	1	U2	VIPer53DIP	**STMicroelectronics**		
	1	TX1	CSM2525-003C	Cramer coil	Primary mode	

Items with a * in the SEC column are parts used for secondary mode.

10. CONCLUSIONS

Power supply using the VIPer53 in Primary mode and secondary mode regulation were designed, built and tested to compare performance and cost. Different functions, mode of operations, protections and EMI have been checked with good results.

The VIPer53 allows designing a 24-watt power supply without a heat sink, without the addition of a reference and optocoupler with the reliability of current mode control with overload and over temperature protection.