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Microchip's Power MOSFET Driver Simulation Models

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INTRODUCTION

The simulation models for Microchip's power MOSFET drivers aid in the design and analysis of various circuits by allowing for detailed simulation of the circuit being designed.

This application note covers the function and use of the SPICE simulation models, tips on solving convergence issues, and provides a boost converter example using the TC1410N simulation model.

MODEL DESCRIPTION

The power MOSFET driver models were written and tested in Orcad's PSPICE 10.0 which is equivalent to Cadence PSPICE 15.x. The type of modeling technique that was used to model the MOSFET drivers is called "Macro Modeling". The model is based on treating the MOSFET driver as a black box and using mathematical equivalents of the internal functions.

There are many advantages of macro modeling over transistor level modeling. Since the internal circuitry has been simplified to mathematically represent the functions, the simulation runs much faster and is more robust. This allows the user to simulate their circuitry at the board or system level with the MOSFET drivers within a reasonable simulation time.

However with transistor level modeling, there are many interactions between the transistors. For example how voltage and current vary with time or temperature. In a macro model, some of these variations have to be simplified. For example, the quiescent current will vary smoothly over temperature for an actual IC or transistor level model. To model this using the macro modeling technique, a look-up table is used. This causes the macro model results to not be as smooth as the actual IC. However the discrepancies between the look-up table and the actual IC performance are minimal.

Parameters Covers By Model

The power MOSFET driver simulation model covers a wide aspect of the MOSFET driver's electrical specifications. Not only does the model cover voltage, current, and resistance of the MOSFET driver, but they also cover the temperature effects on the behavior of the MOSFET driver.

The models have been verified by comparing simulation results against actual driver behavior and specifications contained in the appropriate MOSFET driver data sheet.

The MOSFET driver simulation models have not been verified outside of the specification range listed in the MOSFET driver data sheet. The behavior under these conditions can not be guaranteed that it will match the actual driver performance.

Using The Power MOSFET Simulation Models

The MOSFET driver simulation models are provided in netlist format. This is useful for simulating the models in a number of different simulators. Please refer to your simulator software reference manual on how to create a schematic symbol and relating a netlist to the symbol. All SPICE simulation schematic tools are different in their creation of a schematic symbol and relating it to the library file.

The MOSFET driver model is in sub circuit format. An example of this sub circuit can be found in Figure 1.

```
.SUBCKT TC1410N  1 2 3 4
*                | | | |
*                | | | Negative Supply
*                | | Positive Supply
*                | Output
*               Input
.
... (Continuation of TC1410N Netlist)
.
.ENDS TC1410N_RevA
```

FIGURE 1: *TC1410N Sub Circuit.*

This model has four nodes: Input, Output, Positive Supply, and Negative Supply that correspond to the appropriate pins of the TC1410N MOSFET driver. Certain MOSFET driver netlist models have more nodes that correlate to the addition features present on those MOSFET drivers. However their sub circuit format follows the same node naming convention as shown in Figure 1.

The MOSFET driver models are self contained and require no other models or libraries to run. Figure 2 shows how to call the MOSFET driver sub circuit from a netlist.

```
.DC LIN V_V1 -6 20 0.1
.STEP PARAM VDD LIST 4, 16
.LIB "../../../ TC1410N_RevA.LIB"
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
V_VL       N15201 0 0
R_RL       G N15201  {RL}
X_U1_U1    10 11 12 13 TC1410N_RevA
C_CL       N15201 G  {CL}
V_VGND     13 0 0
V_V1       IN 0 0Vdc
R_RG       11 G  1m
V_VDD      12 0 {VDD}
R_RS       10 IN  50
.PARAM  VDD=10 PW=1 CL=500pF RL=1MEG
.END
```

FIGURE 2: *Calling MOSFET Driver Sub Circuit From Main Circuit Netlist.*

The “X_U1_U1” is the call statement for the MOSFET driver model TC1410N_RevA. The statement “.LIB “../../../TC1410N_RevA.LIB” calls the TC1410N_RevA.LIB which contains the TC1410N_RevA netlist.

SIMULATOR COMPATIBILITY

The original SPICE code, also known as “Berkeley SPICE”, was written by the University of Berkeley, CA. There are many other SPICE simulators, which have taken this code by Berkeley and modified to their own use. They have either modified the syntax structure, usually allowing more features, and/or modified the convergence algorithm to speed up the simulation and improve convergence. Out of all these simulators, PSPICE by Cadence is one of the most widely accepted general purpose circuit simulators and many SPICE vendors have included options to be “PSPICE compatible”. However being compatible does not remove the possibility of syntax errors or convergence issues existing between SPICE and PSPICE simulators.

CONVERGENCE ISSUES

For most simple circuits with short circuit simulation times, the default settings are sufficient as shown in Figure 3.

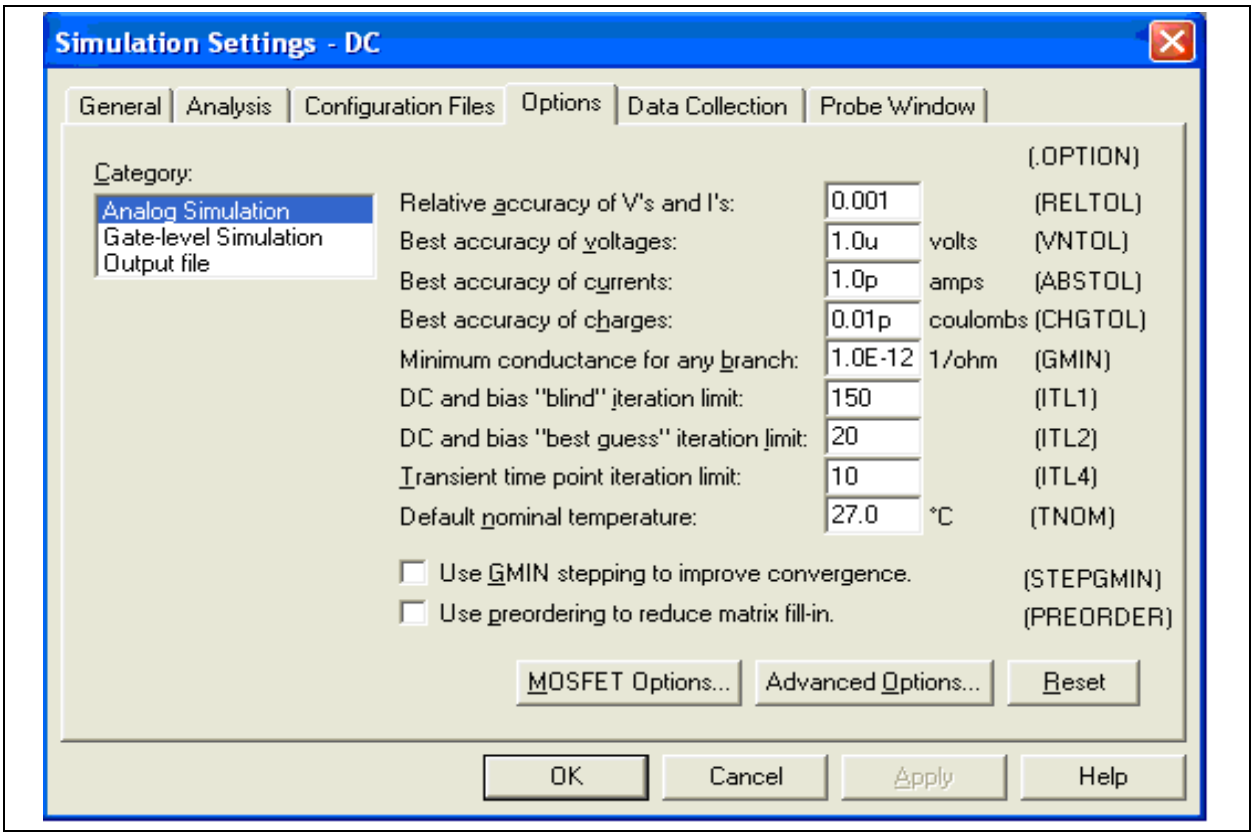

FIGURE 3: *Default PSPICE Settings.*

For complex circuits that have large voltages, currents, or long circuit simulation time, convergence issues could result. These convergence issues could be the MOSFET driver model, the external circuitry, or the simulators' default convergence parameters. Typically the default convergence parameters for PSPICE are set for certain types of circuits. The following are some helpful hints in fixing these convergence problems if encountered.

First change the following parameters. These do not hurt convergence and can only help.

- Increase the ITL1, ITL2, and ITL4 parameters to 1000. This allows the simulator to try smaller steps allowing for a better chance at converging
- Check the "Use GMIN stepping to improve convergence" option if its available. This will vary the GMIN parameter which is inversely proportional to the resistance the simulator adds to each node

If the convergence is still an issue, RELTOL, VNTOL, ABSTOL, and CHGTOL parameters can be changed. However adjusting these parameters can either help or hurt the convergence. It is recommended that the following steps be tried one at a time. If the adjustment does not fix the convergence issue, set it back to the default setting before changing the other parameters.

- Increase the RELTOL parameter to 0.01. This increases the dynamic range of the step size. It is required for circuits that are switching in nanoseconds yet the simulation time is microseconds or higher. This will help the simulator take smaller steps when needed. Going above 0.1 will cause the solutions to be unstable and erroneous results given
- Increase the tolerance parameters such as VNTOL, ABSTOL, and CHGTOL by a factor of 10x with a maximum factor of 100x. For better convergence, increase all of the parameters by the same amount. These parameters set the tolerance on the simulator for solving equations. As an example, in IC's the current can be in µA, but if simulating a switching power supply the currents can be in amps and trying to resolve the currents that are less than 1 µA makes it quite difficult for the simulator
- Configure the simulator is skip the bias point calculation or do not use initial conditions. Sometimes forcing a condition can cause the simulator not to find the correct solution for the whole circuit
- Adjust the maximum step size to a smaller value. This will force the simulator to take smaller steps, but it may take significantly longer to run

PRACTICAL BOOST EXAMPLE

The following is an example of a boost converter using the TC1410N MOSFET driver model.

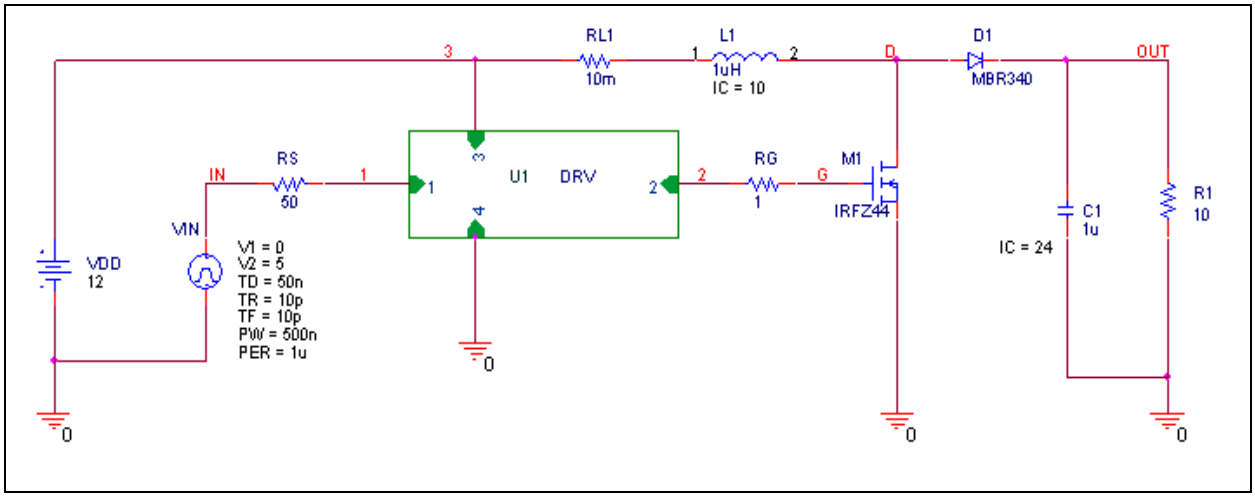

FIGURE 4: *Boost Converter Example.*

Proper simulation of the boost converter results in a long simulation time. This results in the need to change the simulation setting from their default settings. The RELTOL parameter was increased to 0.01. Alternately the maximum step size could be set to 1 nsec resulting in the same performance. Figure 5 shows the changes made to the default simulator settings. The results from the simulation can be found in Figure 6 and Figure 7.

The complete netlist for the simulated boost converter shown in Figure 4 can be found in **Appendix A: "Boost Converter Example Simulation Netlist"**.

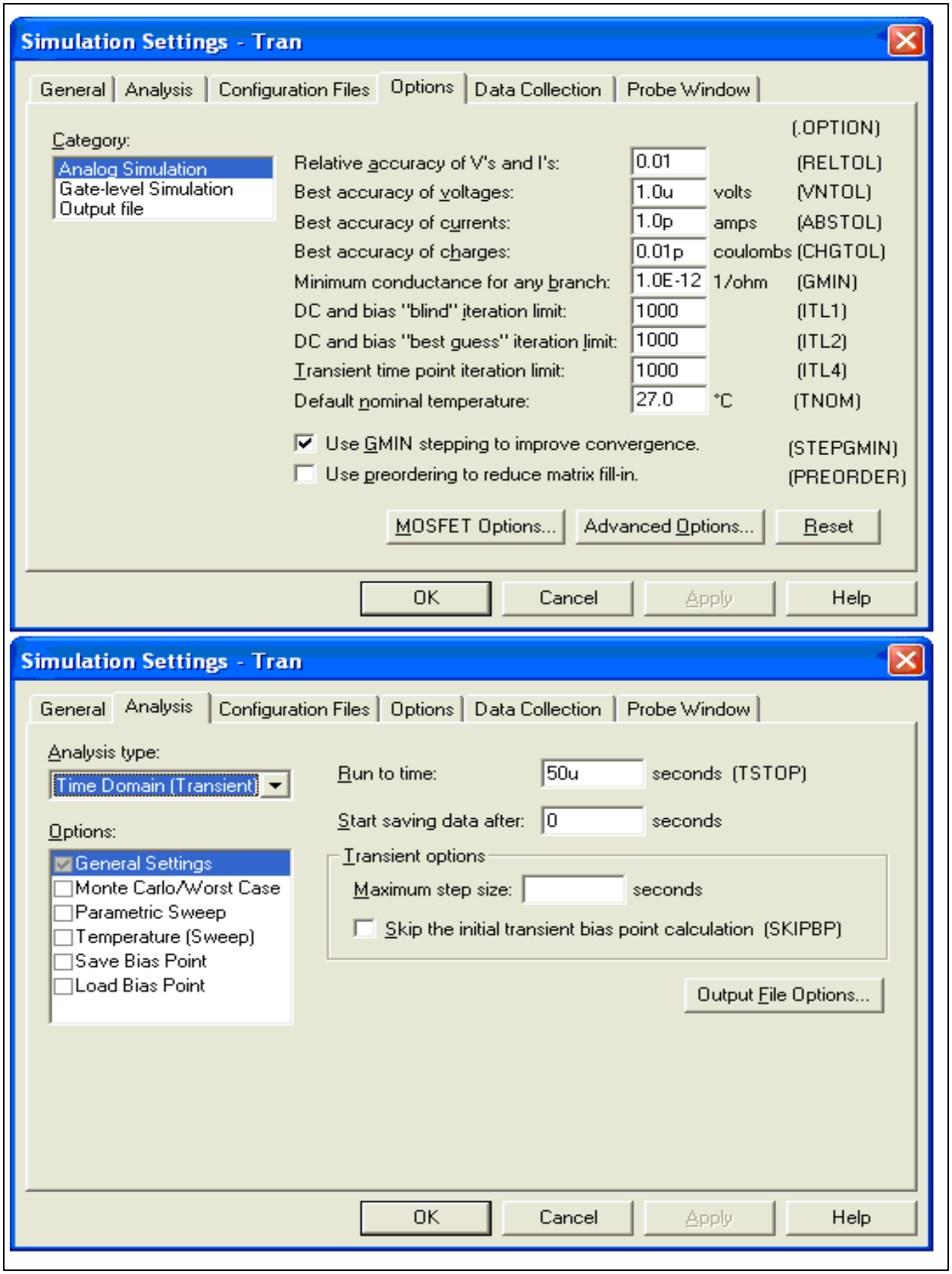

FIGURE 5: *Default Simulator Setting Changes.*

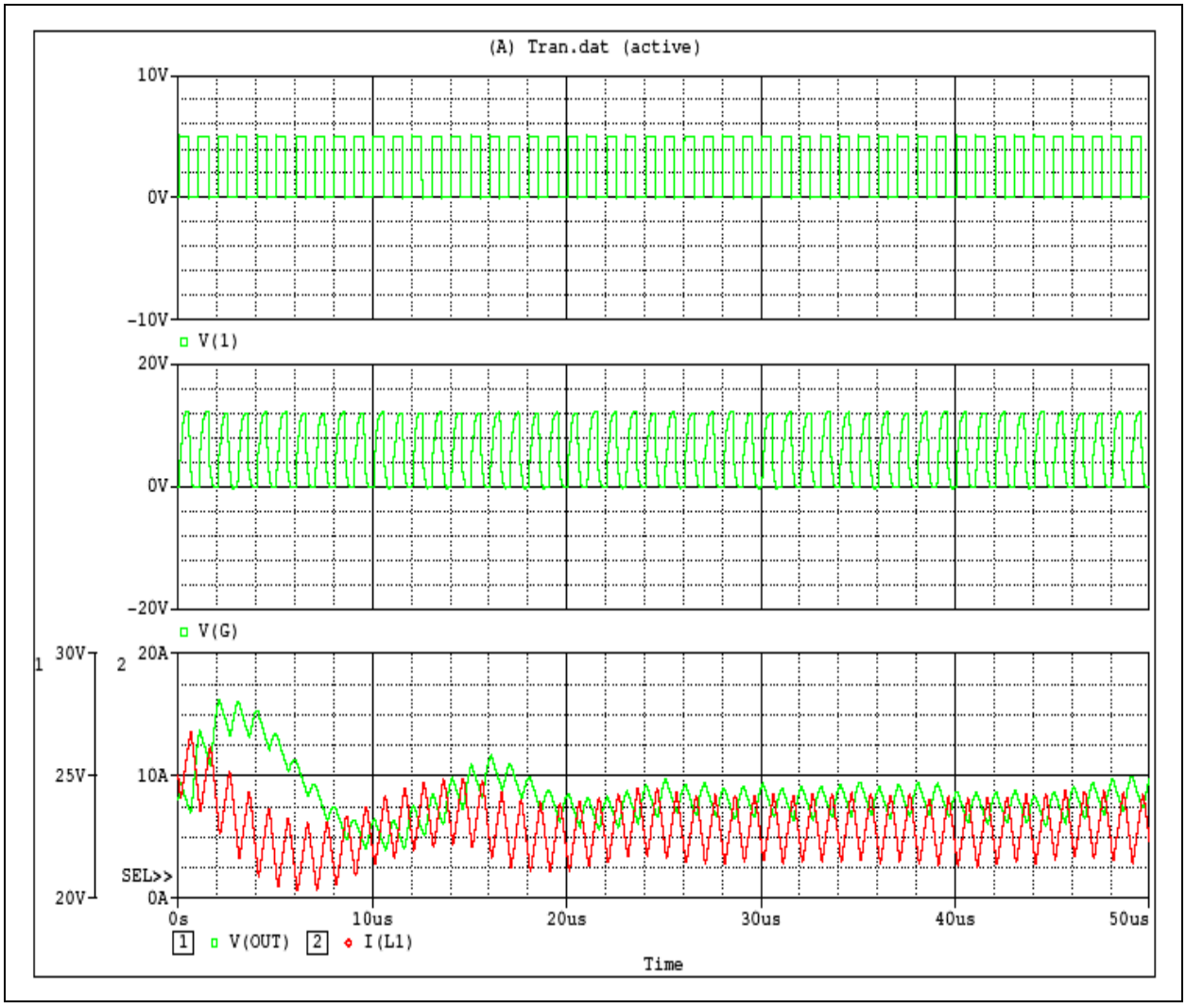

FIGURE 6: *Boost Convert Waveforms.*

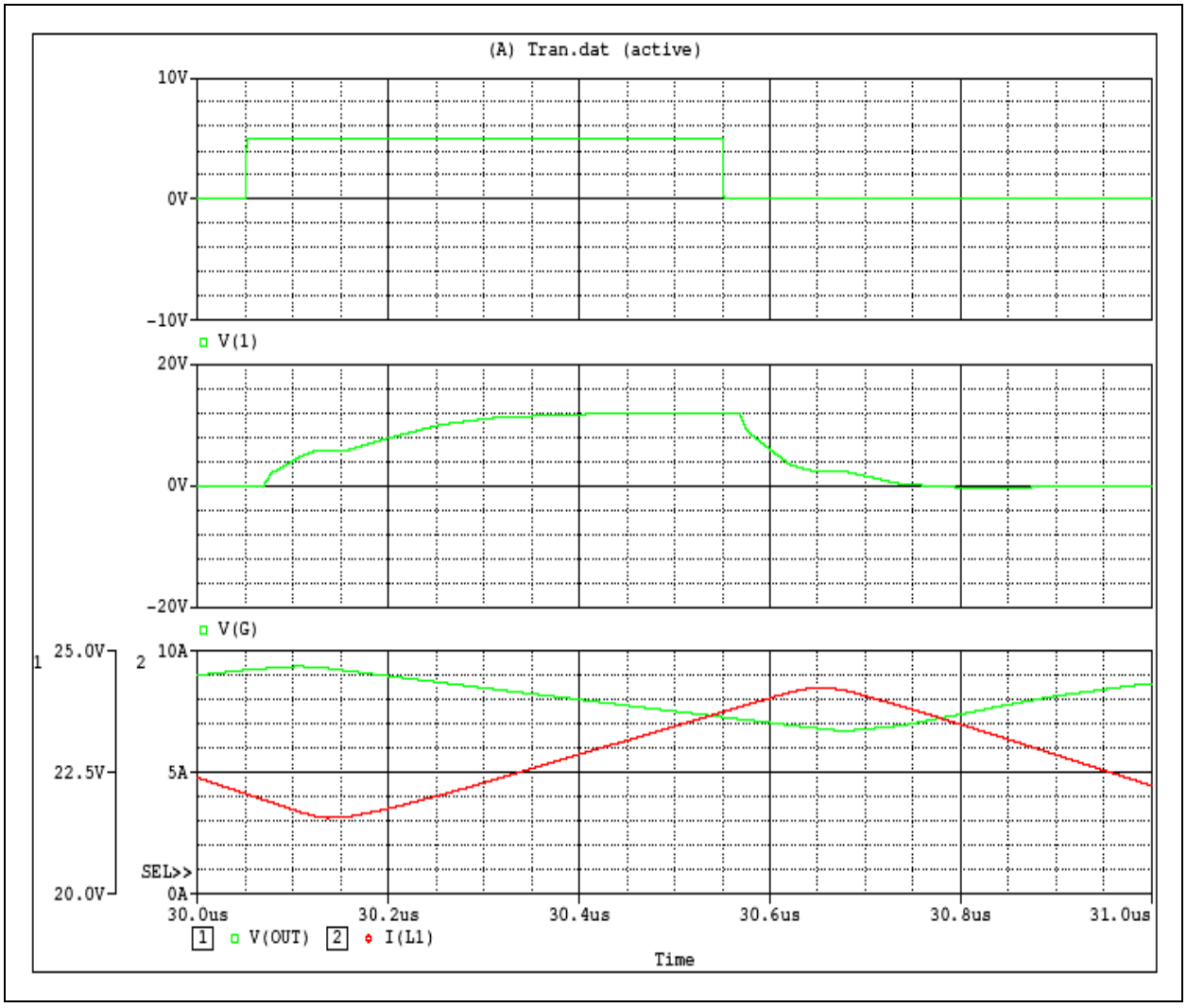

FIGURE 7: *Boost Convert Expanded Waveform.*

APPENDIX A: BOOST CONVERTER EXAMPLE SIMULATION NETLIST

```
*Libraries:
* Profile Libraries :
* Local Libraries :
.LIB "C:/OrCAD/OrCAD_10.0/tools/pspice/library/nom.lib"
.LIB "../../../mcp_drv.lib"

*Analysis directives:
.TRAN  0 50u 0
.OPTIONS EXPAND
.OPTIONS LIBRARY
.OPTIONS STEPGMIN
.OPTIONS ITL1= 1000
.OPTIONS ITL2= 1000
.OPTIONS ITL4= 1000
.OPTIONS RELTOL= 0.01
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))


* Main Circuit
D_D1         D OUT MBR340
M_M1         D G 0 0 IRFZ34
L_L1         N25602 D  1uH IC=10
R_RL1         3 N25602  10m
V_VDD         3 0 12
R_R1         0 OUT  10
R_RS         1 IN  50
C_C1         OUT 0  1u IC=24
R_RG         2 G  1
X_U1_U1         1 2 3 0 TC1410N_RevA
V_VIN          IN 0
+PULSE 0 5 50n 10p 10p 500n 1u
.END

**** FROM LIBRARY diode.lib ****
.model MBR340   D(Is=823.9n Rs=18.27m Ikf=.5654 N=1 Xti=0 Eg=1.11 Cjo=477.2p
+               M=.4787 Vj=.75 Fc=.5 Isr=838.6n Nr=2)


**** FROM LIBRARY pwrmos.lib ****
.model IRFZ34   NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0.2 Vmax=0 Xj=0
+               Tox=100n Uo=600 Phi=.6 Rs=38.1m Kp=20.42u W=2 L=2u Vto=3.247
+               Rd=3.031m Rds=266.7K Cbd=2.887n Pb=.8 Mj=.5 Fc=.5 Cgso=472.1p
+               Cgdo=292.8p Rg=6.827 Is=1.981p N=1 Tt=365n)

**** FROM LIBRARY ../../../mcp_drv.lib ****
.SUBCKT TC1410N_RevA 1 2 3 4
*      For a quick, effective design, use a combination of: data sheet
*            specs, bench testing, and simulations with this macromodel
*      For high impedance circuits, set GMIN=100F in the .OPTIONS statement
*
* Supported:
*      Typical performance for temperature range (-40 to 85) degrees Celsius
*      DC, AC, Transient, and Noise analyses.
*      Most specs, including: propgation delays, rise times, fall times, max sink/source current,
*            input thresholds, voltage ranges, supply current, ... , etc.
*      Temperature effects for Ibias, Iquiescent, output current, output
*            resistance,....,etc.
*
*
```

```
* Not Supported:
*      Some Variation in specs vs. Power Supply Voltage
*      Vos distribution, Ib distribution for Monte Carlo
*      Some Temperature analysis
*      Process variation
*      Behavior outside normal operating region
*
* Known Discrepancies in Model vs. Datasheet:
*
* Input Impedance/Clamp
R1  4    1    100MEG
C1  4    1    10.0P
G3  3    1    TABLE { V(3, 1) } ((-770M,-1.00)(-700M,-10.0M)(-630M,-1.00N)(0,0)(20.0,1.00N))
G4  1    4    TABLE { V(1, 4) } ((-5.94,-1.00)(-5.4,-10.0M)(-4.86,-1.00N)(0,0)(20.0,1.00N))
* Threshold
G11 0    30   TABLE { V(1, 11) } ( (-1m,10n)(0,0)(0.78,-.1)(1.25,-1)(2,-1) )
G12 0    30   TABLE {V(1,12)} ( (-2,1)(-1.2,1)(-0.6,.1)(0,0)(1,-10n))
G21 0    11   TABLE { V(3, 4) } ((0,1.35)(4.00,1.35)(6.00,1.5)(10.0,1.48)(13.0,1.49)(16.0,1.5))
G22 0    12   TABLE { V(3, 4) } ((0,1.35)(4.00,1.16)(6.00,1.25)(10.0,1.24)(13.0,1.24)(16.0,1.25))
R21 0    11   1 TC 504U  2.33U
R22 0    12   1 TC 231U  -103N
C30 30   0    1n
* HL Circuit
G31 0    31   TABLE { V(3, 4) } ((0,130)(4.00,47.0)(6.00,28.8)(10.0,19.1)(13.0,17.3)(16.0,18.5))
R31 31   0    1 TC 3.72M  18.4U
G33 0    30   TABLE { V(31, 30) } ( (-1M,-10)(0,0)(1,10N) )
S31 31   30 31 30 SS31
* LH Circuit
G32 32   0    TABLE { V(3, 4) } ((0,150)(4.00,45.0)(6.00,27.6)(10.0,16.6)(13.0,15.9)(16.0,15.0))
R32 0    32   1 TC 4.95M  42.0U
G34 30   0    TABLE { V(30, 32) } ( (-1M,-10)(0,0)(1,10N) )
R30 32   30   1MEG
* DRIVE
G51 0   50   TABLE { V(0, 30) } ( (-5,-1U)(-3,-1U)(0,0)(6,697M)(16,702M) )
G52 50   0    TABLE { V(30, 0) } ( (-5,-1U)(-3,-1U)(0,0)(6,997M)(16,1002M) )
R53 0    50   1
G50 51   60   VALUE {V(50,0)*200M/((200M-1)+16.0/(V(3,4) + 1M))}
R51 51    0   1
G53  3    0   TABLE {V(51,0)} ((-100,100)(0,0)(1,1n))
G54  0    4   TABLE {V(0,51)} ((-100,100)(0,0)(1,1n))
R60 0    60   100MEG
H67 0    69   V67 1
V67 60   59   0V
C60 561  60   100P
R59 59   2    4.39
L59 59   2    10.0N
* Shoot-through adjustment
VC60 56 0 0V
RC60 56 561 1m
H60 58 0 VC60 56
G60P 0 3 TABLE { V(58, 0) } ((-1,-1u)(0,0)(25,0.01)(40,0))
G60N 4 0 TABLE { V(0, 58) } ((-1,-1u)(0,0)(25,0.01)(40,0))
* Source Output
E67 67   0    TABLE { V(69, 0) } ( (-500M,-500M)(0,0)(1,2.00) )
G63 0    63   POLY(1) 3 4 60.7 -5.97 194M
R63 0    63   1 TC 3.75M 321n
E61 61   65   VALUE {V(67,0)*V(63,0)}
V63 65   3    100U
G61 61   60   TABLE { V(61, 60) } (-20.0M,-50.0)(-15.0M,-25.0)(-10.0M,-5.00)(0,0)(10,1N))
* Sink Output
E68 68   0    TABLE { V(69, 0) }  ( (-1,-2.00)(0,0)(500M,500M) )
G64 0    64   POLY(1) 3 4 16.1 -1.19 38.8M
R64 0    64   1 TC 5.19M 21.8U
E62 62   66   VALUE {V(68,0)*V(64,0)}
V64 66   4    100U
G62 60   62   TABLE { V(60, 62) } (-20.0M,-50.0)(-15.0M,-25.0)(-10.0M,-5.00)(0,0)(10,1N))
* Bias Current
G55 0    55   TABLE { V(3, 4) } ((0,0)(4.00,270U)(6.00,350U)(10.0,330U)(16.0,350U))
G56 3    4    55 0 1
R55 55   0    1 TC  462U 6.89U
G57 0    57   TABLE { V(3, 4) } ((0,0)(4.00,30.0U)(6.00,50.0U)(10.0,50.0U)(16.0,50.0U))
G58 3    4    57 0 1
```

```
R57 57   0    1 TC  -692U 11.9U
S59 55   0    1 0 SS59
* Models
.MODEL SS59 VSWITCH Roff=1m Ron=100Meg Voff=1.2V Von=1.5V
.MODEL SS31 VSWITCH Roff=100MEG Ron=800 Voff=0.2V Von=0.1V
.ENDS TC1410N_RevA
```

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