Implement a SMPTE 259M Serial Digital Interface Using SMPTE HOTLink™ and CY7C9235/9335

Introduction

The Society of Motion Picture and Television Engineers (SMPTE) is a professional organization that develops interface and protocol standards for the professional video industry. One such standard, SMPTE 259M, documents the Serial Digital Interface (SDI) which is used to transport 10-Bit 4:2:2 component and 4fSC composite digital video signals across 75Ω coaxial cables. This standard supports transmission of both 525 line@60 Hz and 625 line@50 Hz television signals in both 4:3 and 16:9 aspect ratio forms (Reference 1).

This application note describes how to implement an ANSI/SMPTE 259M link using the Cypress SMPTE chip set. The transmit portion of this chip set consists of the Cypress CY7C9235 SMPTE 259M/DVB-ASI Scrambler-Controller and the CY7B9234 SMPTE HOTLink™ Transmitter that provide the proper scrambling, encoding, and parallel-to-serial conversion of component (SMPTE 125M) or composite (SMPTE 244M) video. The receive portion of this chip set consists of the CY7B9334 SMPTE HOTLink Receiver and the Cypress CY7C9335 SMPTE 259M/DVB-ASI Descrambler/Framer-Controller that provide the proper serial-to-parallel conversion, decoding, descrambling, and framing of these same video formats (Reference 2, 3).

This application note also discusses how to use these same components to implement an interface that supports both SMPTE 259M and Digital Video Broadcast-Asynchronous Serial Interface (DVB-ASI) protocols. DVB-ASI is a similar professional video interface used to transmit MPEG2 (Motion Picture Experts Group) encoded video (Reference 4).

SMPTE-259M

SMPTE 259M specifies the requirements of the SDI between digital video equipment. This standard documents the means by which SMPTE 125M or 244M bit-parallel (4:2:2 component or 4fSC composite) digital video is serialized, scrambled, encoded, and transmitted over a link. It also specifies the receive requirements for serial-to-parallel conversion, decoding, descrambling, and framing.

SMPTE 259M defines four operating data rates that are listed as levels of support:

- Level A: 143 Mbps NTSC
- Level B: 177 Mbps PAL
- Level C: 270 Mbps 525/625 Component (4:3 aspect ratio)
- Level D: 360 Mbps 525/625 Component (16:9 aspect ratio)

To be considered SMPTE 259M compliant, a piece of equipment must support at least one of these data rates. An SDI supporting only 270 Mbps serial video would be identified as SMPTE 259M-C compliant, while one supporting 177, 270, and 360 Mbps would be identified as SMPTE 259M-BCD compliant.

Block Diagram

A simplified block diagram of the logic portion of a SMPTE 259M link is shown in Figure 1. The parallel data input for the transmit interface can accept either 8- or 10-bit parallel digital video (as specified by SMPTE 125M or 244M). The data captured at these parallel inputs are then converted to a serial data stream (LSB first). This serialized data is next routed to a scrambler and NRZI (Non-Return to Zero, Invert ones) encoder. The NRZI encoded serial stream is finally driven onto a coaxial cable.

This transmit path operates with a single clock operating at the 10-bit character rate. This character-rate clock is multiplied by ten using a high-performance PLL to provide the bit-rate clock for the serial data path. The specific serial data
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rate used is dependent upon the character rate of the source video stream.

The receive path performs the opposite function of the transmit path. This starts with a high-performance PLL-based Clock and Data Recovery (CDR) circuit that captures the serial data from the coaxial cable, and extracts a bit-rate clock from the transitions in the data stream. This bit-rate clock is then divided by ten to generate a character-rate clock that is presented along with the output characters.

The data bits captured at the serial interface are first routed through an NRZI-to-NRZ decoder. This decoded bit-stream is then descrambled to remove the extra transitions added at the transmit end of the link. The bit-stream is finally framed to the proper character boundaries, and the 10-bit characters are output.

**Scrambling**

Scrambling is used to increase the transition density of the serial bit-stream, and to attempt to limit the maximum run-lengths of continuous zeros or ones than can occur when sending certain characters. The scrambler generator polynomial is listed in Equation 1.

\[ G_1(X) = X^9 + X^4 + 1 \]  
\[ \text{Eq. 1} \]

Logic block diagrams of a serial implementation of a scrambler/NRZI encoder, and NRZI decoder/descrambler are shown in Figure 2. Each rectangle containing a \( D \) represents a D-type flip-flop. These flip-flops are connected to form a specialized shift register that implements the scrambler polynomial. The \( X^9 \) term in the scrambler polynomial identifies the maximum number of shifts that take place when scrambling each bit in the data stream. The scrambler is self clearing and operates by feeding back previously scrambled bits to be mixed with unscrambled bits.

In a SMPTE serial link, the least significant bit (LSB) of each 10-bit character is scrambled first. Once the data has been serialized, scrambled, and NRZI encoded, it can be sent over the cable to the receiver.

**NRZI Encoding**

NRZI encoding is also used to increase the transition density in the serial data stream. It also allows the data stream to be phase independent; i.e., an inverted data stream will decode to the same signal as a non-inverted stream. The NRZI encoder polynomial is listed in Equation 2.

\[ G_2(X) = X + 1 \]  
\[ \text{Eq. 2} \]

The hardware implementation of this polynomial consists of the last flip-flop and XOR gate in the transmit data path portion of Figure 2.

**Receive Operations**

The receive end of the interface performs the exact opposite functionality as the transmit interface. Following reception, the data bits are routed through an NRZI-to-NRZ converter and then descrambled. The hardware used to perform these operations is very similar to that used in the transmit portion of the interface, with two major exceptions.

First, the polynomials are reversed. Now instead of feedback operation, all the shift register XOR gates are configured for feed-forward operation. This removes the additional transitions added by the transmit data path and returns the data to its original bit-stream form.

The second major difference in the receive interface, is that the data (at this point) has no available reference to identify the start or end of each 10-bit character. The operation of finding the character boundary in the data stream is known as framing.

**Framing**

Framing is the function of determining where (in a serial data stream) characters begin and end. Framing of a SMPTE 259M video stream uses specialized hardware to detect a bit pattern known as the Timing Reference Signal (TRS). Once the TRS is detected, the framer hardware adjusts to align the 10-bit output character with the recovered character clock.

![Figure 2. Block Diagram of SMPTE 259M Scrambler/Encoder and Descrambler/Decoder](image-url)
The TRS consists of a three characters sequence of 3FF\textsubscript{h}, 000\textsubscript{h}, and 000\textsubscript{h} (10 bit hex) respectively. To allow this sequence to be used for framing, it must not be possible for the same bit sequence to occur at other bit offsets within characters. This is controlled within SMPTE video by making the characters in the ranges of 000\textsubscript{h}–003\textsubscript{h} and 3FC\textsubscript{h}–3FF\textsubscript{h} illegal for use in the active portion of video fields. This leaves 1016 characters in the code space for representing the various luminance and chrominance levels in the active video fields.

8-bit Video

Not all digital video formats are based on 10-bit characters. Some only carry 8-bit representations of images. While these video formats are somewhat lower in quality than those based on 10-bit characters, it is still possible to transport them across SMPTE 259M interfaces. This is done by mapping the 8-bit characters to the upper eight bits of each 10-bit character. The two unused bits in the 10-bit field are used for framing, it must not be possible for the same bit sequence to occur at other bit offsets within characters. All values in the range of 000\textsubscript{h} to 003\textsubscript{h} are reserved characters. All values in the range of 3FC\textsubscript{h} to 000\textsubscript{h} are converted to 3FF\textsubscript{h}. The conversion from an 8-bit TRS to an 10-bit character TRS is shown in Figure 3.

These 8-bit video formats reserve the 00\textsubscript{h} and FF\textsubscript{h} characters for use in the TRS. The two unused bits in the 10-bit field are undefined, but are usually tied LOW. This practice unfortunately converts the 8-bit TRS of FF\textsubscript{h}, 00\textsubscript{h}, 00\textsubscript{h} into 3FC\textsubscript{h}, 000\textsubscript{h}, 000\textsubscript{h}.

To allow these 8-bit video streams to operate, the encoding hardware checks the input character stream for any of the reserved characters. All values in the range of 000\textsubscript{h} to 003\textsubscript{h} are converted to 000\textsubscript{h}, while all values in the range of 3FC\textsubscript{h} to 3FF\textsubscript{h} are converted to 3FF\textsubscript{h}. The conversion from an 8-bit character TRS to an 10-bit character TRS is shown in Figure 3.

DVB-ASI

The DVB-ASI specification describes the serial transfer of MPEG-2 video. The ASI standard documents a serial link operating at a fixed 270 Mbps rate. DVB-ASI does not use the scrambling and NRZI encoding of SMPTE 259M. Instead it makes use of a form of encoding called 8B/10B. This code was developed for use on fiberoptic links, but has numerous signalling benefits for transmission of copper media as well.

DVB-ASI supports two different media types: 75Ω coaxial cable and multi-mode optical fiber using LED emitters. The physical layer of DVB-ASI is based in part on the FC-0 and FC-1 physical layers of the ANSI Fibre Channel (FC) Standard X3.230-1994, but at a slightly different data rate. A logic block diagram of a coaxial cable implementation of a DVB-ASI interface is shown in Figure 4 (Reference 5).

Additional information on the Digital Video Broadcasting standard is available from the DVB Project Office or from the DVB web site at, http://www.dvb.org.

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SMPTE and DVB

The DVB-ASI interface has numerous similarities to SMPTE 259M. Both interfaces operate on 75Ω cables terminated with BNC connectors. They both specify a peak-to-peak launch amplitude of 800mV±10%, and share a common serial transmission rate of 270 Mbps.

There are also numerous differences. The source data for DVB is based on 8-bit characters, while SMPTE uses 10-bit characters. Each interface also makes use of different methods (encoding vs. scrambling) of forcing transitions into the data stream.

Because the differences between DVB-ASI and SMPTE 259M exist only at the digital or protocol levels, it is possible to implement an interface that is capable of operating in both SMPTE 259M and DVB-ASI modes. The Cypress SMPTE chip set is the only digital video chip set capable of supporting both protocols. It allows dynamic selection of the video protocol by means of simple hardware (and/or software) control.

For more information on SMPTE standards, contact SMPTE or visit the SMPTE web site at, http://www.smpte.org.
The remainder of this application note focuses on implementing a SMPTE 259M SDI and how to make the same interface DVB-ASI compatible.

**SMPTE Chip Set Functional Description**

Cyress’s SMPTE chip set consists of four components:
- CY7C9235 SMPTE/DVB Scrambler/Controller
- CY7B9234 SMPTE HOTLink Serializer
- CY7B9334 SMPTE HOTLink Deserializer
- CY7C9335 SMPTE/DVB Descrambler/Framer

This chip set allows a video serial digital interface to be implemented that is compliant to both SMPTE 259M and DVB-ASI standards. Although DVB-ASI is specified for both coaxial and fiberoptic media, only the coaxial interface is discussed.

**CY7C9235 SMPTE/DVB Scrambler/Controller**

**SMPTE 259M Mode**

The CY7C9235 SMPTE-259M/DVB-ASI Scrambler/Controller is a CMOS integrated circuit designed to perform the scrambling, NRZ-to-NRZI encoding, and TRS detection and filtering required by SMPTE 259M. The 10-bit scrambled and encoded data outputs (Q₀–₉) of the CY7C9235, along with the ENA_OUT signal, are designed to be directly mated to a CY7B9234 SMPTE HOTLink Transmitter which converts the parallel characters into a SMPTE 259M compatible serial data stream.

**DVB-ASI Mode**

The CY7C9235 also contains the necessary multiplexers, control inputs, and outputs, to sequence out a DVB-ASI compliant video stream. Selection of DVB-ASI mode is made through use of a single input signal, DVB_EN. When operating with DVB-ASI data (DVB_EN = LOW), the scrambling and encoding required by SMPTE 259M are disabled. The data inputs (PD₀–₉) along with the ENA, and ENN signals (which can be used to interface to synchronous or asynchronous FIFOs) are latched into the input register in the CY7C9235, and routed directly to the Q₀–₉ and ENA_OUT outputs. The 8-bit parallel data outputs (Q₁–₈), along with the SVS (Q₉), SC/D (Q₀), and ENA_OUT signals are passed to the CY7B9234 SMPTE HOTLink.

**CY7B9234 SMPTE HOTLink Serializer**

**SMPTE 259M Mode**

In SMPTE 259M mode (MODE = HIGH), the CY7B9234 SMPTE HOTLink Transmitter accepts the ENA_OUT signal as well as the 10-bit parallel scrambled and encoded data from the CY7C9235. It converts the parallel data into a serial form ready to be driven across the link. The SMPTE HOTLink is configured for BYPASS mode, which allows it to serialize the 10-bit data and transmit it at ten times the character clock rate. The SMPTE HOTLink supports serial data rates of 160-400 Mbps, allowing compliance to SMPTE 259M-BCD.

**DVB-ASI Mode**

When configured for DVB-ASI mode (MODE = LOW), the SMPTE HOTLink transmitter accepts the 8-bit parallel data, SC/D, SVS, and ENA_OUT signals from the CY7C9235. The SMPTE HOTLink performs the 8B/10B encoding required for DVB-ASI. For DVB-ASI operation the serial data rate must be fixed at 270 Mbps. A simplified block diagram of the transmit portion of a SMPTE 259M/DVB-ASI serial interface is shown in Figure 5.

**CY7B9334 SMPTE HOTLink Deserializer**

**SMPTE 259M Mode**

In SMPTE 259M mode (MODE = HIGH), the CY7B9334 SMPTE HOTLink Receiver is configured for BYPASS mode. It accepts the serial data stream generated by the SMPTE HOTLink Transmitter, performs the serial-to-parallel conversion, and passes 10-bit parallel characters to the CY7C9335.

**DVB-ASI Mode**

In DVB-ASI mode (DVB_EN = HIGH), the CY7B9334 SMPTE HOTLink Receiver is configured for ENCODED mode. It accepts the serial data stream generated by the SMPTE HOTLink Transmitter, performs serial-to-parallel conversion, 10B/8B decoding, and presents 8-bit parallel characters, along with the SC/D and RVS outputs to the CY7C9335.

**CY7C9335 SMPTE/DVB Descrambler/Framer**

**SMPTE 259M Mode**

The CY7C9335 SMPTE-259M/DVB-ASI Descrambler/Framer is a CMOS integrated circuit, designed to be directly mated to the SMPTE HOTLink Receiver. In SMPTE 259M mode (DVB_EN = HIGH), it receives the deserialized data from the SMPTE HOTLink Receiver as 10-bit parallel characters, and performs the descrambling and decoding functions as specified in SMPTE 259M. Following TRS detection, it frames the descrambled characters to the proper character boundaries and outputs 10-bit parallel characters.

**DVB-ASI Mode**

In DVB-ASI mode (DVB_EN = LOW), the CY7C9335 automatically enables both the 10B/8B decoder and multi-byte framer logic contained in the CY7B9334 SMPTE HOTLink Receiver. All error detection, fill, and command codes are detected and output by the CY7C9335. In this mode the decoding and descrambling functionality (required for SMPTE 259M operation) is disabled the characters are routed directly to the CY7C9335 outputs. A simplified block diagram of the receive end of the SMPTE 259M/DVB-ASI serial interface is shown in Figure 6.

**SMPTE 259M Transmit Interface**

A schematic of a complete transmit interface is shown in Figure 7. This interface is capable of transmitting data compatible with either SMPTE 259M or DVB-ASI standards, and can be dynamically configured for either or both protocols.
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Both SMPTE 244M and SMPTE 125M digital video standards document video stream formats that are suitable for transport on SMPTE 259M interfaces. These interfaces provide 10-bit parallel characters that are fed to the DATA9–0 inputs of the CY7C9235 (DATA9 is the MSB).

For those SMPTE implementations using 8-bit characters, the DATA9–2 inputs are used to carry the video characters, and DATA1–0 are tied LOW. With 8-bit data path, it is necessary to tie the TRS_FILT input of the CY7C9235 LOW to enable the proper conversion of 8-bit TRS characters to 10-bit TRS characters (as shown in Figure 3).

The video characters are accompanied by a continuous character clock. This clock is used both to latch the data into the CY7C9235, and as a reference for a bit-rate clock multiplier PLL in the CY7B9234. This clock operates at the character rate of the SMPTE video format: 17.7 MHz for Level B, 27.0 MHz for Level C, and 36.0 MHz for Level D.

The parallel SMPTE video interface standards, when driven through a cabled interface, operate with differential ECL-compatible signals. The CY7C9235, however, accepts only TTL or CMOS level signals at all inputs. If the parallel data for the CY7C9235 comes from one of these ECL interfaces, it is necessary to convert the differential ECL signals to single-ended TTL. This can be done by using an ECL-TTL translator such as the Cypress CY101E383 ECL/TTL/ECL Translator and High-Speed Bus Driver.

**Line Interface**

The CY7B9234 SMPTE HOTLink outputs serialized data through three differential PECL pairs (OUTA±, OUTB±, and OUTC±). Each output pair can be used to direct the serial stream to different applications. The PECL outputs require proper biasing and termination. See the Cypress HOTLink User’s Guide for additional information on biasing and termination of these serial outputs (Reference 6).

The serial media interface for both SMPTE 259M and DVB-ASI requires a single-ended signal, at 800 mV±10% (p-p), launched into a 75Ω transmission line or a matching resistive load. These signals are required to be source matched with a return loss (S11) of less than 15dB. Because the source matching adds a 6-dB loss from the signal generated by the driver, it is not possible to directly drive the interface using the standard PECL outputs of the CY7B9234. Separate line drivers are available that are optimized for this type of signal transmission, such as the MC10EL89, or the CLC007. While only a single external driver is shown in Figure 7, the CY7B9234 SMPTE HOTLink can support multiple line drivers per PECL output pair. The triple redundant...
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output pairs of the CY7B9234 permit a wide array of local and external connections.

If the interface is to be used only for DVB-ASI serial streams, the external driver may be replaced with a Balun transformer. This transformer allows the complimentary PECL outputs of the SMPTE HOTLink to drive a single cable or load to the proper amplitude. Due to the limited bandwidth of the transformer (and the very wide bandwidth requirements of SMPTE serial signaling) this transformer configuration cannot be used for SMPTE video signals.

Configuration

The schematic in Figure 7 shows the inputs used by both SMPTE 259M and DVB-ASI serial interfaces. In addition to the ten data inputs and character clock, there are eight control inputs that determine how the CY7C9235 (and the CY7B9234) operates. These control inputs can be divided into three groups: mode selection, configuration, and diagnostic.

Mode Selection

The DVB_ENABLE input is the only mode selection signal present. For operation as a SMPTE 259M interface the DVB_ENABLE line must be tied HIGH. This enables the scrambler and NRZ-to-NRZI encoder in the CY7C9235. In this mode, the ENA, ENN, SVS_EN, and SC/D_EN configuration inputs are ignored.

For operation as a DVB-ASI interface the DVB_ENABLE input must be LOW. This mode disables the scrambler and NRZ-to-NRZI encoder, and passes the data from the input register to the CY7B9234 for 8B/10B encoding and serialization. In this mode the TRS_FILT configuration input is ignored.

Configuration Inputs

The CY7C9235 has five configuration inputs:

- TRS_FILT—filter TRS characters
- ENA—enable parallel data
- ENN—enable next parallel data
- SVS_EN—enable error characters
- SC/D_EN—enable control characters

The TRS_FILT input is only interpreted when the CY7C9235 is set for SMPTE operation. In this mode, it controls the filtering of the non-video characters. When TRS_FILT is HIGH, all input characters are passed to the scrambler without modification. When TRS_FILT is LOW, all 10-bit characters in the range of 000h to 003h are converted to 000h, and all characters in the range of 3FCh to 3FFh are converted to 3FFh.

The ENA input is only interpreted when the CY7C9235 is set for DVB operation. In this mode it controls the timing of the ENA_OUT signal that is passed to the CY7B9234. When ENA is active (LOW) at the rising edge of the character clock (CKW), the character present on the PD9–0 inputs is routed to the CY7B9234 inputs and ENA_OUT is driven LOW.

The ENN input is only interpreted when the CY7C9235 is set for DVB operation. In this mode it controls the timing of the ENN_OUT signal that is passed to the CY7B9234. When ENN is active (LOW) at the rising edge of the character clock (CKW), the character present on the PD9–0 inputs at the immediately following character clock is routed to the CY7B9234 inputs and ENA_OUT is driven LOW.

The SVS_EN input is only interpreted when the CY7C9235 is set for DVB operation. In this mode it controls the propagation of the PD9 input to the Q9 output of the CY7C9235. When SVS_EN is HIGH, data present on the PD9 input is passed directly to the Q9 output without modification. When SVS_EN is LOW, Q9 is forced LOW.

The SC/D_EN input is only interpreted when the CY7C9235 is set for DVB operation. In this mode it controls the propagation of the PD9 input to the Q9 output of the CY7C9235. When SC/D_EN is HIGH, data present on the PD9 input is passed directly to the Q9 output without modification. When SC/D_EN is LOW, Q9 is forced LOW.

Diagnostic Inputs

The BYPASS input is used for diagnostic purposes. When active (HIGH) it overrides the DVB_ENABLE mode selection input. In this mode, all data present at the PD9–0 inputs of the CY7C9235 are passed without modification to the Q9–0 outputs.

The OE input controls the output drivers of the CY7C9235. When OE is HIGH, all data and control outputs are active. When OE is LOW, all data and control outputs become high impedance.

SMPTE 259M Receive Interface

A schematic of a complete receive interface is shown in Figure 8. This interface is capable of receiving data compatible with either SMPTE 259M or DVB-ASI standards, and can be dynamically configured for either or both protocols. It is constructed from a cable receiver/equalizer (such as the CLC014), the CY7B9334 SMPTE HOTLink Receiver, and the SMPTE 259M/DVB-ASI Descrambler/Framer-Controller.

Line Interface

Signals are received from a 75Ω coaxial cable. These signals are first routed to an adaptive equalizer. This function is necessary to operate with maximum length cables (up to 300m) allowed by SMPTE 259M. When used on shorter cables it is possible to couple the signal directly to the CY7B9334 SMPTE HOTLink Receiver using capacitive coupling.

When used only for DVB-ASI operation, the CY7B9334 may also be transformer coupled to the coaxial cable. Additional information on transformer coupling is available in the Cypress HOTLink User’s Guide.

Deserializer

Following equalization (if present) the serial data is fed to the CY7B9334 SMPTE HOTLink for deserialization into parallel characters. The SMPTE HOTLink receiver extracts both bit and character-rate clocks from the transitions in the serial data stream. The bit-rate clock is used to sample the data stream to recover the serial data. These recovered bits are then output as parallel characters.

The CY7B9334 SMPTE HOTLink receiver outputs the parallel characters in one of two forms, depending on the state of the DVB_ENABLE signal. When DVB_ENABLE is active (LOW), the CY7B9334 decodes the received characters using an integrated 10B/8B decoder. When DVB_ENABLE is inactive (HIGH), the decoder is disabled and raw 10-bit characters are passed to the CY7C9335 for decoding and framing.

The SMPTE HOTLink Receiver also requires a local reference clock to operate. This reference clock feeds the...
The CY7C9335 is used to process SMPTE 259M or DVB-ASI character streams. It operates in one of three modes as selected by the DVB_ENABLE, BYPASS, and OE signals.

### SMPTE 259M Operation
When DVB_ENABLE is inactive (HIGH), the CY7C9335 is configured for handling of SMPTE 259M character streams. In this mode, the 10-bit characters received from the CY7B9334 are routed first through an NRZI-to-NRZ converter, then through a descrambler. The descrambled characters are then searched for the TRS pattern to locate the start and end of each character in the data stream. Finally, the framed characters are output to the PD9-0 pins of the CY7C9335.

The H_SYNC signal is used to indicate the detection of the TRS pattern in the data stream. This signal toggles state one clock cycle prior to the first character (3FFh) of the TRS appearing at the PD9-0 outputs.

SYNC_EN is used to limit the effect of bit errors in the data stream from causing a false detection of a TRS. When SYNC_EN is inactive (LOW), the framer adjusts the output character boundary on every TRS found in the data stream. When SYNC_EN is active (HIGH), the character offset is only updated following the detection of two consecutive TRS patterns that both indicate a different character offset.

The detection of a new character offset (when SYNC_EN is active) is indicated by the SYNC_ERR output. This output pulses HIGH for one clock period, starting at the same time that H_SYNC toggles.

The CY7C9335 outputs are TTL compatible. These outputs cannot be directly used to drive a SMPTE 125M or 244M parallel interface. They can be adapted to these interfaces by converting them to differential ECL using a device such as the CY101E383 ECL/TTL/ECL Translator.

### DVB-ASI Operation
When DVB_ENABLE is active (LOW), the CY7C9335 disables the decoding, descrambling and framing capabilities used for SMPTE data reception. These same functions are performed by the CY7B9334 SMPTE HOTLink receiver. In this mode, the H_SYNC and SYNC_ERR outputs are not used.

When the DVB_ENABLE signal is asserted (LOW) the RF output of the CY7C9335 is driven HIGH. This places the CY7B9334 SMPTE HOTLink receiver into the multi-byte framing mode that is required for DVB_ASI operation.

### Diagnostic Controls
The CY7C9335 has two diagnostic inputs. When BYPASS is active (HIGH) it overrides the DVB_ENABLE mode selection input. In this mode, all data present at the D9-0 inputs of the CY7C9335 are passed without modification to the PD9-0 outputs.

The OE input controls the output drivers of the CY7C9335. When OE is HIGH, all data, status, and control outputs are disabled.
active. When OE is LOW, all outputs become high impedance.

Mixed SMPTE 259M/DVB-ASI Environment

A standard SMPTE 259M environment makes use of both true and compliment (inverted) data streams. These can be used interchangeably due to the NRZI encoding of the serial data. Normally, the 8B/10B encoded streams used for DVB-ASI transmission can only be used with true (non-inverted) data streams. This either prohibits these data streams from being used with SMPTE serial switches, or greatly restricts the usable ports on those switches.

The CY7C9335 contains circuitry to allow reception of both true and compliment 8B/10B encoded DVB-ASI video streams. This circuitry operates by monitoring the decoded character stream for a statistical error rate, and inverting the data stream if this rate is exceeded. This automatic inversion is only enabled when DVB_ENABLE is asserted (LOW). To enable this capability, the CY7B9234 and CY7C9335 must be connected as shown in Figure 9.

Conclusion

The Cypress SMPTE chip set is capable of generating and receiving both SMPTE 259M and DVB-ASI compatible serial data streams. It allows selection of the operating mode to be performed on a dynamic basis. By making use of the superior PLL characteristics found in the CY7B9234 and CY7B9334 SMPTE HOTLinks, it is possible to build compatible interfaces that are simple to design, free from calibration, and immune from the temperature and noise problems that have plagued similar interfaces in the past.

References

4. Interfaces for CATV / SMATV Headends and Similar Professional Equipment, DVB Document A010, October 1995

![Figure 9. Schematic of a SMPTE 259/DVB-ASI Receiver SDI](image-url)