



Application Note 129

PCB Layout Guideline for SDRAM SDICLK and SDOCLK

KS8695X/KS8695P/KS8695PX

General Description

SDOCLK is the SDRAM device clock and can be programmed from 25 MHz to 125 MHz. SDICLK is used to register the data read from the SDRAM back into KS8695. To insure proper read timing is met with respect to KS8695 internal timing requirement, SDICLK must be delayed with respect to SDOCLK as shown in Figures 1.

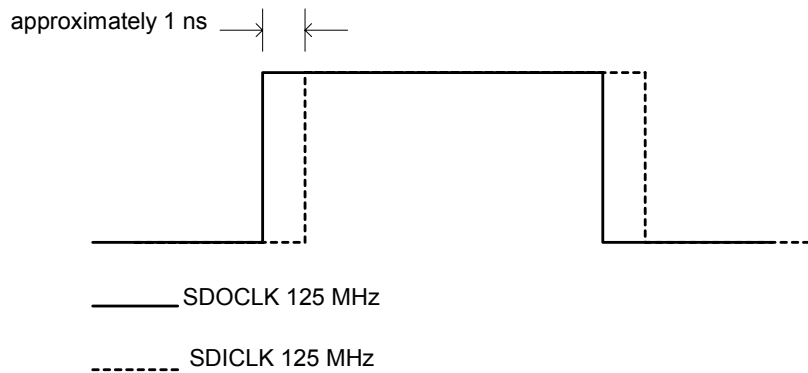


Figure 1 SDOCLK vs. SDICLK Phase Relation

Figure 2 illustrates recommended implementation of this phase.

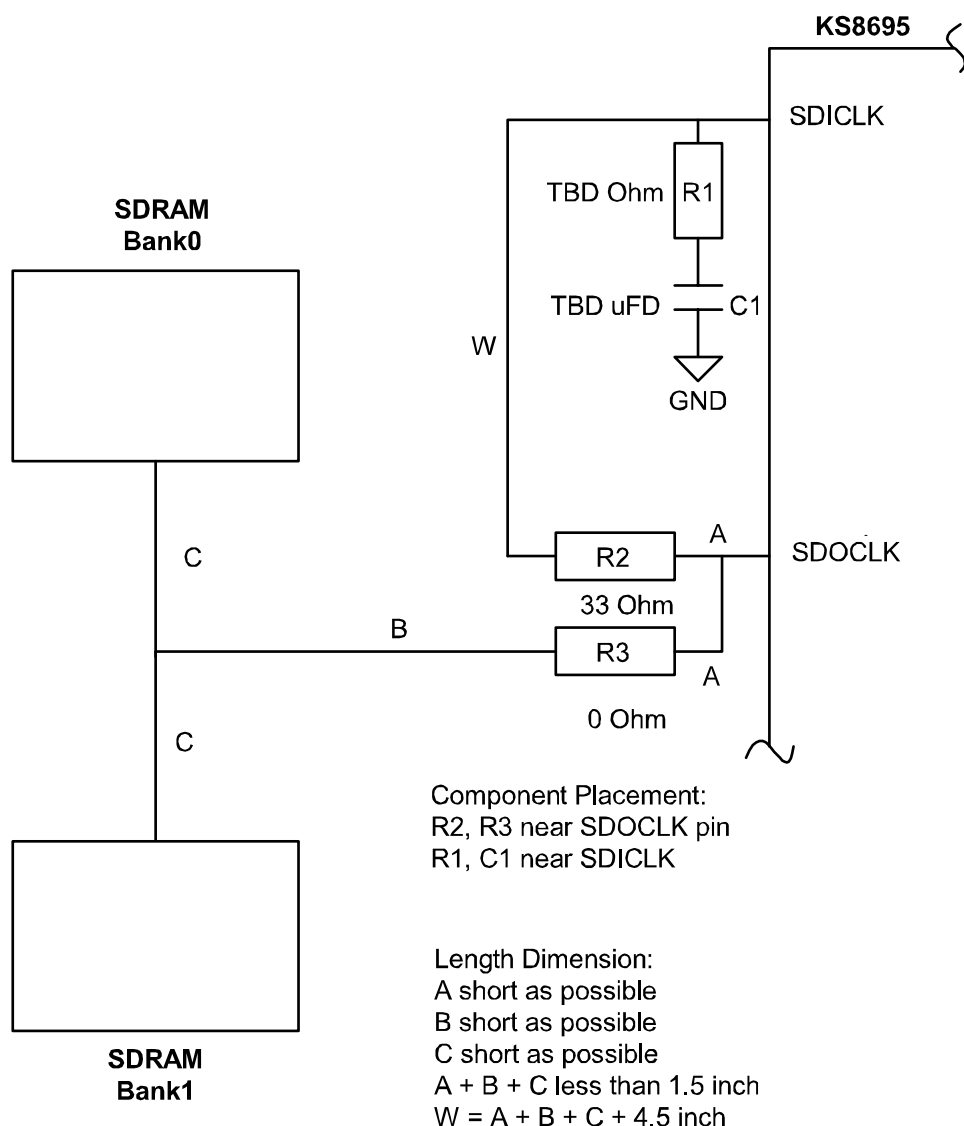


Figure 2. SDOCLK vs. SDICLK Phase Relation Implementation

R1 and C1 are RC termination to provide additional SDICLK delay if needed.

It is recommended to layout traces as 50 ohm and next to GND layer for impedance control. Traces should be kept on same layer to avoid vias. If vias must be used, do not exceed 2 vias. Place SDRAM devices as close as possible to the KS8695 to minimize SDOCLK length.

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Revision History		
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