



# Application Note 113

## Protocol Engine for CRC Generation

### KS8695X

#### General Description

The KS8695X features a hardware protocol engine that accelerates packet-processing performance. In many systems, the central processing unit (CPU) is left with the burden of verifying the internet protocol (IP) header, transmission control protocol (TCP), or user datagram protocol (UDP) checksum of each incoming packet, and then calculating a checksum for each outgoing packet. The hardware protocol engine relieves the CPU of these duties, leaving more processing power for other tasks, such as firewall and VPN software, or simply to boost throughput.

This application note shows how to configure the KS8695X and user software to take full advantage of the hardware protocol engine.

For additional support, contact your local Micrel Field Application Engineer or salesperson.

#### Enabling the Protocol Engine

The protocol engine can be enabled for the WAN and LAN interfaces independently. There are separate bits to enable the IP header, TCP, and UDP checksum generation for outgoing packets. We strongly recommend that hardware transmit padding be enabled along with hardware CRC insertion.

If software padding is used, the software must pad with zeroes, and the length field must be updated to 60 bytes. Padding is usually required for data alignment. For example, when you send an 8-bit character across the network as a 32-bit word, you need to pad, i.e., "fill in" the extra 24 bits with 0.

There are separate enable bits for the IP, TCP, and UDP checksum verification on incoming packets. The system register offsets and bit numbers are shown in the following tables.

In general, these bits should be enabled as a default for systems that want to get the most performance out of the KS8695X hardware. In the Linux OS, there is a mechanism to notify the upper layer stack of the status of these bits. This allows the upper layer to take the appropriate actions.

System Register	Bit	Description	Enable	Disable (default)
0x6000	16	WAN MAC Transmit IP Header Checksum Generate	1	0
0x6000	17	WAN MAC Transmit TCP Checksum Generate	1	0
0x6000	18	WAN MAC Transmit UDP Checksum Generate	1	0
0x8000	16	LAN MAC Transmit IP Header Checksum Generate	1	0
0x8000	1	LAN MAC Transmit TCP Checksum Generate	1	0
0x8000	18	LAN MAC Transmit UDP Checksum Generate	1	0

Table 1. Protocol Engine Checksum Generation Enable Bits

System Register	Bit	Description	Enable	Disable (default)
0x6000	1	WAN MAC DMA Transmit Add CRC	1	0
0x6000	2	WAN MAC DMA Transmit Enable Padding	1	0
0x8000	1	LAN MAC DMA Transmit Add CRC	1	0
0x8000	2	LAN MAC DMA Transmit Enable Padding	1	0

Table 2. Protocol Engine TX Padding and CRC Insertion Enable Bits

System Register	Bit	Description	Enable	Disable (default)
0x6004	16	WAN MAC Receive IP Header Checksum Verification	1	0
0x6004	17	WAN MAC Transmit TCP Checksum Verification	1	0
0x6004	18	WAN MAC Transmit UDP Checksum Verification	1	0
0x8004	16	LAN MAC Transmit IP Header Checksum Verification	1	0
0x8004	17	LAN MAC Transmit TCP Checksum Verification	1	0
0x8004	18	LAN MAC Transmit UDP Checksum Verification	1	0

**Table 3. Protocol Engine Checksum Verification Enable Bits**

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