

General Description

One popular application for the KS8695X is as a wireless access point plus residential gateway. With the powerful ARM9 CPU and a 3rd generation 5-port switch built-in, the system designer needs only to interface the KS8695X with an 802.11b wireless LAN chipset and some memory to complete the hardware design.

This application note illustrates how to connect the KS8695X to a PCMCIA connector to implement the wireless LAN access point portion of the design. The descriptions in the application note are based on reference hardware that was built and validated to work with Intersil PRISM® 2.5 or PRISM® 3.0 chipsets.

Since the reference board was designed for the development environment, the hardware supports 3.3V PCMCIA cards only. It does not support hot plug features. Hot plug features can be supported using GPIO pins and external glue logic.

Scenario

The connections between the KS8695X and the PCMCIA connector are shown in Figure 1. Address lines A[16:2] are passed through a 16244 buffer and connected to PCMCIA connector address lines A[14:1]. The buffer is required to handle the loading of the PCMCIA card that will be plugged into the socket. It is not required if the WLAN chipset is placed directly on the board.

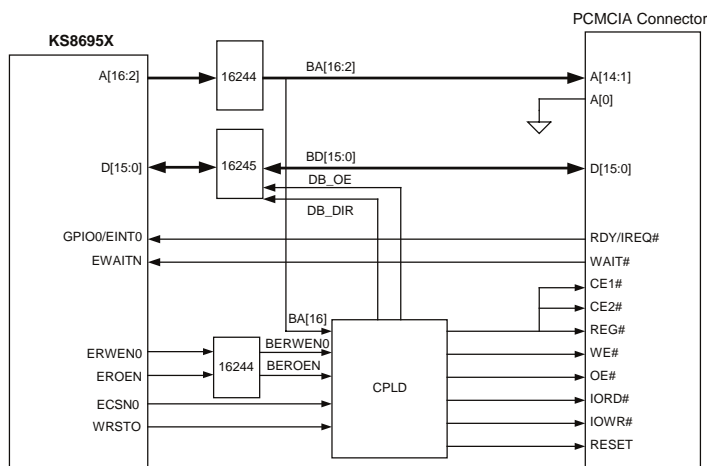


Figure 1. KS8695X Interface to PCMCIA

The address mapping as shown in Figure 1, is used so that software can make single 32-bit accesses to retrieve a 16-bit word. In this configuration, the address mapping is 4:1 for the 8-bit attribute space accesses and 2:1 for 16-bit I/O space accesses on the PCMCIA card. PCMCIA I/O memory read accesses are 16 bit, but in the case of write accesses, the software needs to cast the data as 32 bits.

A [0] on the PCMCIA connector is grounded since we are only interested in making 16 bit PCMCIA I/O space accesses. Please see the PCMCIA specification for more information on this interface.

There are 16-data bit connections between the KS8695X and the PCMCIA connector. These are made through 16245 bidirectional buffers. These buffers are required due to the load that the PCMCIA card adds to the data lines. If the WLAN chipset is placed directly on the board, the buffers are not necessary.

CPLD

The KS8695X WLAN reference board uses a low cost CPLD to implement the glue logic required to generate control signals to the PCMCIA connector and to the 16245 bidirectional buffers.

Figure 2 shows the simple logic used to generate these control signals.

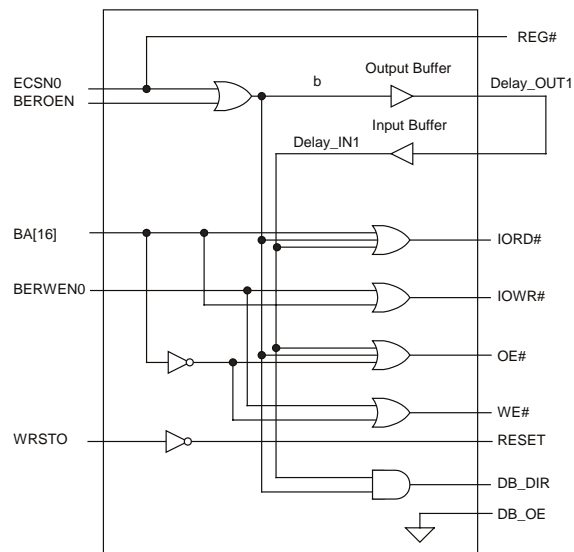


Figure 2. WLAN Signal Control Logic

| Voltage Rail | Current Consumption | Worst Case |
|--------------|--------------------------------------|--------------|
| ECSN0 | KS8695X External I/O Chip Select 0 | Active low |
| BA[16] | Buffered Address Bit 16 | N/A |
| BERWEN0 | Buffered KS8695X Byte 0 Write Enable | Active low |
| WRSTO | KS8695X Reset Output | Programmable |
| REG# | PCMCIA Attribute or I/O Space Select | Active low |
| IORD# | PCMCIA I/O Space Read Strobe | Active low |
| IOWR# | PCMCIA I/O Space Write Strobe | Active low |
| OE# | PCMCIA Output Enable | Active low |
| WE# | PCMCIA Write Enable | Active low |
| RESET | PCMCIA Reset | Active high |
| DB_DIR | Data Buffer (16245) Direction | N/A |
| DB_OE | Data Buffer Output Enable | Active low |

Table 1. CPLD Signal Descriptions

The KS8695X needs to make attribute space and I/O space accesses to the PCMCIA card. Since the REG# signal is always asserted during attribute space and I/O space accesses, it is connected to the KS8695X external I/O chip select ECSN0. Address bit BA[16] is used to differentiate between attribute space and I/O space.

IORD# and IOWR# are the read and write strobes to the PCMCIA I/O space. They are generated using BEROEN and BERWEN0 qualified appropriately with the BA[16] bit. If REG# is asserted low, OE# and WE# are the output enable and write enable signals for the PCMCIA attribute space. They are generated using the BEROEN and BERWEN0 signals qualified with the opposite polarity of the BA[16] signal. Note that BERWEN0 is the buffered write enable for the least significant bit of the KS8695X 32-bit data bus. ERWEN1 is also asserted during 16-bit writes to the PCMCIA interface; however, this signal is not required to generate write enables to the PCMCIA interface.

The WRSTO reset output on the KS8695X has programmable polarity, however the PCMCIA RESET signal is active high, whereas other resets in our system are active low. Thus, inversion of the signal in the CPLD is required. DB_DIR controls the direction of the bidirectional data buffer (16245).

The logic implemented dictates that when a read access is made to the PCMCIA, the direction of the buffer changes so that the buffer will accept data from the PCMCIA card as an input and output it to the KS8695X. The default mode is to accept data from the KS8695X as inputs and then output it to the PCMCIA card.

The logic has also been designed with a logical "AND" of the read access signal with a delayed version of itself. This ensures the buffer changes direction well within the bounds of the read access to prevent bus contention.

For additional support, contact your local Micrel Field Application Engineer or salesperson.

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