*TMS320 DSP*
*DESIGNER'S NOTEBOOK*

# *Reading a 16-Bit Bus With the TMS320C5x Serial Port*

*APPLICATION BRIEF: SPRA270*

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TEXAS INSTRUMENTS

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## Abstract

It is possible to read data directly from a parallel bus. Each word is loaded by a signal, for example /WE. In order to read this kind of word with a synchronous serial port, it has to be converted in series and synchronized by a transmission clock. The solution presented in this document uses the clock signal coming from the DSP, although an independent clock source could be implemented successfully. This solution contains two 8-bit registers instead of one single 16-bit register, such as a 74LS674, because if the bus is only 8 bits wide, you must remove one to adapt the device. A complete schematic of the solution is provided.

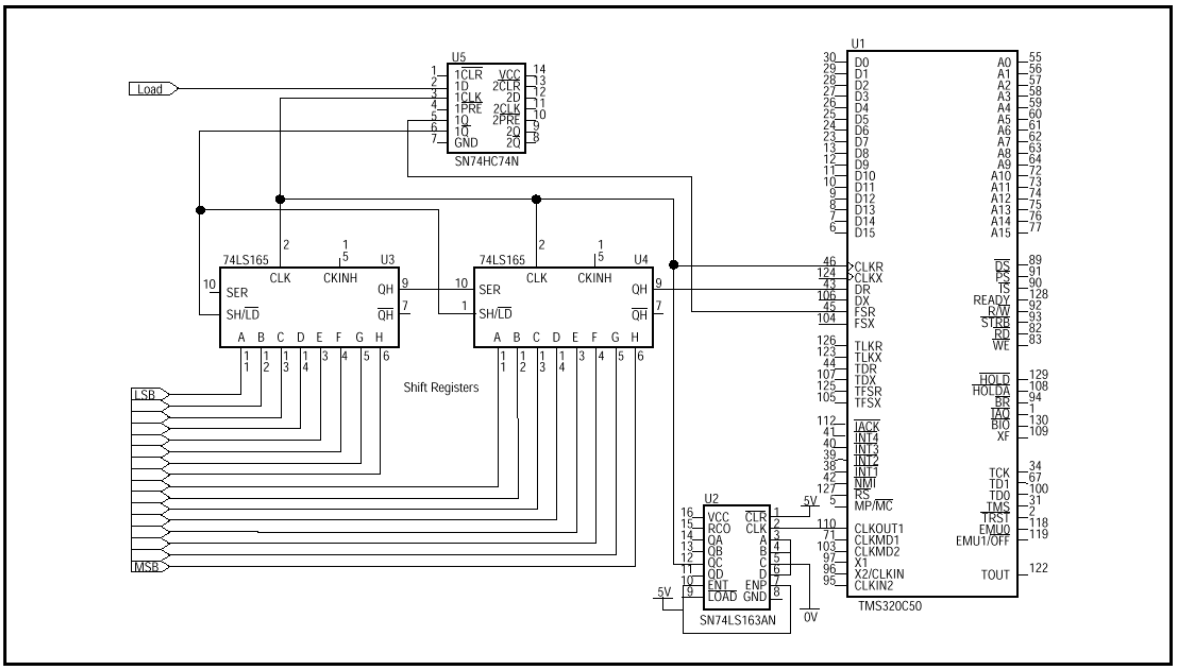
## Design Problem

How can I read a word from a 16-bit bus with the synchronous serial port of a TMS320C5x DSP?

## Solution

It is possible to compute data directly from a parallel bus. In this case, every word is loaded by a signal, for example /WE. In order to read this kind of word with a synchronous serial port, it has to be converted in series and synchronized by a transmission clock. The solution presented in Figure 1 uses the clock signal coming from the DSP, although an independent clock source could be implemented successfully. The following solution contains two 8-bit registers instead of one single 16-bit register, such as a 74LS674, because if the bus is only 8 bits wide, you must remove one to adapt the device.

*Figure 1. Connecting a 16-bit Bus to the TMS320C5x's Serial Port*



### Data Transmission on the Serial Port

The DSP's serial port, which runs in burst mode, consists of three types of signals: the clock (CLK), which imposes the pace of the bit sequence and which equals the bit rate of the communication; the frame synchro (FS), which indicates the beginning of a bit sequence, on a negative slope, to the other device; and finally, the data line (D), which conveys the bits. The bit rate and the synchro signal are imposed by the device. Data is transmitted and loaded MSB first and is right justified.

### Schematic Details

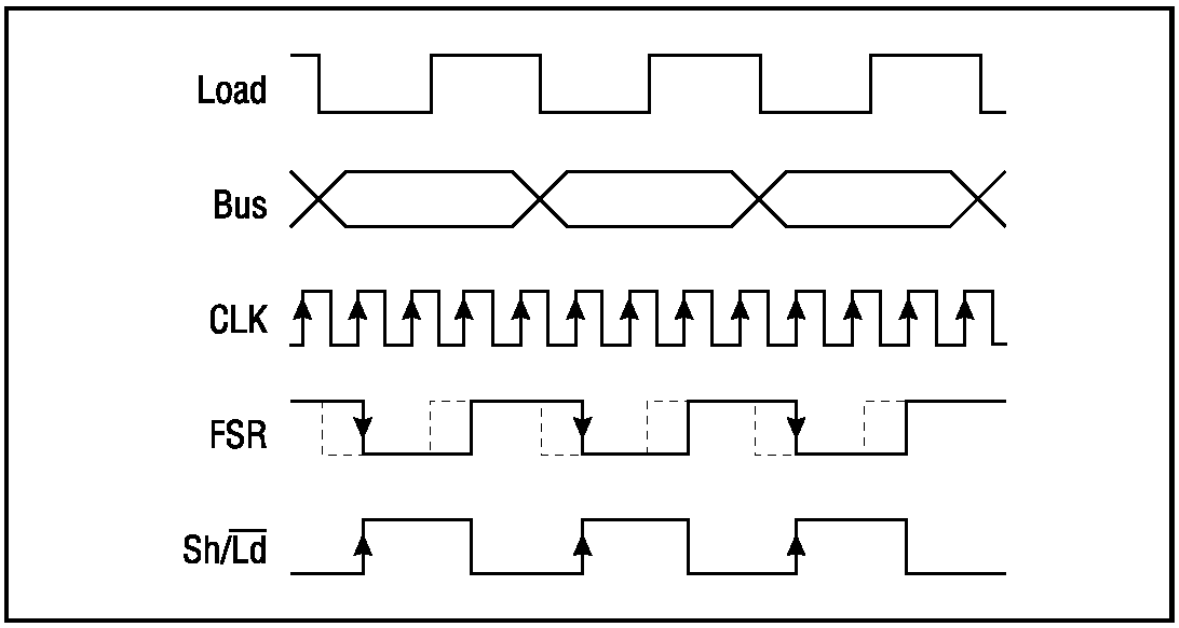
The clock out frequency from the DSP is 20 MHz. The maximum bit rate for data transmission through the serial port is 5 Mbit/s. Using the 74LS163 counter, the 20-MHz frequency is divided by 2 (QA), by 4 (QB), by 8 (QC), and by 16 (QD). So, we have three different bit rates: 1.25 MHz, 2.5 MHz, and 5 MHz. The choice of the rate depends on the loading frequency of the bus.

### Signal Principles

In our solution, a low state of load signal indicates that the bus is valid. This signal has to be synchronized by a positive clock slope, thanks to a '74 flip-flop before it enables the shift sequence, making the system fully synchronous. When the shift sequence begins, the FS signal performs a negative transition, which is done selectively by the inverted synchronous load signal by using it as the inverted output of the '74 flip-flop Sh/Ld (see Figure 2).

Two shift registers in cascade provide the parallel-to-serial conversion. If the bus is only 8 bits wide, you can remove one of the two registers. In this case, the 8-bit word will be inserted into the DSP's internal 16-bit word memory as the most significant bits (MSB). The other 8 bits will be set at the least significant bits (LSB) value.

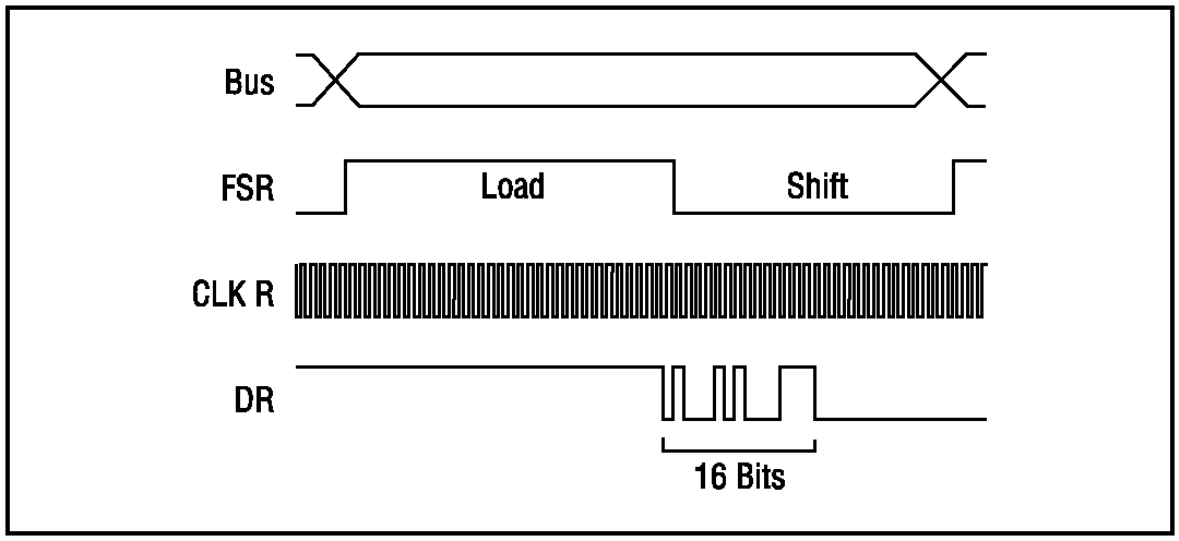
*Figure 2. Synchro principle*




**Constraints on the Loading Signal**

It is necessary that the bus value does not change during the shift sequence. The shift sequence duration is $T_{SH} = 16/F_{CLK}$. So, be aware that the Sh/ Ld signal is high during at least $T_{SH}$ whereas data on the bus is stable (see Figure 3).

*Figure 3. Typical Load/Shift Sequence*



### How to Choose the Right Bit Rate

One must also take into account that as the clock frequency is increased, distortion in the signal increases as well. This consideration might lower the maximum bit rate under 5 Mbit/s (maximum clock frequency for the DSP). On the other hand, it is possible to calculate the minimum bit rate $F_{CLK}$, knowing the frequency $F_{LD}$ and the duty cycle of the loading signal (active low).

$$F_{CLK} = F_{LD} \times 16 / \alpha$$