Application Report
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TI Power Management Solution for Freescale™ i.MX31

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ABSTRACT

This document details the voltage, current, and sequencing requirements for the i.MX31 and shows how to power it using the TPS650240.

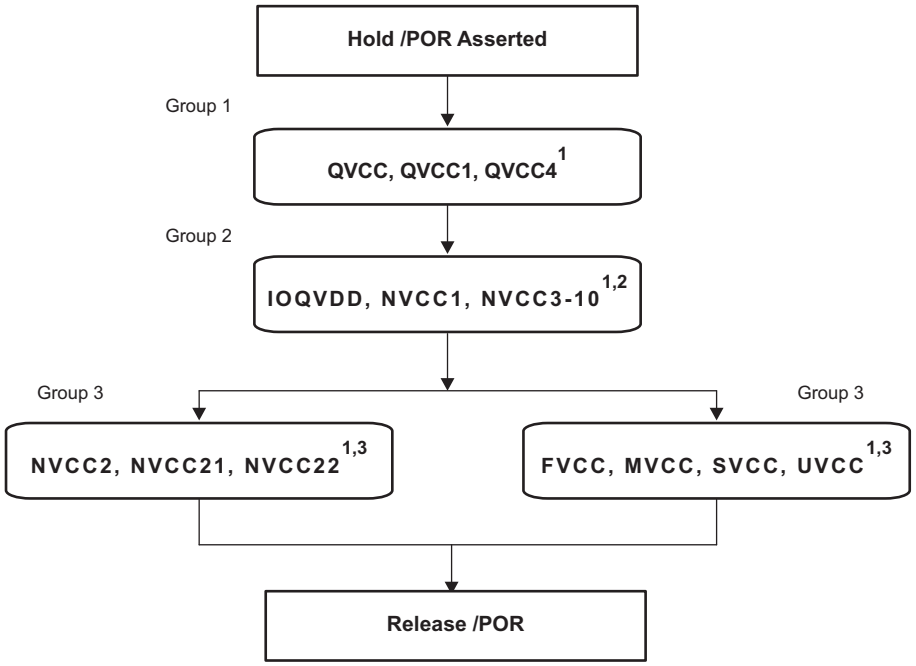
1 Original Supply Power-Up/Power-Down Requirements and Restrictions

As noted in the i.MX31 data sheet, any i.MX31 board design must comply with the power-up and power-down sequence guidelines in the following discussion in order to ensure reliable operation of the device. Any deviation from the sequence in the following discussion may lead to excessive current during the power-up phase, prevent the device from booting, or may cause irreversible damage to the processor.

1.1 Powering Up

The Power on Reset pin ($\overline{\text{POR}}$) must be kept asserted (low) throughout the power-up sequence. Power-up logic must ensure that all power sources reach their target values prior to the release of the $\overline{\text{POR}}$ pin. The Figure 1 shows the power-up sequence for silicon Revision 2.0.

The stages need to be performed in the order shown. However, within each stage, supplies can be powered up in any order. Note the restrictions within each stage.



(1) The board's design must ensure that supplies reach a 90% level before transition to the next state, using a power management IC or other means.

(2) The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.

(3) The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent.

Figure 1. Power-Up Sequence

1.2 Powering Down

For silicon revisions beginning with Revision 2.0, the power-down sequence has no special requirements.

1.3 Measurements for Power Up of the i.MX31P

Measurements were made on the development board in order to analyze the power-up sequencing required for the i.MX31. The signals that needed to be measured were short listed.

GROUP 1			GROUP 2	
QVCC	**QVCC**		IOQVDD	**1.8V_NVCC10**
QVCC1	**QVCC_ARM**		NVCC1	**1.8V_NVCC1**
QVCC4	**QVCC_L2**		NVCC3[2]	**NVCC3**
GROUP 3			NVCC4[2]	**NVCC4**
NVCC2	1.4V_DDR		NVCC5[2]	2.7V_NVCC5/NVCC8
NVCC21	1.4V_DDR		NVCC6[2]	2.7V_NVCC6/NVCC9
NVCC22	1.4V_DDR		NVCC7[2]	**1.8V_NVCC7**
FVCC	VCC_VDIG		NVCC8[2]	2.7V_NVCC5/NVCC8
MVCC	VCC_VDIG		NVCC9[2]	2.7V_NVCC6/NVCC9
SVCC	VCC_VDIG		NVCC10[2]	**1.8V_NVCC10**
UVCC	VCC_VDIG			

The following results were obtained for the power up of the i.MX31 processor using the MC13783 Power Management and Audio Component.

Figure 2 shows the timing diagram for all the relevant power-up signals.

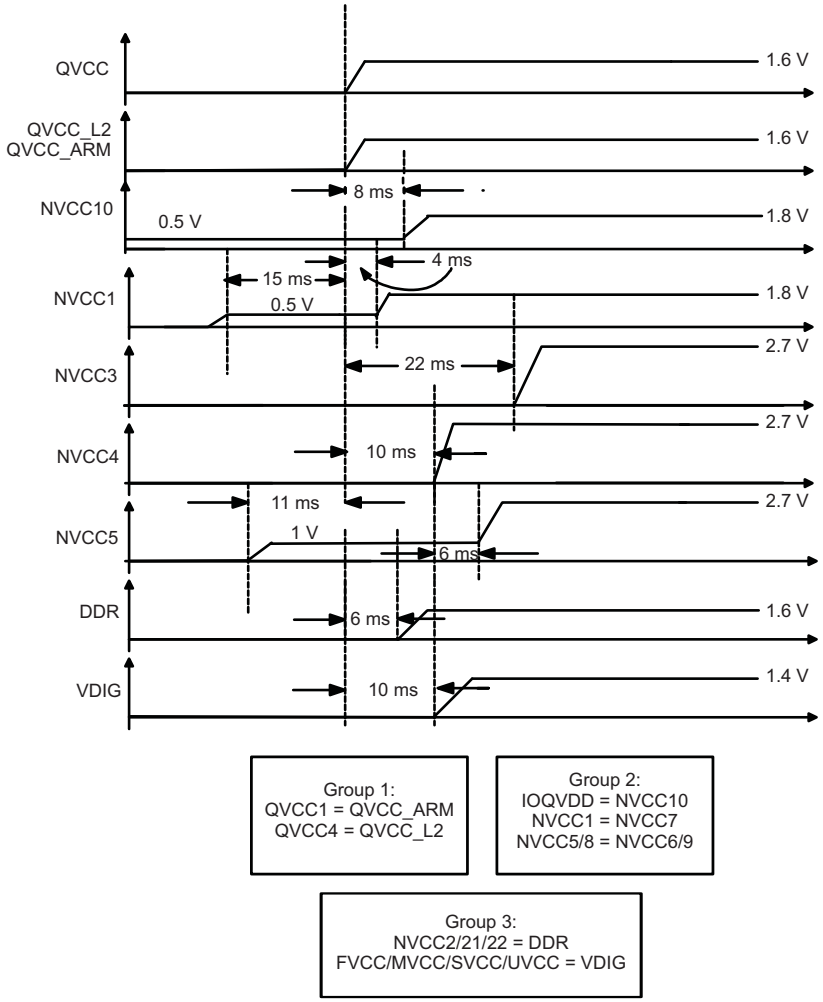


Figure 2. Power-Up of the i.MX31 Processor Timing Diagram

1.4 TI Solution for the i.MX31 Power-Up Sequence Using TPS650240

Figure 3 shows the proposed schematic for powering up the Freescale™ processor using TPS650240 power management integrated circuit (IC).

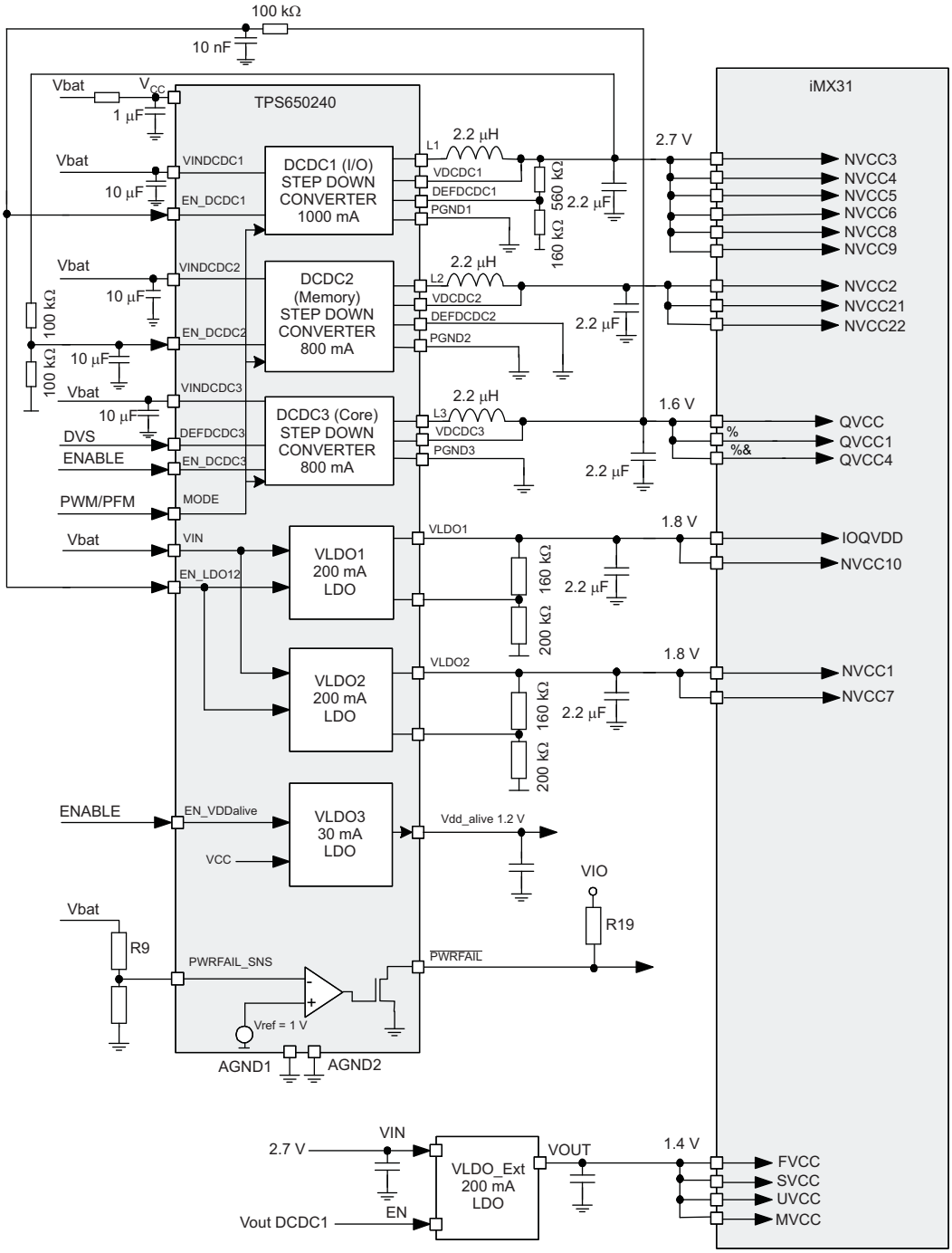
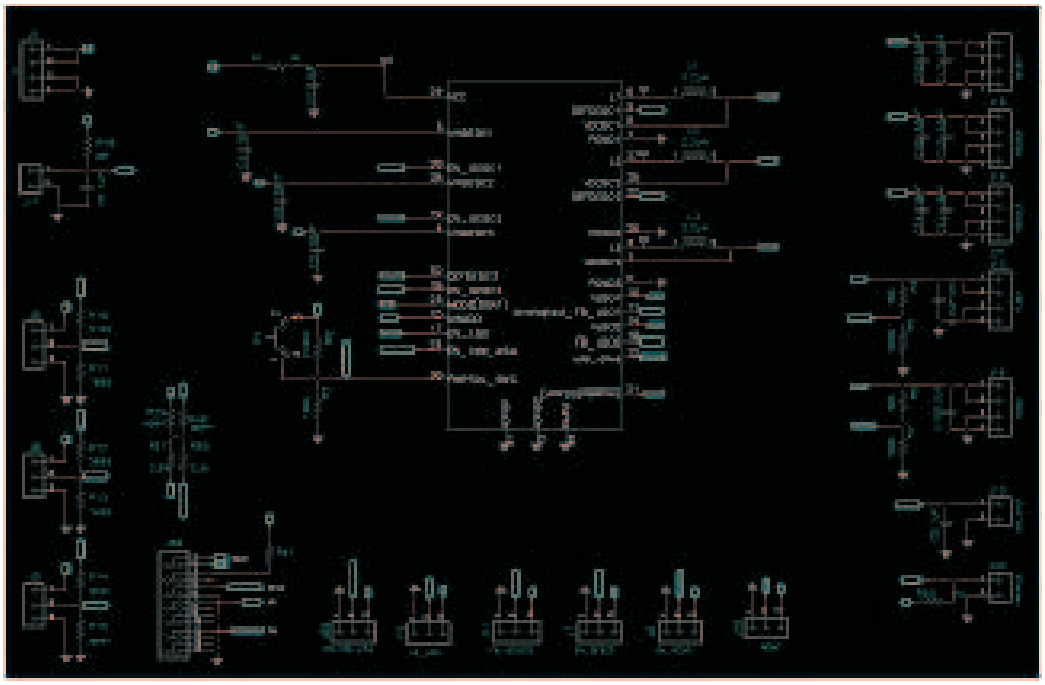
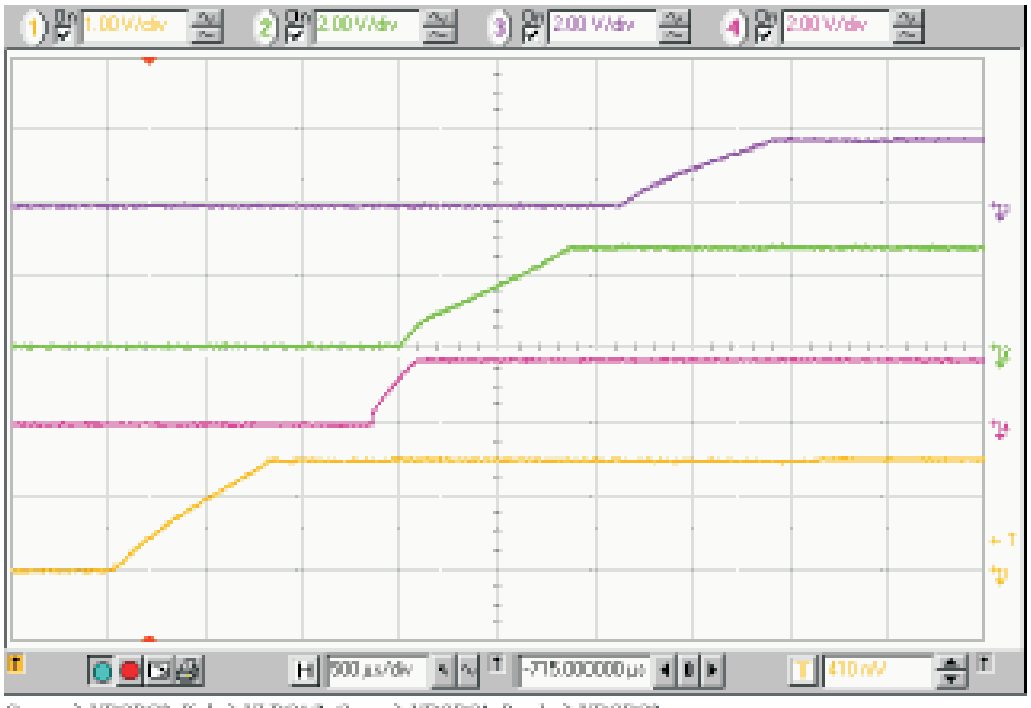


Figure 3. Proposed Schematic for i.MX31 Powering Using TPS650240

The EVM was soldered according to the following schematic, and measurements were made in order to analyze the TPS650240 output voltages and sequencing.



Signal analysis showed the following results for sequencing:



Orange→ VDCDC3, Pink→ VLDO1/2, Green→ VDCDC1, Purple→ VDCDC2

2 Summary

The TPS650240 devices provide voltages 1.5 V, 1.4 V, and 2.7 V for various signals in Groups 1, 2, and 3 of the sequencing scheme necessary for the powering up the i.MX31 multimedia application processor.

Step-down converter DCDC3 is enabled first to provide a 1.5-V signal for QVCC, QVCC1, and QVCC 4 as shown in Figure 3.

The output of DCDC3 also enables the LDOs, VLDO1 and VLDO2. It also simultaneously enables the step-down converter DCDC1. IOQVDD, NVCC1-10 are then triggered. The necessary output levels are achieved using different resistor values.

The output of DCDC1 enables DCDC2 and the external LDO, simultaneously. Thus, as required, NVCC2, NVCC21, NVCC22, FVCC, SVCC, MVCC, and UVCC are all triggered in the end.

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