

AN-EVAL3A1065ELJ

15W 5.0V SMPS Evaluation Board with
CoolSET[®] F3 ICE3A1065ELJ

Power Management & Supply



N e v e r s t o p t h i n k i n g .

Edition 2010-08-11

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15W 5V Demo board using ICE3A1065ELJ on board

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V1.1

Previous Version: 1.0

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1, 5, 11	Change demo board name to EVAL3A1065ELJ

15W 5.0V SMPS Evaluation Board with CoolSET® F3 ICE3A1065ELJ:
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Table of Contents	Page
1 Abstract.....	5
2 Evaluation Board.....	5
3 List of Features	6
4 Technical Specifications	6
5 Circuit Diagram	7
6 PCB Layout.....	9
6.1 Component side component legend	9
6.2 Solder side copper & component legend	9
7 Circuit Description	11
7.1 Introduction.....	11
7.2 Line Input.....	11
7.3 Start up & auxiliary supply circuit	11
7.4 RCD Clamper circuit	11
7.5 Peak primary current control circuit	11
7.6 Output Stage of secondary side.....	11
7.7 Feedback and regulation.....	12
7.8 Particular features	12
7.8.1 Blanking Window for Load Jump & Active Burst Mode.....	12
7.8.2 Active Burst Mode	12
7.8.3 Frequency jitter mode	12
7.9 Protection modes	13
7.9.1 Auto restart mode.....	13
7.9.2 Latch off mode.....	13
8 Component List.....	14
9 Transformer Construction.....	15
10 Test Results	16
10.1 Efficiency	16
10.2 Input Standby Power	17
10.3 Line Regulation	18
10.4 Load Regulation	19
10.5 Max. Overload Output Power.....	19
10.6 Electrostatic Discharge Test (ESD).....	20
10.7 Lightning Surge Test.....	20
10.8 Conducted EMI Test	20
11 Waveforms and scope plots	22
11.1 Startup @ low and high AC line input voltage and 15W load	22
11.2 Drain to source voltage and current during 15W load operation	23
11.3 Load transient response (Load jump from 10% to 100%)	23
11.4 AC output ripple during 15W	24
11.5 Active Burst Mode @ light load	25
11.6 Vcc overvoltage protection (latch off mode).....	26
11.7 Overload protection without/with extended blanking time (auto restart mode).....	27
11.8 Open loop protection (auto restart mode)	28
11.9 Vcc under voltage/Short optocoupler protection (auto restart mode)	28
11.10 External latch off enable.....	29
11.11 Frequency Jittering.....	29
12 Appendix	30
12.1 Slope compensation for CCM operation	30
13 References	30

1 Abstract

This document is an engineering report that describes a universal input power supply designed in a 5V 15W off line SMPS flyback converter topology that utilizes the ICE3A1065ELJ CoolSET[®]¹. The application board is designed for discontinuous conduction mode (DCM) with current mode controller IC and running at 100 kHz switching frequency. It has one output voltage with secondary control regulation. It is especially suitable for small power supply such as DVD player, set-top box, game console, charger and auxiliary power for high power system, etc. The ICE3A1065ELJ is an enhanced version of the F3 CoolSET[®] especially in robustness to the system noise such as ESD, lightning surge, etc. Besides having the basic features of the F3 CoolSET[®] such as Active Burst Mode, propagation delay compensation, soft gate drive, latch off protection for serious fault (Vcc OVP, OTP and short winding) and auto-restart protection for general fault (OLP and Open loop), etc., it also has the BiCMOS technology design, built-in soft start time, built-in and extendable blanking time, frequency jitter feature with built-in jitter period and external latch enable pin, etc. The particular good features are the extremely low standby input power, the low EMI performance and the robustness to the system noise.

2 Evaluation Board

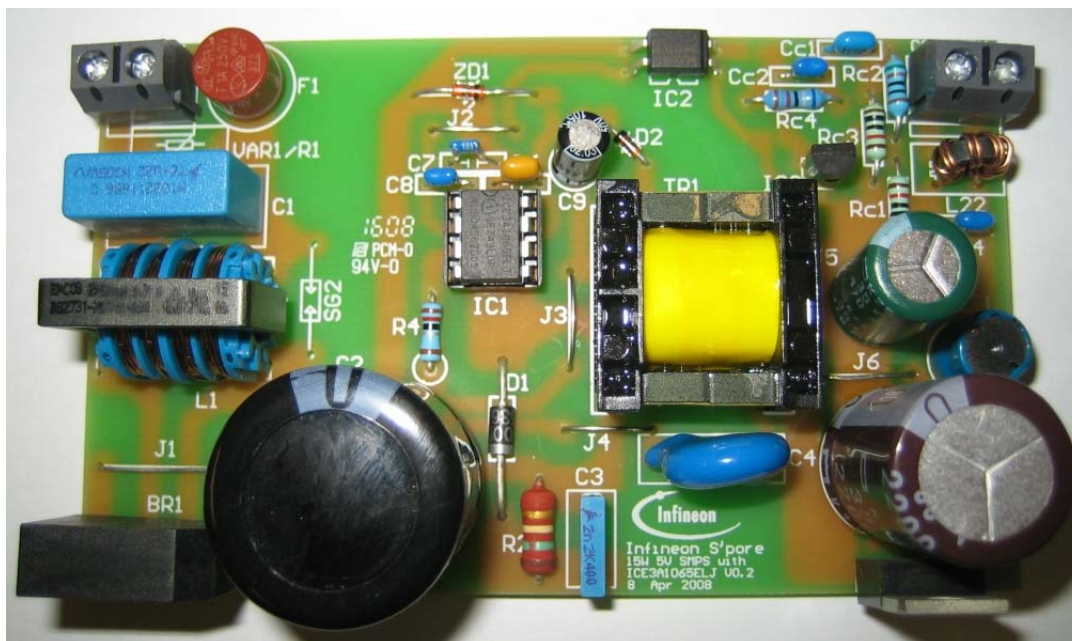


Figure 1 – EVAL3A1065ELJ

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction drawing. Typical operating characteristics are presented at the rear of the report and it consists of performance curves and scope waveforms.

¹ CoolSET[®] is a current mode PWM control IC and the power MOSFET CoolMOS[®] within one package designed for low cost switch mode power supplies (SMPS).

3 List of Features

650V avalanche rugged CoolMOS® with built-in Startup Cell
Active Burst Mode for lowest Standby Power
Fast load jump response in Active Burst Mode
100kHz internally fixed switching frequency
Built-in latched Off Mode for Overtemperature, Overvoltage & Short Winding Detection
Auto Restart Mode for Overload, Open Loop & VCC Undervoltage
Built-in Soft Start
Built-in and extendable blanking Window for short duration high current
External latch enable function
Max Duty Cycle 75%
Overall tolerance of Current Limiting < $\pm 5\%$
Internal PWM Leading Edge Blanking
BiCMOS technology provide wide VCC range
Frequency jitter and soft driving for low EMI
Robustness to system noise such as ESD, lightning surge, etc.

4 Technical Specifications

Input voltage	85VAC~265VAC
Input frequency	50Hz, 60Hz
Input Standby Power	<100mW @ no load; < 0.8W @ 0.5W load
Output voltage and current	5V +/- 2%
Output current	3.0A
Output power	15W
Efficiency	>75% at full load
Output ripple voltage	< 50mVp-p

5 Circuit Diagram

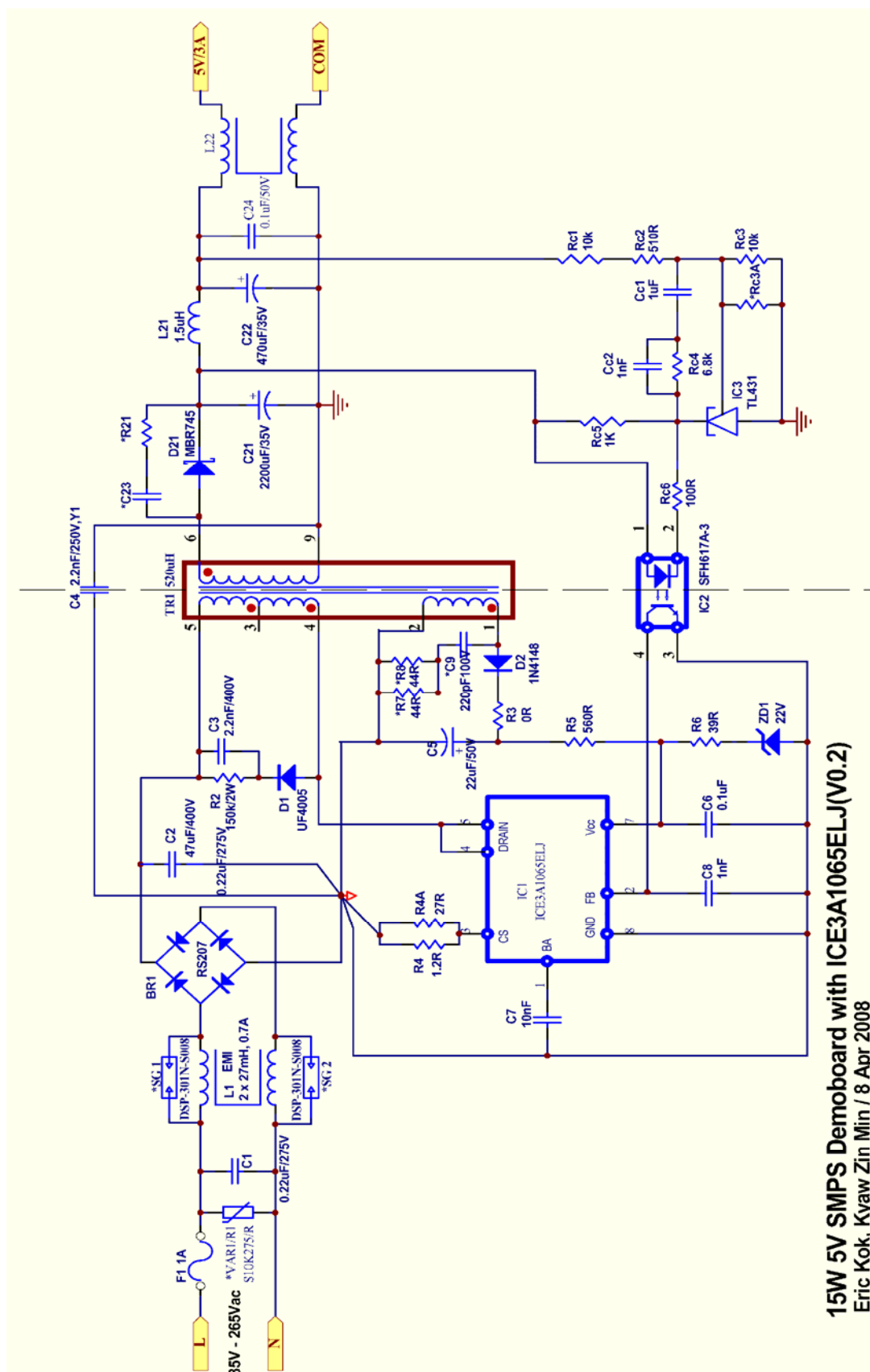


Figure 2 – 15W 5.0V ICE3A1065ELJ power supply Schematic

N.B. : In order to get the optimized performance of the CoolSET[®], the grounding of the PCB layout must be connected very carefully. From the circuit diagram above, it indicates that the grounding for the CoolSET[®] can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be connected to the bulk capacitor ground separately.

- Signal ground includes all small signal grounds connecting to the CoolSET[®] GND pin such as filter capacitor ground, C6, C7, C8 and optocoupler ground.
- Vcc ground includes the Vcc capacitor ground, C9 and the auxiliary winding ground, pin 2 of the power transformer.
- Current Sense resistor ground includes current sense resistor R4 and R4A.
- EMI return ground includes Y capacitor, C4.

6.1 Component side component legend

Figure 3 – Component side Component Legend – View from Component Side

6.2 Solder side copper & component legend

Figure 4 – Solder side copper – View from Component Side

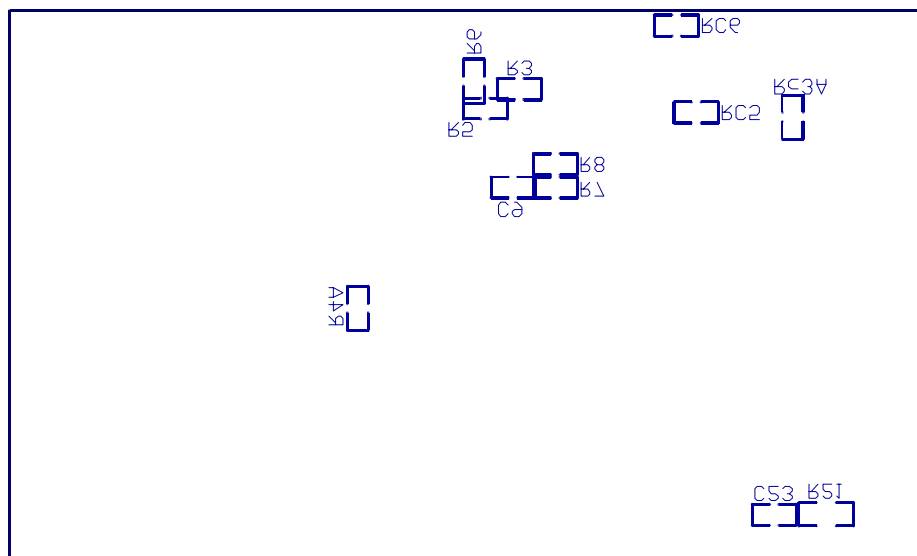


Figure 5 – Solder side component Legend – View from Component Side

7 Circuit Description

7.1 Introduction

The EVAL3A1065ELJ demoboard is a low cost off line flyback switch mode power supply (SMPS) using the ICE3A1065ELJ system IC from the CoolSET®-F3 family. The circuit, shown in Figure 2, details a 5.0V, 15W power supply that operates from an AC line input voltage range of 85Vac to 265Vac, suitable for applications requiring either an open frame supply or an enclosed adapter.

7.2 Line Input

The AC line input side comprises the input fuse F1 as over-current protection. The common mode choke L1, X2-capacitor C1 and Y1-capacitor C4 act as EMI suppressors. Spark gap device SG1 and SG2 can absorb high voltage stress during lightning surge test. After the bridge rectifier BR1 and the input bulk capacitor C2, a voltage of 100 to 380 V_{DC} is present which changed with input voltage.

7.3 Start up & auxiliary supply circuit

Since there is a built-in startup cell in the ICE3A1065ELJ, there is no need for external start up resistor. The startup cell is connecting the Drain pin of the IC. Once the voltage is built up at the Drain pin of the ICE3A1065ELJ, the startup cell will charge up the Vcc capacitor C5 and C6. When the Vcc voltage exceeds the UVLO at 18V, the IC starts up. Then the Vcc voltage is bootstrapped by the auxiliary winding to sustain the operation.

During operation, the Vcc pin is supplied via a separate transformer winding with associated rectification D2 and buffering C5 and C6. Resistor R3 & R5 is used for current limiting. In order not to exceed the maximum voltage at Vcc pin an external zenor diode ZD1 and resistor R6 are added.

The Soft-Start is a built-in function and is set at 20ms. There is no need for extra components.

7.4 RCD Clamper circuit

While turning off the internal CoolMOS®, the clamper circuit R2, C3 and D1 absorbs the current caused by transformer leakage inductance once the voltage exceeds clamper circuit voltage. Then the Drain to Source voltage is well below the maximum break down voltage ($V_{(BR)DSS} = 650V^1$) of internal CoolMOS®.

7.5 Peak primary current control circuit

The drain to source current of the internal CoolMOS® is sensed via external shunt resistors R4 and R4A. An accurate value of the shunt together with the IC's propagation delay compensation control can effectively improve the peak power control between high line and low line which is shown in the peak power limitation curve in the rear part of the report.

7.6 Output Stage of secondary side

On the secondary side of the system the power is coupled out by a schottky diode D21. The capacitor C21 provides energy buffering following with the LC filter L21 and C22 to reduce the output voltage ripple considerably. Storage capacitor C21 is a high ripple current electrolytic capacitor which has a very low ESR and can reduce the output voltage ripple. L22 and C24 can help to suppress the high transient voltage spike during Electrostatic Discharge (ESD) test.

¹ $V_{(BR)DSS} = 650V @ T_j = 110^\circ C$

7.7 Feedback and regulation

The output voltage is controlled using a TL431 reference diode IC (IC3). This device incorporates the voltage reference as well as the error amplifier and a driver stage. Compensation network Cc1, Cc2, Rc1, Rc2, Rc3, Rc3A and Rc4 constitute the external circuitry of the error amplifier of IC3. This circuitry allows the feedback to be precisely matched to dynamically varying load conditions, thereby providing stable control. The maximum current through the optocoupler diode and the voltage reference is set by using resistors Rc5 and Rc6. Optocoupler IC2 is used for floating transmission of the control signal to the "Feedback" input via capacitor C8 of the ICE3A1065ELJ control device. The selected optocoupler meets DIN VDE 884 requirements for a wider creepage distance. C8 is a noise filtering capacitor. It should be as small as possible so that it can reduce the noise and at the same time provide fast response to the output.

7.8 Particular features

7.8.1 Blanking Window for Load Jump & Active Burst Mode

In case of Load Jumps the Controller provides a Blanking Window before activating the Over Load Protection. There are 2 modes for the blanking time setting; basic mode and the extendable mode. If there is no capacitor added to the BL pin, it would fall into the basic mode; i.e. the blanking time is set at 20ms. If a longer blanking time is required, it should go to the extendable mode, where a capacitor, C7 should be added to BL pin. The extended blanking time can be achieved by charging the C7 at BL pin from 0.9V to 4.0V with an internal 8.4uA constant current source. Thus the overall blanking time is the addition of 20ms and the extended time. For example, C7=10nF, I_{BK} (internal current source)=8.4uA. The voltage at Feedback pin will rise up to exceed 4.5V without switching off the IC under over load condition when it is within the blanking time frame. At that period the transferred power is limited to the maximum peak current defined by the value of the current sense resistor, R4 and R4A.

Blanking time (total) = 20ms + $C7 \times (4-0.9)/I_{BK} = 23.7\text{ms}$

Note: A noise filtering capacitor (at least 100pF) may be needed to add to the BL pin if the noises cannot be avoided to enter that pin in the physical PCB layout. Otherwise, some protection features may be mis-triggered and the system may not be working properly.

The blanking time to enter the Active Burst Mode is built-in 20ms with no extension. If a low load condition is detected when V_{FB} is falling below 1.35V, the system will only enter Active Burst Mode after 20ms blanking time while V_{FB} is still below 1.35V.

7.8.2 Active Burst Mode

At light load condition, the SMPS enters into Active Burst Mode. The controller is always active at this state. V_{CC} must be designed higher than the Vcc switch off threshold $V_{CCoff} \geq 10.5\text{V}$. While supporting low ripple on V_{OUT} and fast response on load jump, efficiency also increased significantly during Active Burst Mode. When the voltage level at FB falls below 1.35V, the internal blanking timer starts to count. When it reaches 20ms and the FB voltage is still below 1.35V, it will enter Active Burst Mode. The Blanking Window is generated to avoid a sudden entering of Burst Mode due to load jump.

During Active Burst Mode the current sense voltage limit is reduced from 1V to 0.31V so as to reduce the conduction losses. All the internal circuits are switched off except the reference and bias voltages to reduce the total V_{CC} current consumption to below 0.45mA. At burst mode, the FB voltage is changing like a sawtooth between 3.0 and 3.61V. To leave Burst Mode, FB voltage must exceed 4.5V. It will reset the Active Burst Mode and turn the SMPS into Normal Operating Mode. Maximum current can then be provided to stabilize V_{OUT} .

7.8.3 Frequency jitter mode

The ICE3A1065ELJ has frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set at 100 kHz +/-4 kHz and the jitter period is set at 4ms.

7.9 Protection modes

There are two kinds of protection modes for the device; auto-restart mode and the latch-off mode. The auto-restart mode is for the general fault and the latch off mode is for the serious fault.

7.9.1 Auto restart mode

In the auto-restart mode, the gate switching is stopped and the Vcc voltage will drop. When it drops to 10.5V, the startup cell will turn on and charge up the Vcc capacitor to 18V. Then the startup cell turns off and the device will start the start up phase from soft start. However, if the fault persists, the device will enter the auto-restart mode again. If the fault is removed, the device will return to normal mode in the next start up phase. A list of auto restart mode protections and the failure conditions are showed in the below table.

Protection function	Failure condition	Protection Mode
Over-load / Open loop	$V_{FB} > 4.5V$ and $V_{BL} > 4.0V$ (Blanking time counted from charging V_{BA} from 0.9V to 4.0V together with the basic 20ms)	Auto Restart
Vcc Under-voltage / short Optocoupler	$V_{CC} < 10.5V$	Auto Restart

7.9.2 Latch off mode

The operation of latch-off mode is very similar to auto-restart mode but there is no startup phase when the Vcc reach 18V. Since there is no switching energy from the auxiliary winding, the Vcc voltage will then drop to 10.5V. Then the startup cell charge sequence repeats again. The Vcc waveform during latch-off mode likes a saw-tooth shape. The latch-off mode can be reset if the Vcc voltage is lower than 6.23V. A list of latch off mode protections and the failure conditions are showed in the below table.

Protection function	Failure condition	Protection Mode
Vcc Over-voltage	$V_{CC} > 24V$ & $V_{FB} > 4.5V$	Latch Off
Over-temperature (controller junction)	$T_J > 130^{\circ}C$	Latch Off
Short Winding/Short Diode	$V_{CS} > 1.66V$	Latch Off
External latch enable	$V_{BL} < 0.1V$	Latch Off

8 Component List

Items	Part	Type	Quantity	Manufacturer
1	BR1	RS207, 2A 1000V	1	-
2	C1	0.22uF/275V, X2 capacitor	1	EPCOS
3	C2	47uF/400V	1	EPCOS
4	C3	2n2F/400V	1	EPCOS
5	C4	2.2nF/250V, Y1 capacitor	1	-
6	C6	0.1u/50V	1	Murata
7	C7	10nF/50V	1	EPCOS
8	C8	1nF/50V	1	EPCOS
9	C9	22u/50V	1	-
10	C21	2200uF/35V	1	-
11	C22	470uF/35V	1	-
12	C24	0.1uF/50V	1	Murata
13	Cc1	1uF/50V	1	Murata
14	Cc2	1nF/50V	1	EPCOS
15	D1	UF4005	1	-
16	D2	1N4148	1	-
17	D21	MBR745	1	-
18	F1	1A 250V	1	-
19	IC1	ICE3A1065ELJ	1	Infineon
20	IC2	SFH617A-3 1	1	-
21	IC3	TL431CLP	1	-
22	J1, J2, J3, J4, J5, J6	Jumper	6	-
23	L1	2 x 27mH, 0.7A	1	EPCOS
24	L21	1.5uH	1	NEC-Tokin
25	L22	2 x 100uH, (μi=10000, T38, R 6.30)	1	EPCOS
26	R2	150K, 2W, 5%	1	-
27	R3	0R, (SMD 0805)	1	ROHM
28	R4	R4 1.2R, 0.5W, 1%	1	-
29	R4A	27R, 0.1W, 5% (0805 SMD)	1	ROHM
30	R5	560R, 0.1W, 5% (0805 SMD)	1	ROHM
31	R6	39R, 0.1W, 5% (0805 SMD)	1	ROHM
32	Rc1	10K, 0.25W, 1%	1	-
33	Rc2	510R, 0.25W, 1%	1	-
34	Rc3	10K, 0.25W, 1%	1	-
35	Rc4	6.8K, 0.25W, 5%	1	-
36	Rc5	1K, 5% (0805 SMD)	1	ROHM
37	Rc6	100R, 5% (0805 SMD)	1	ROHM
38	TR1	EF20, N87, Lp=520uH	1	EPCOS
39	ZD1	22V zener diode	1	-

9 Transformer Construction

Core and material: EF20/10/6, N87

Bobbin: Horizontal type

Primary Inductance, $L_p = 520\mu\text{H}$ measured between pin 4 and pin 5 (Gapped to Inductance)

Transformer structure:

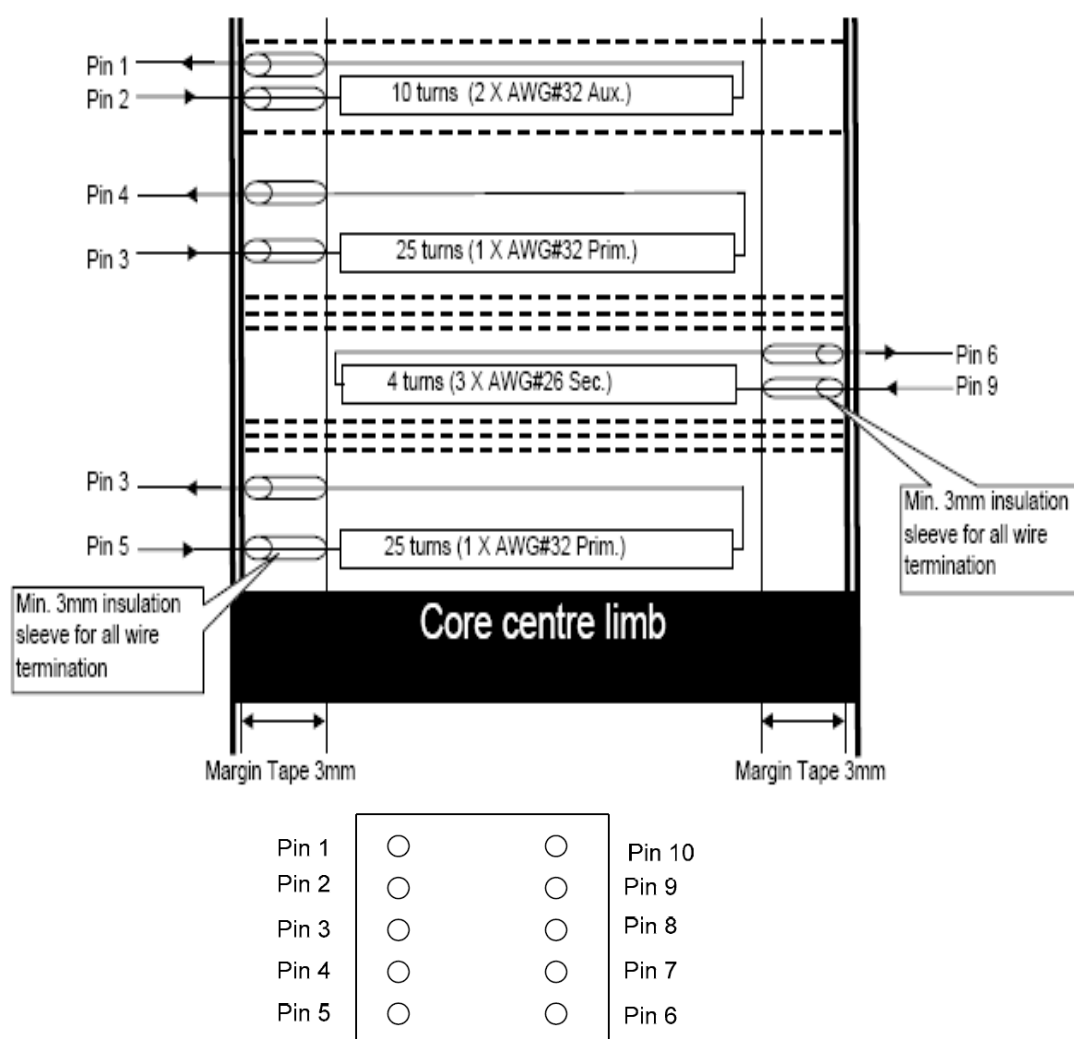


Figure 6 – Transformer structure and top view of transformer complete

Wire size requirement:

Start	Stop	No. of turns	Wire size	Layer
2	1	10	2XAWG#32	Auxiliary
3	4	25	1XAWG#32	$\frac{1}{2}$ Primary
9	6	4	3XAWG#26	Secondary
5	3	25	1XAWG#32	$\frac{1}{2}$ Primary

10 Test Results

10.1 Efficiency

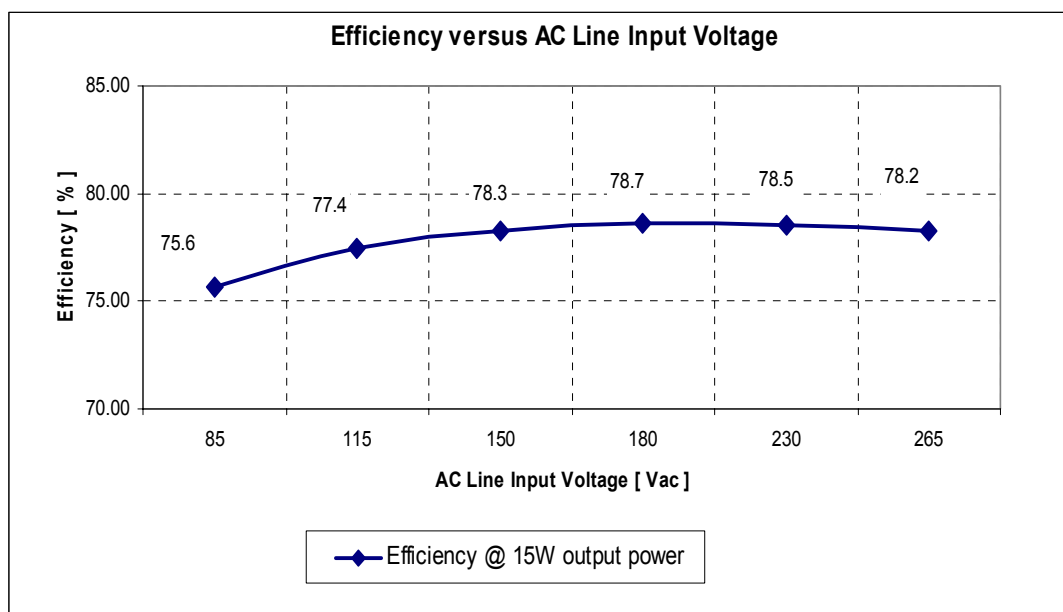


Figure 7 – Efficiency versus AC Line Input Voltage

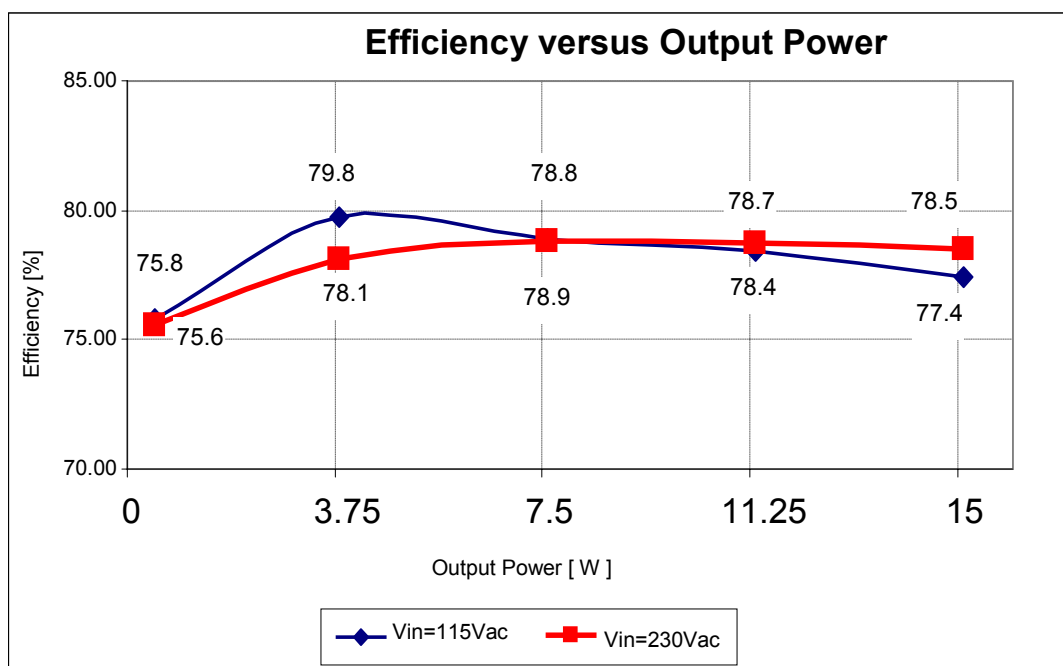


Figure 8 – Efficiency vs. Output Power @ 115 & 230 Vac

10.2 Input Standby Power

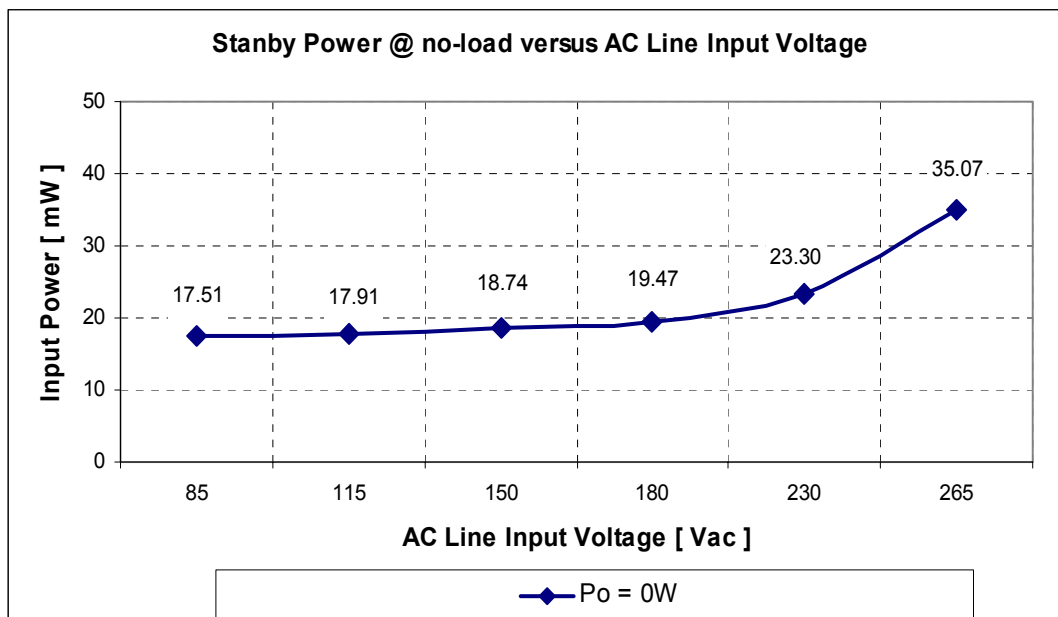


Figure 9 – Input Standby Power @ no load vs. AC Line Input Voltage (measured by Yokogawa WT210 power meter – integration mode)

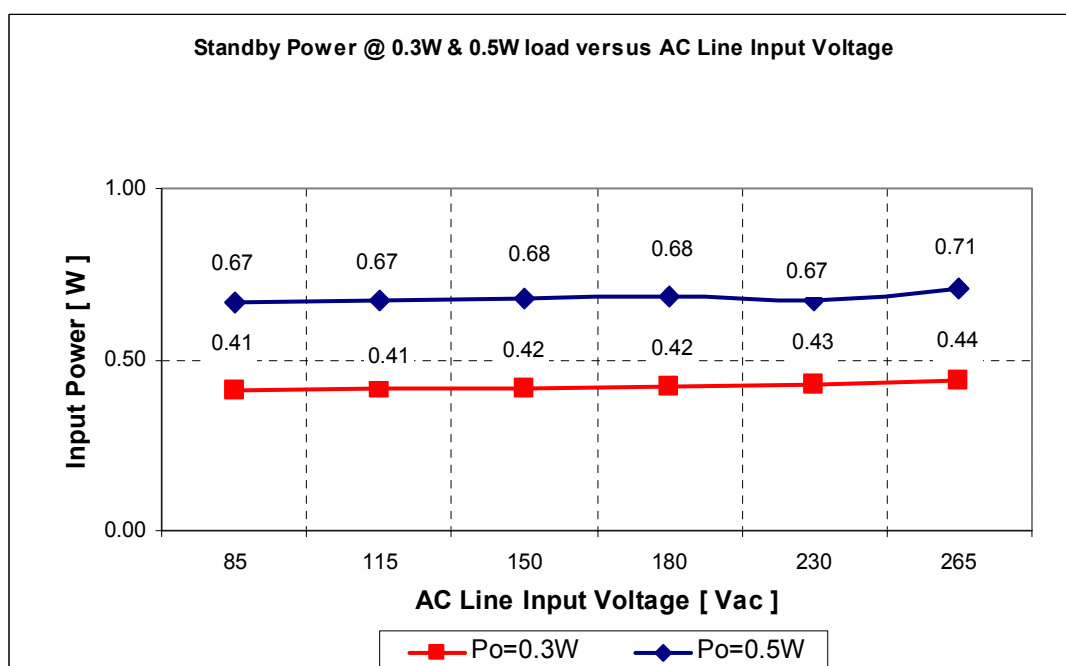


Figure 10 – Input Standby Power @ 0.3 and 0.5W load vs. AC Line Input Voltage (measured by Yokogawa WT210 power meter – integration mode)

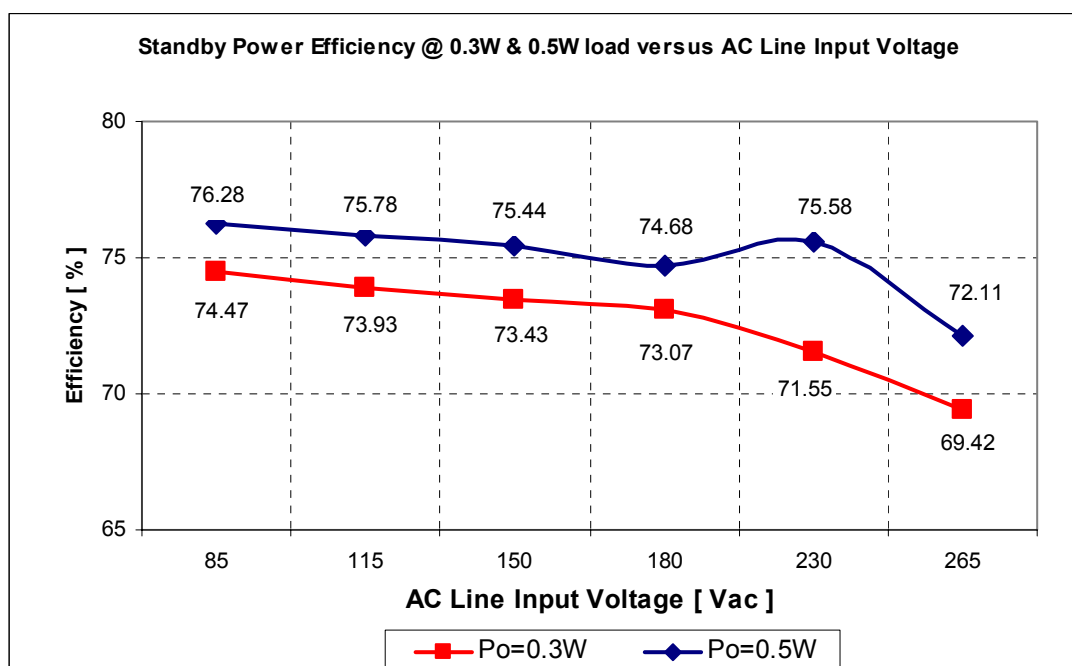


Figure 10 – Input Standby Power efficiency @ 0.3 and 0.5W load vs. AC Line Input Voltage

10.3 Line Regulation

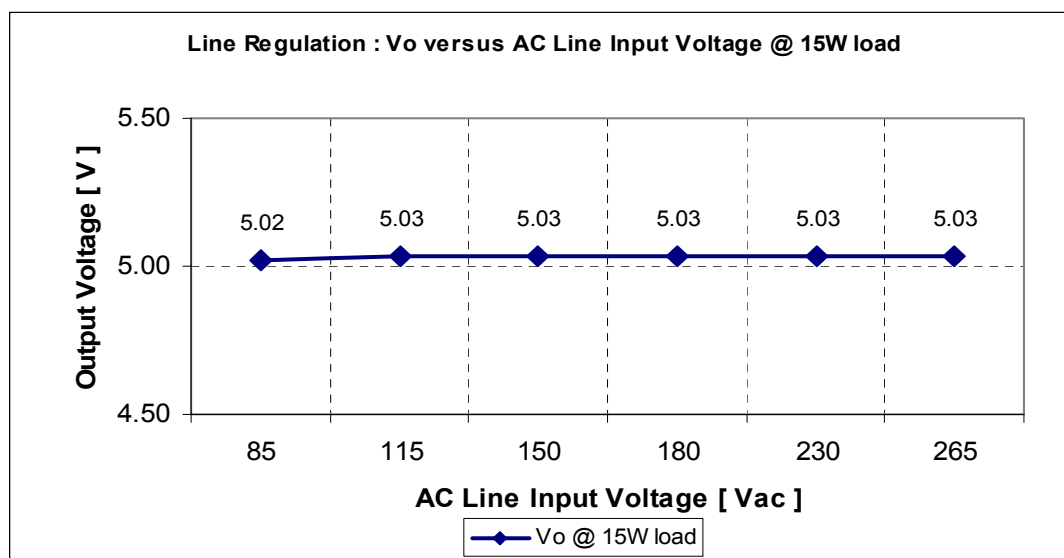


Figure 11 – Line Regulation vs. AC Line Input Voltage

10.4 Load Regulation

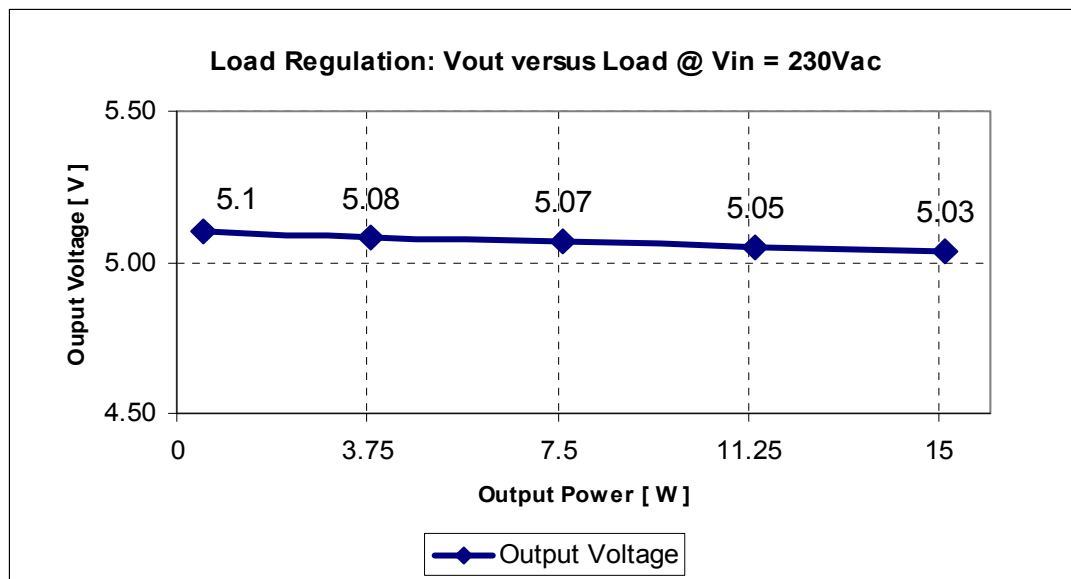


Figure 12 – Load Regulation vs. AC Line Input Voltage

10.5 Max. Overload Output Power

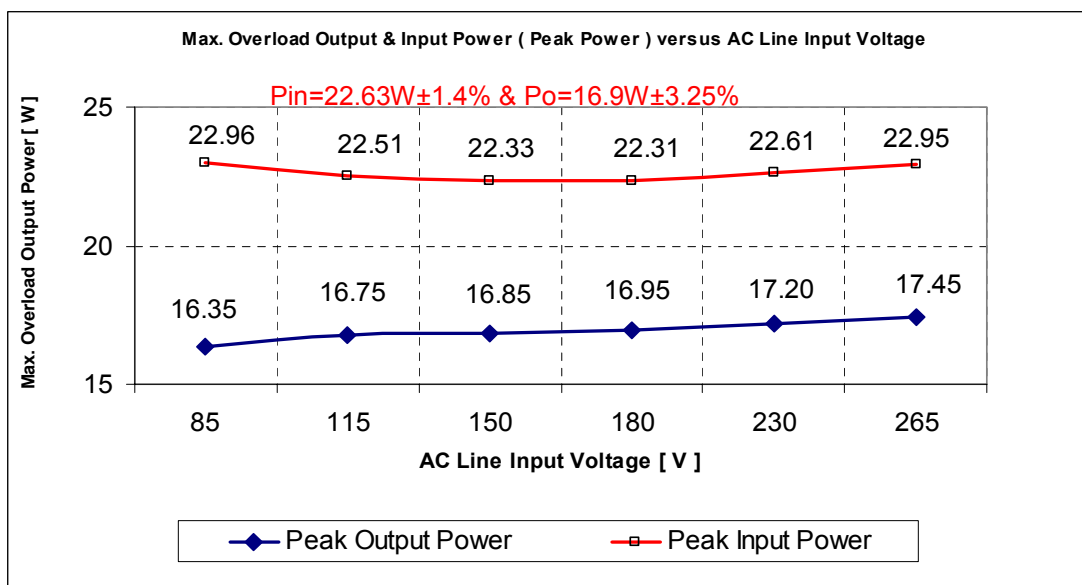


Figure 13 – Maximum Overload Output & Input Power vs. AC Line Input Voltage

10.6 Electrostatic Discharge Test (ESD)

Pass 20kV ESD test (EN61000-4-2) in contact discharge.

10.7 Lightning Surge Test

Pass 8kV lightning surge test (EN61000-4-5) in Line to Earth.

* With the addition of SG1 & SG2 (DSP-301N-S008).

10.8 Conducted EMI Test

Pass CISPR 22 Class B EMI test.

The conducted EMI was measured by Schaffner (SMR4503) receiver under CISPR 22 class B test standard. The demo board was tested with maximum load (15W) with input voltage of 115Vac and 230Vac.

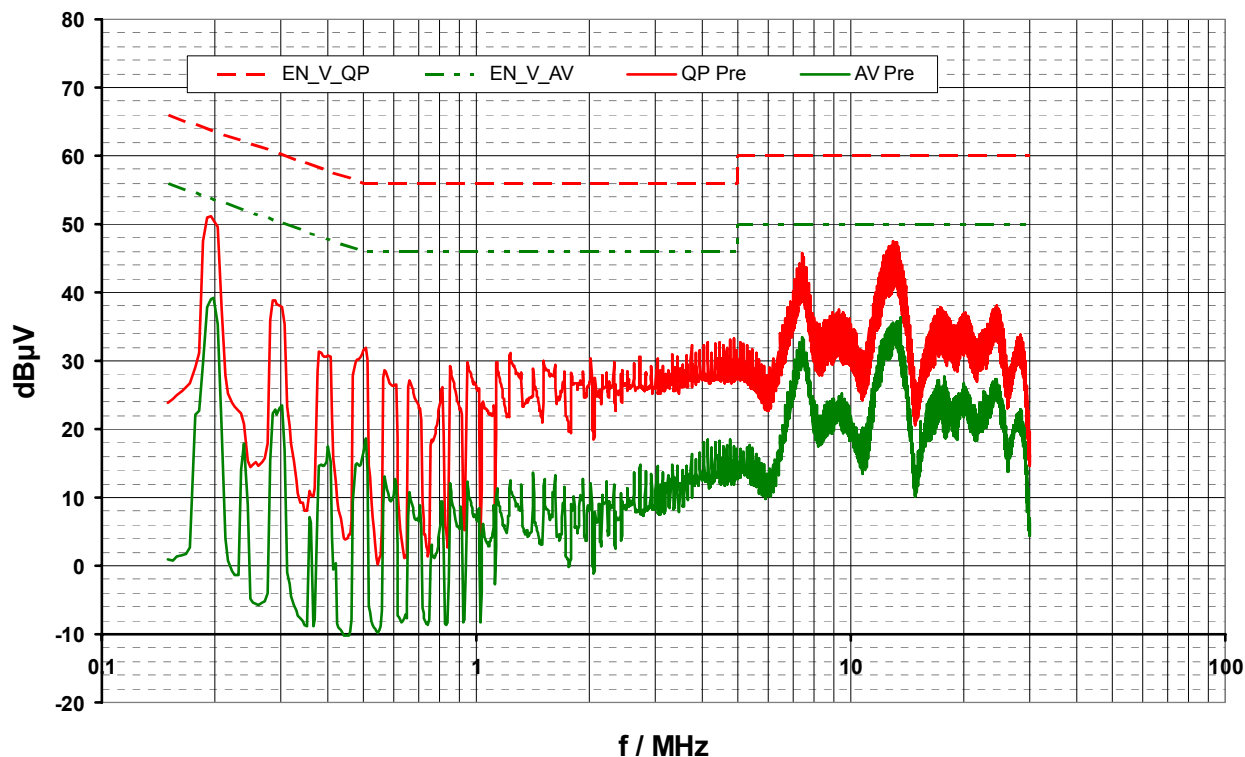


Figure 14 – Max. Load (15W) with 115 Vac (Line)

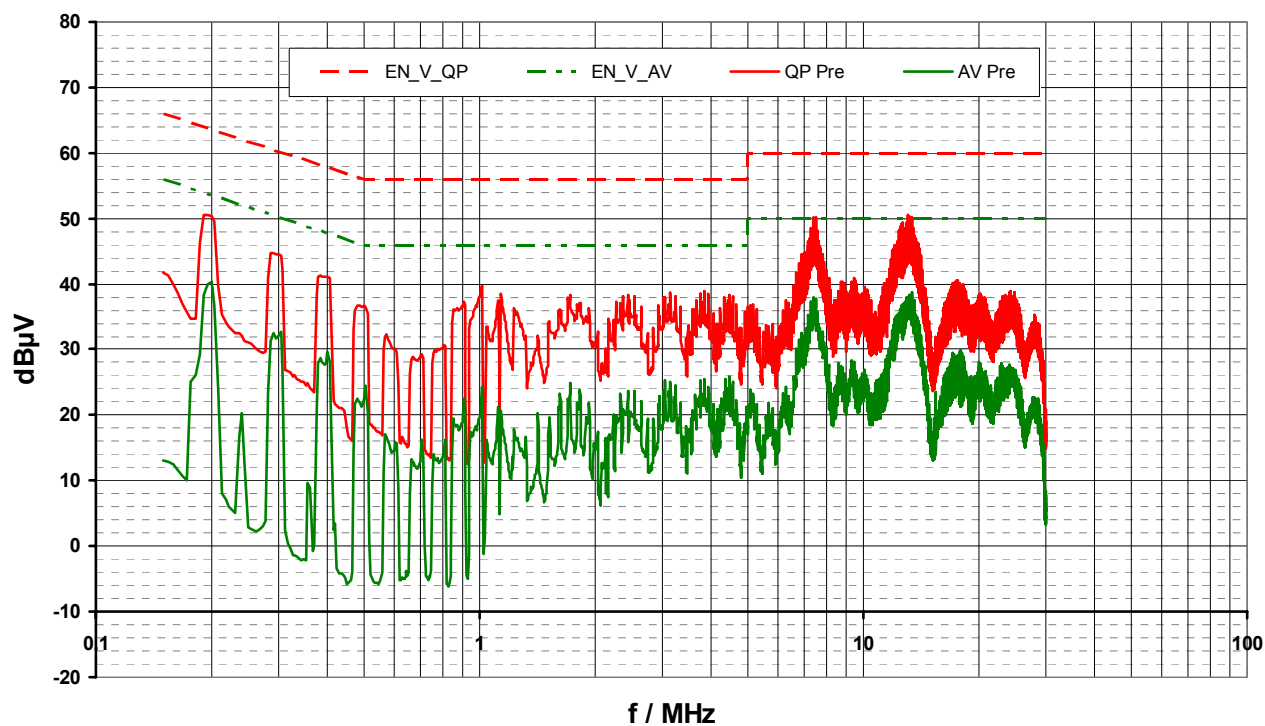


Figure 15 – Max. Load (15W) with 230 Vac (Neutral)

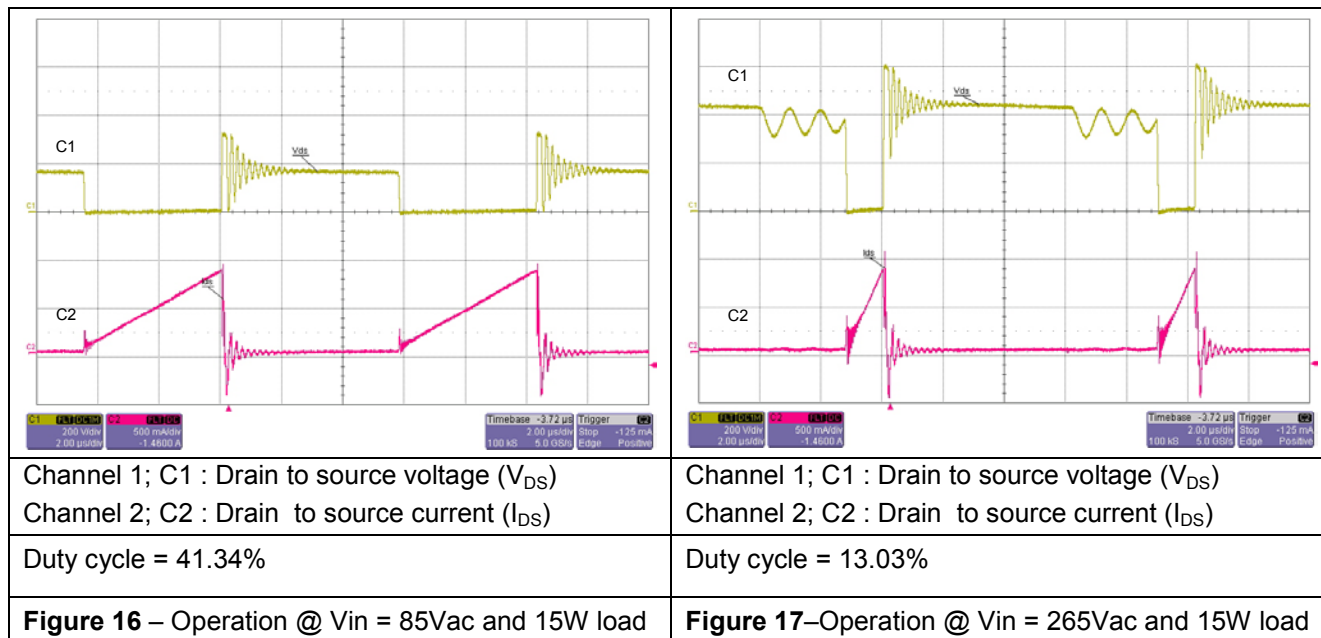
11 Waveforms and scope plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope

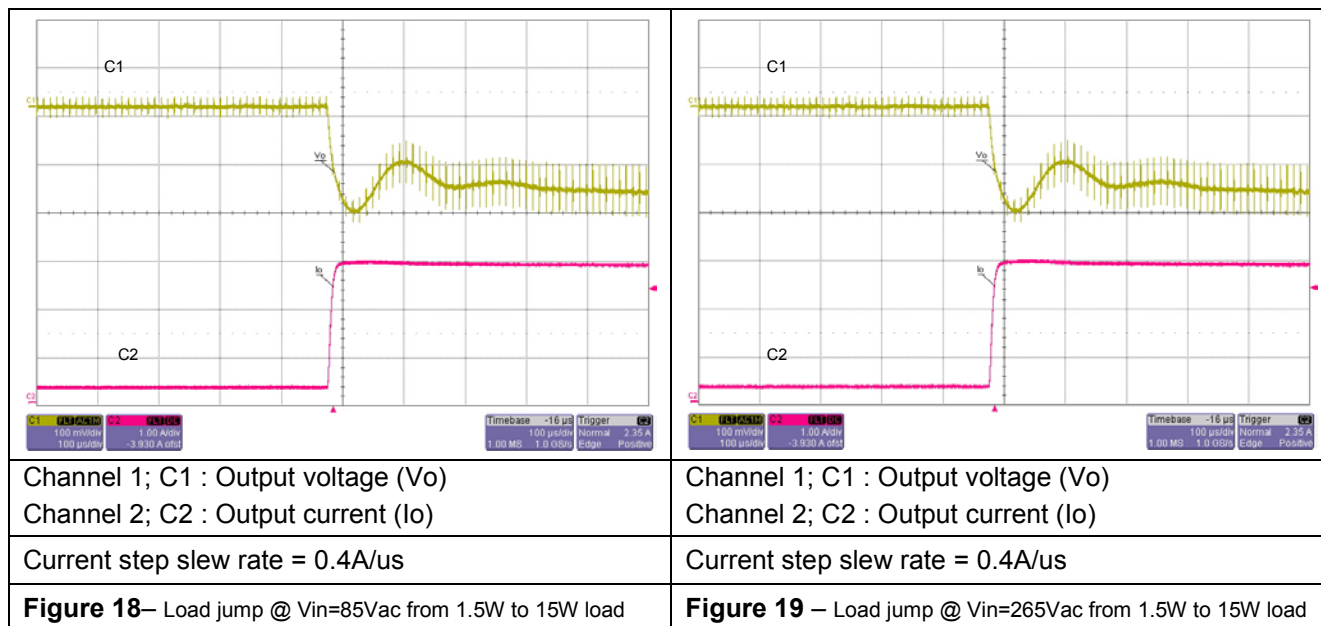
11.1 Startup @ low and high AC line input voltage and 15W load

Channel 1; C1 : Drain to source voltage (V_{DS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL voltage (V_{BL})	Channel 1; C1 : Drain to source voltage (V_{DS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL voltage (V_{BL})
Startup time = 0.52s	Startup time = 0.52s
Figure 16 – Startup @ $V_{in}=85V_{ac}$ and 15W load	Figure 17 – Startup @ $V_{in}=265V_{ac}$ and 15W load
Channel 1; C1 : Drain to source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Current sense voltage (V_{CS}) Channel Z4; Zoom of Channel 4	Channel 1; C1 : Drain to source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Current sense voltage (V_{CS}) Channel Z4; Zoom of Channel 4
Soft start time = 20ms	Soft start time = 20ms
Figure 18 – Soft Start @ $V_{in}=85V_{ac}$ and 15W load	Figure 19 – Soft Start @ $V_{in}=265V_{ac}$ and 15W load

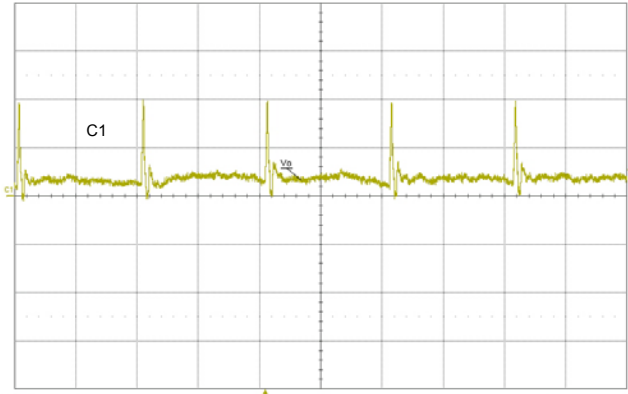
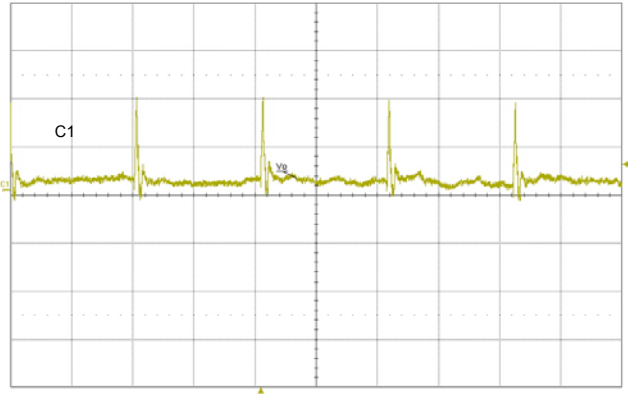
11.2 Drain to source voltage and current during 15W load operation



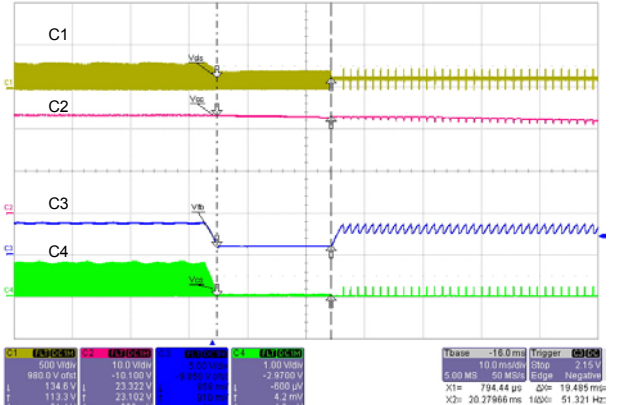
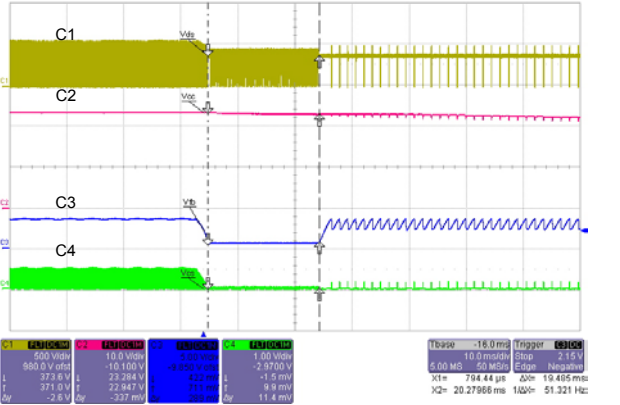
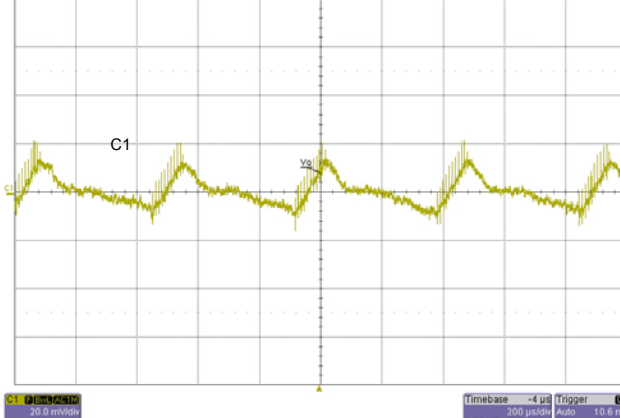
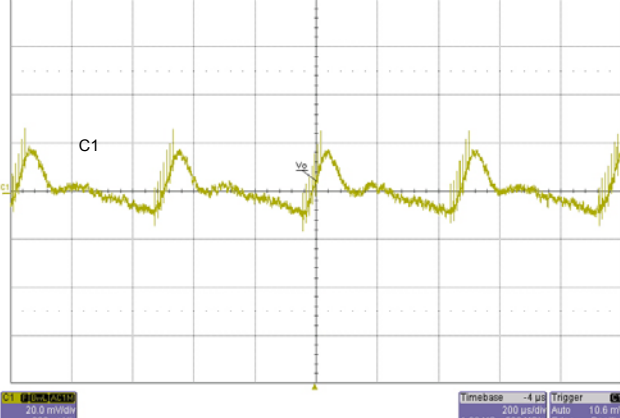
11.3 Load transient response (Load jump from 10% to 100%)



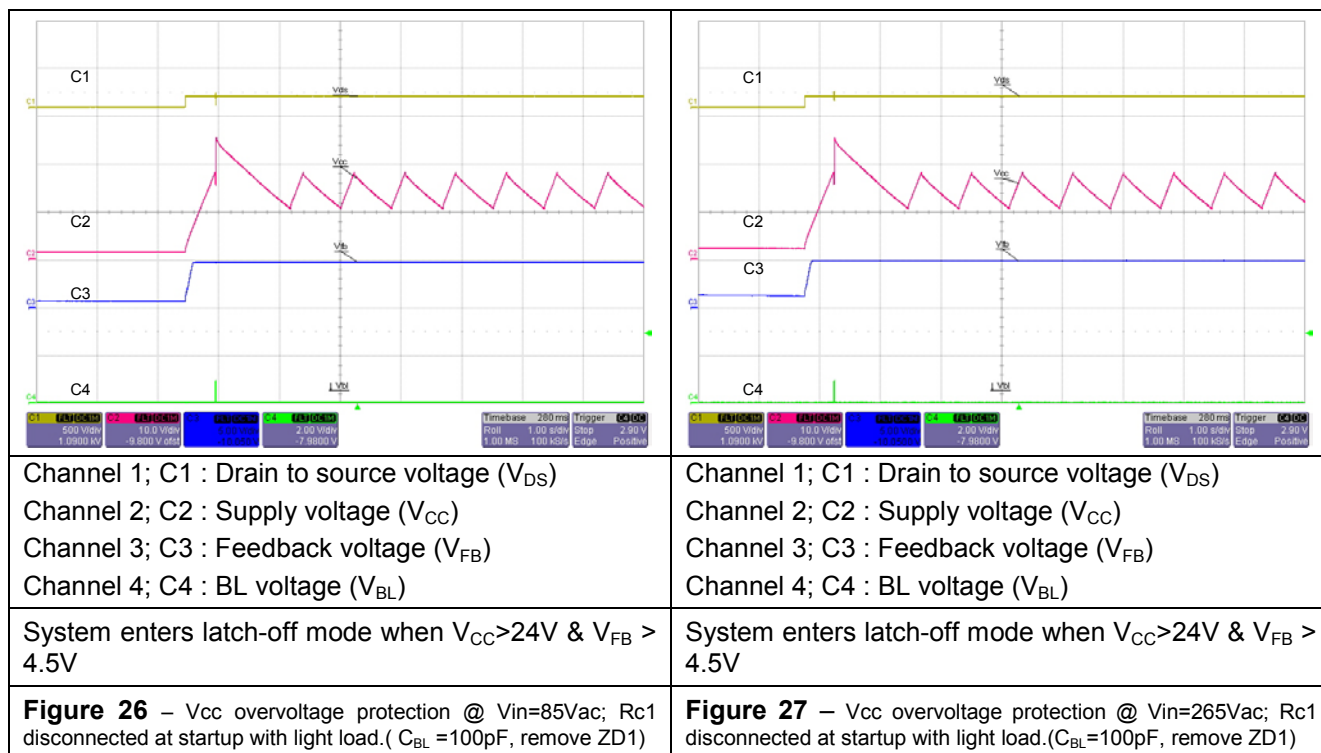
11.4 AC output ripple during 15W

	
Channel 1; C1 : Output ripple voltage	Channel 1; C1 : Output ripple voltage
Vo_ripple_pk_to_pk = 40mV Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 10uF(Electrolytic), 20MHz filter	Vo_ripple_pk_to_pk = 40mV Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 10uF(Electrolytic), 20MHz filter
Figure 20 – AC output ripple @ Vin=85Vac and 15W load	Figure 21 – AC output ripple @ Vin=265Vac and 15W load

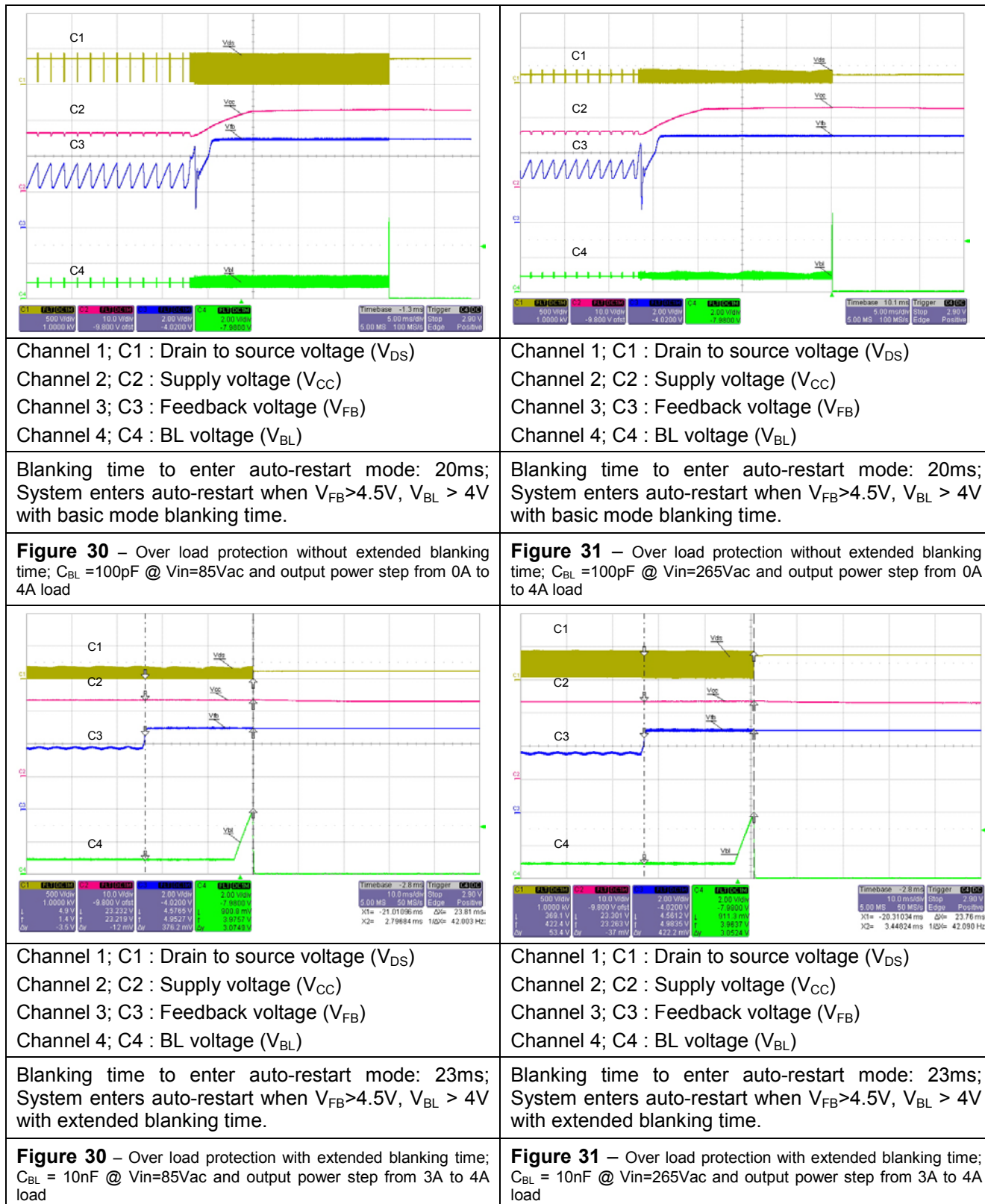
11.5 Active Burst Mode @ light load

	
Channel 1; C1 : Drain to source voltage (V_{DS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Current sense voltage (V_{CS})	Channel 1; C1 : Drain to source voltage (V_{DS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Current sense voltage (V_{CS})
Blanking time to enter burst mode : 19.4ms	Blanking time to enter burst mode : 19.4ms
Figure 22 – Active burst mode @ $V_{in}=85V_{ac}$ and step from 3A to 0.05A load	Figure 23 – Active burst mode @ $V_{in}=265V_{ac}$ and step from 3A to 0.05A load
	
Channel 1; C1 : Output ripple voltage	Channel 1; C1 : Output ripple voltage
$V_{o_ripple_pk_to_pk} = 40mV$ Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 10uF(Electrolytic), 20MHz filter	$V_{o_ripple_pk_to_pk} = 40mV$ Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 10uF(Electrolytic), 20MHz filter
Figure 24 – Output ripple at active burst mode @ $V_{in}=85V_{ac}$ and 0.25W load	Figure 25 – Output ripple at active burst mode @ $V_{in}=265V_{ac}$ and 0.25W load

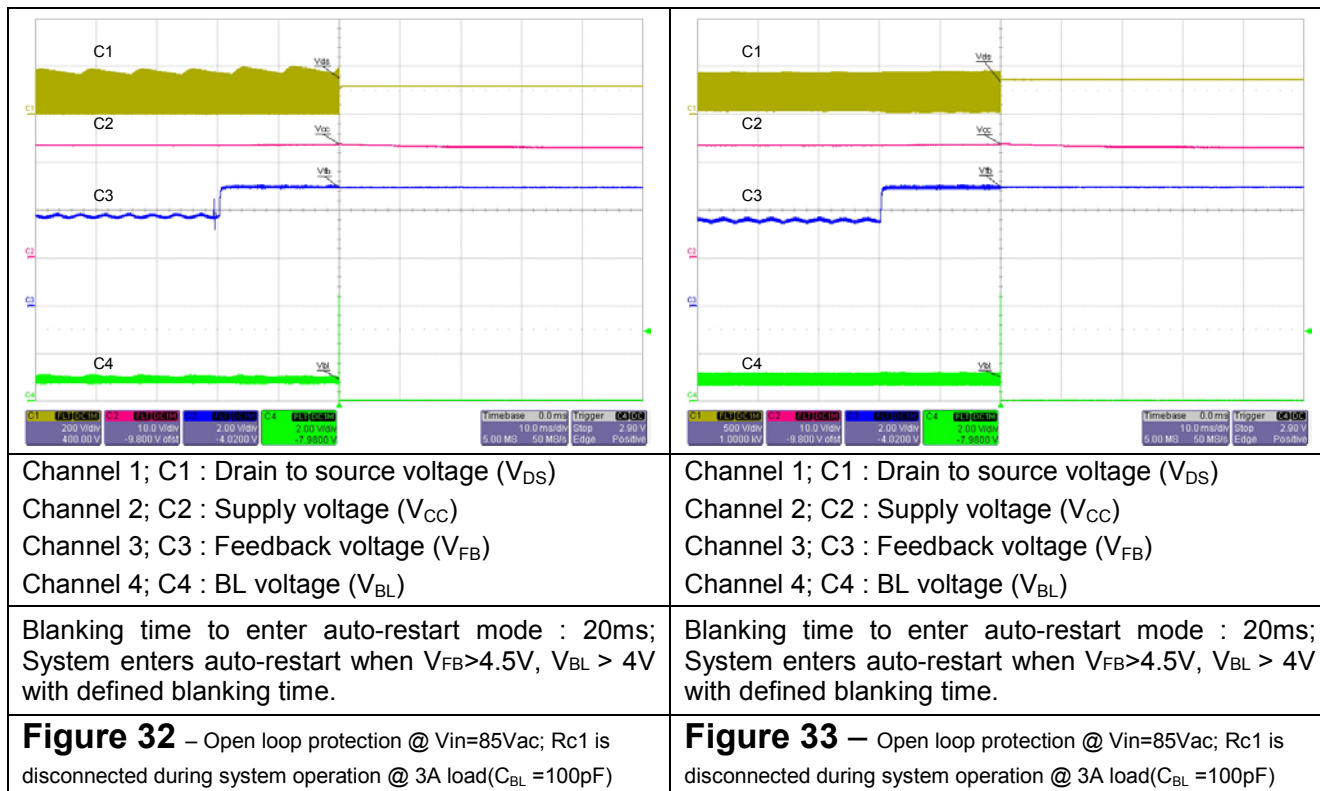
11.6 Vcc overvoltage protection (latch off mode)



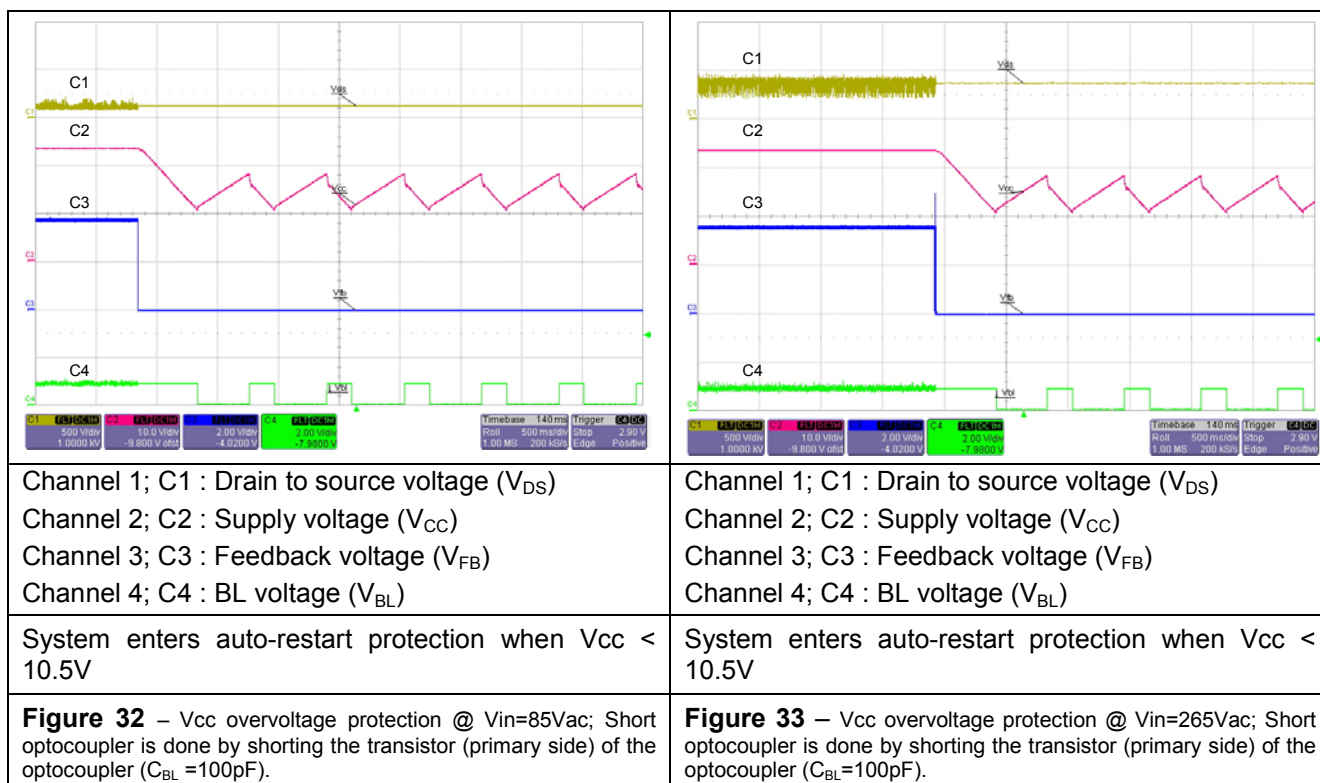
11.7 Overload protection without/with extended blanking time (auto restart mode)



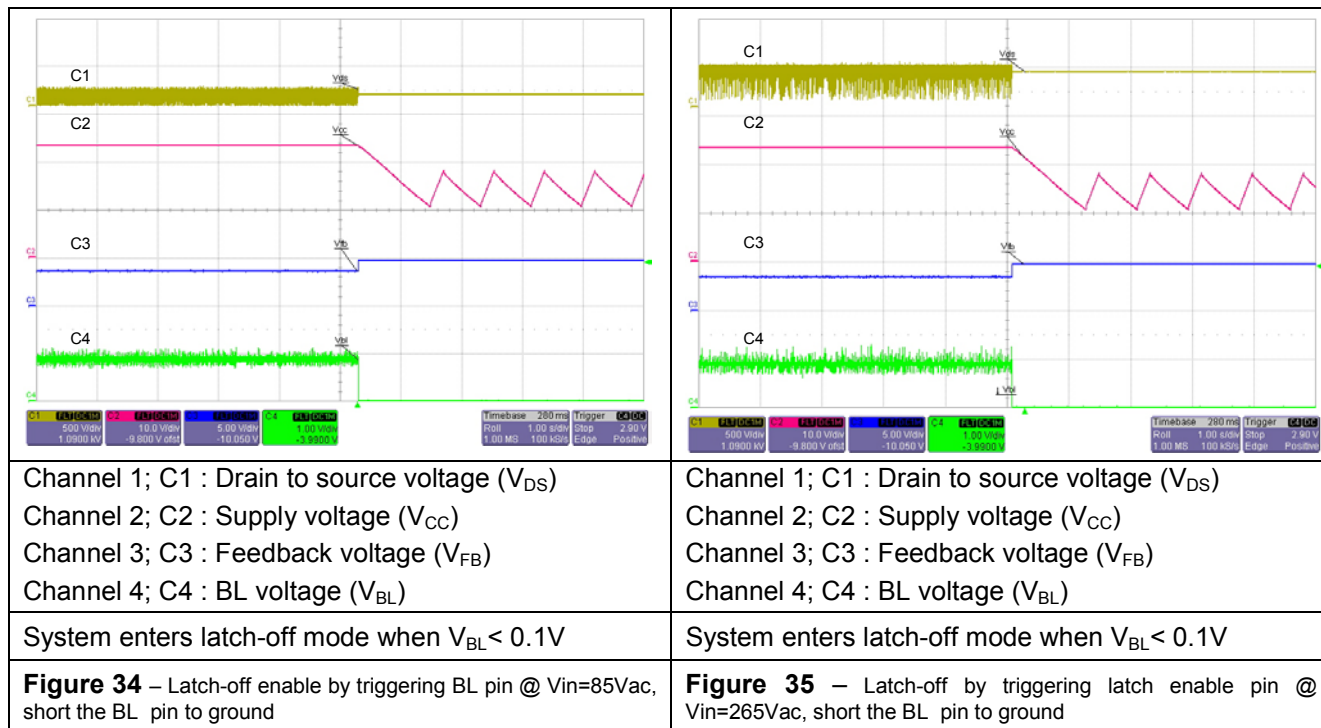
11.8 Open loop protection (auto restart mode)



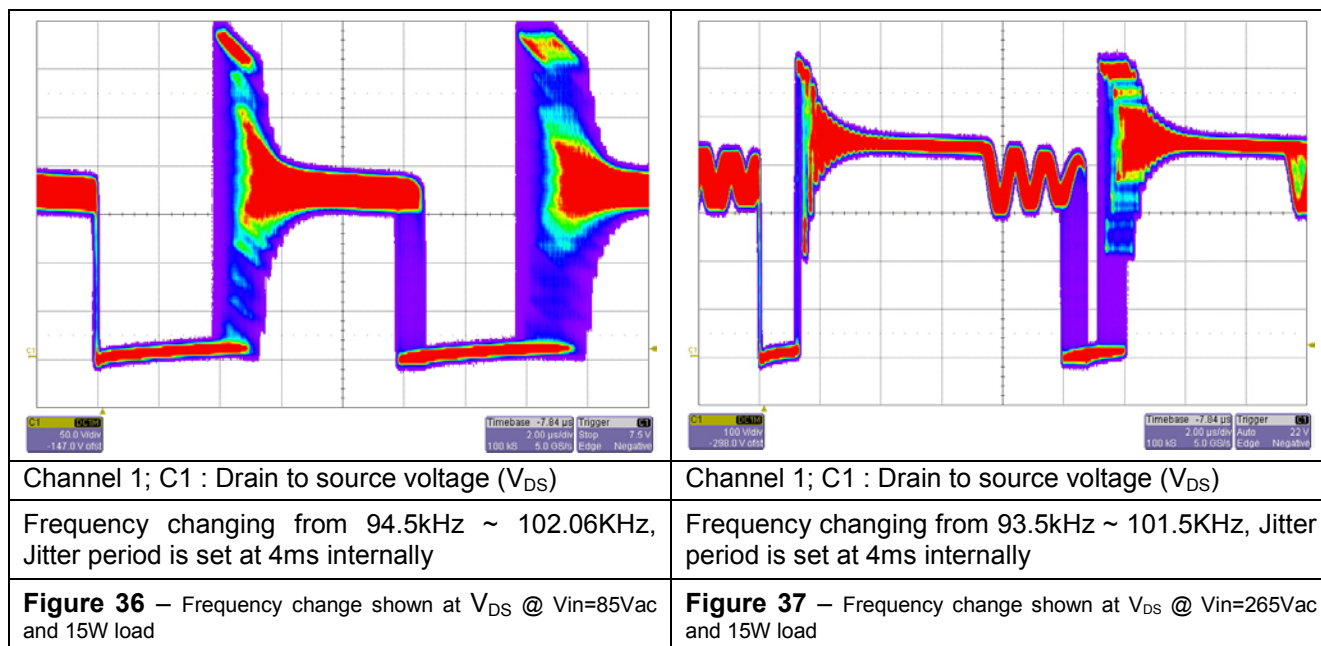
11.9 V_{CC} under voltage/Short optocoupler protection (auto restart mode)



11.10 External latch off enable



11.11 Frequency Jittering



12 Appendix

12.1 Slope compensation for CCM operation

This demo board is designed in Discontinuous Conduction Mode (DCM) operation. If the application is designed in Continuous Conduction Mode (CCM) operation where the maximum duty cycle exceeds the 50% threshold, it needs to add the slope compensation network. Otherwise, the circuitry will be unstable. In that case, three extra components (2 ceramic capacitors C17 & C18 and one resistor R19) are needed to add as shown in the circuit diagram below (red block).

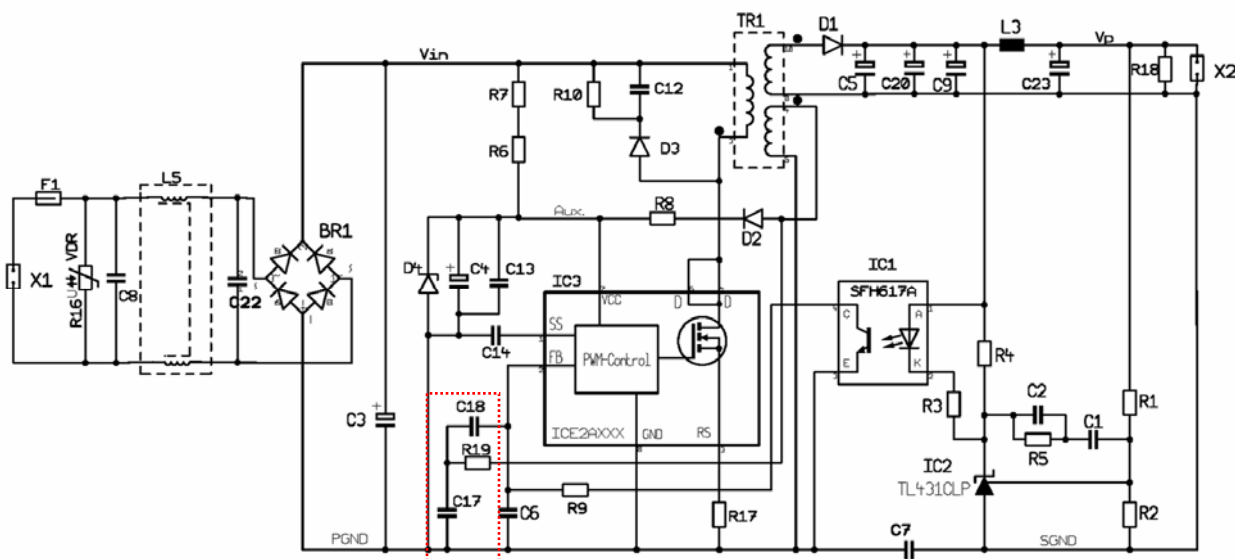


Figure 38 – Circuit Diagram Switch Mode Power Supply with Slope Compensation

More information regarding how to calculate the additional components, see in the application note AN_SMPS_ICE2xXXX – available on the internet: www.infineon.com/CoolSET CoolSET F2.

13 References

- [1] Infineon Technologies, Datasheet “CoolSET®-F3 ICE3A1065ELJ Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell (Latch and Frequency Jitter Mode)”
- [2] Kyaw Zin Min, Eric Kok Siu Kam, Infineon Technologies, Application Note “ICE3Axx65ELJ CoolSET® F3 latch & Jitter version Design Guide, AN-PS0030”
- [3] Harald Zoellinger, Rainer Kling, Infineon Technologies, Application Note “AN-SMPS-ICE2xXXX-1, CoolSET® ICE2xXXXX for Off-Line Switching Mode Power supply (SMPS)”