Protecting the TPS2392 and TPS2393 Insertion Inputs in Fused Applications

Andrew Ripanti *System Power*

ABSTRACT

The TPS2392 and TPS2393 −48-V hot swap power manager integrated circuits feature a useful insertion detection feature. This feature can sometimes be implemented in target application circuits directly as shown in the device data sheet. However, there are certain circuit configurations, when combined with specific failure mode sequences, that can lead to premature failure of the controller device. These application circuits and failure modes are identified in this document, along with a simple two-resistor solution to protect the system and on-board electronics even in these situations.

1 Introduction

The TPS2392 and TPS2393 are hot swap power manager (HSPM) devices designed to provide integrated hot swap capability in nominal −48-V supply systems. They feature inrush current slewing and peak limiting, overcurrent fault timing, programmable undervoltage (UV) and overvoltage (OV) thresholds and a powergood ($\overline{PG}$) output. In addition, two input pins are available for *insertion detection*; that is, verifying that a connector or plug-in module is fully seated prior to enabling power-up of the module electronics. It may be applicable in some applications to directly hard-wire these pins to the low-side rail potential. However due to the implementation scheme, fused applications require additional consideration and a slight modification of the circuit. This minor modification is necessary to protect the HSPM device under conditions in which the fuse itself is anticipated to blow.

2 Implementing Insertion Detection − The Basics

These devices monitor two logic inputs, INSA (pin 2) and INSB (pin 3) to determine if a card is fully seated in its chassis slot connector(s). The on-chip circuit looks for both inputs to be pulled below the nominal 1.4-V threshold. Once this condition is met, an internal timer is started to create a nominal 2.5-ms delay prior to enabling the output. If either logic low status is interrupted during the timeout period, for example, due to contact bounce, the timer is reset and then restarted when the required condition is met once again. Internal current sources at each pin pull the inputs to about 6 V during disconnected states, so no external drive circuitry is needed to generate the logic high condition.

A schematic of a TPS2392/2393-based hot swap circuit is shown in Figure 1. This may be recognized as the typical application schematic shown on page 1 of the device data sheet. Electrically, the two pins are pulled to the −VIN potential of the device (the device reference node) via hardwire connection to the −48-V rail through the backplane wiring. Therefore, these two connections, along with the −48-V power, must be made to meet the load enable requirements. This connection scheme, combined with the 2.5-ms delay, provides for a clean load power-up sequence commencing only after full board insertion and after any contact bounce.

From a mechanical standpoint, two design practices can be employed to maximize the performance of this function. One of these is the physical location of the INSA and INSB contacts. Besides showing the electrical connections, the Figure 1 drawing also attempts to illustrate, by way of the location of the INSx connector contacts, that ideally these contacts are selected at opposite ends of the card connector edge. Barring that , in systems where a designated power connector is pre-defined, and it does not occupy the entire card edge, then the INSx contacts should be located at opposite ends of the connector’s shell. If permitted, designers may also want to consider splitting these inputs between two PCB edge connectors in order to achieve the optimum physical placement.

The second effective practice is to use connector pin staging, wherein different signal groups are allocated among contact groupings having different pin lengths. Where this is available, tie the INSx inputs to the shortest pins in the connector.

Both of these practices improve the feature’s sensitivity to rocking of the plug-in card, during both insertion and extraction events, which serves to force full seating of the board before the electronics are powered.

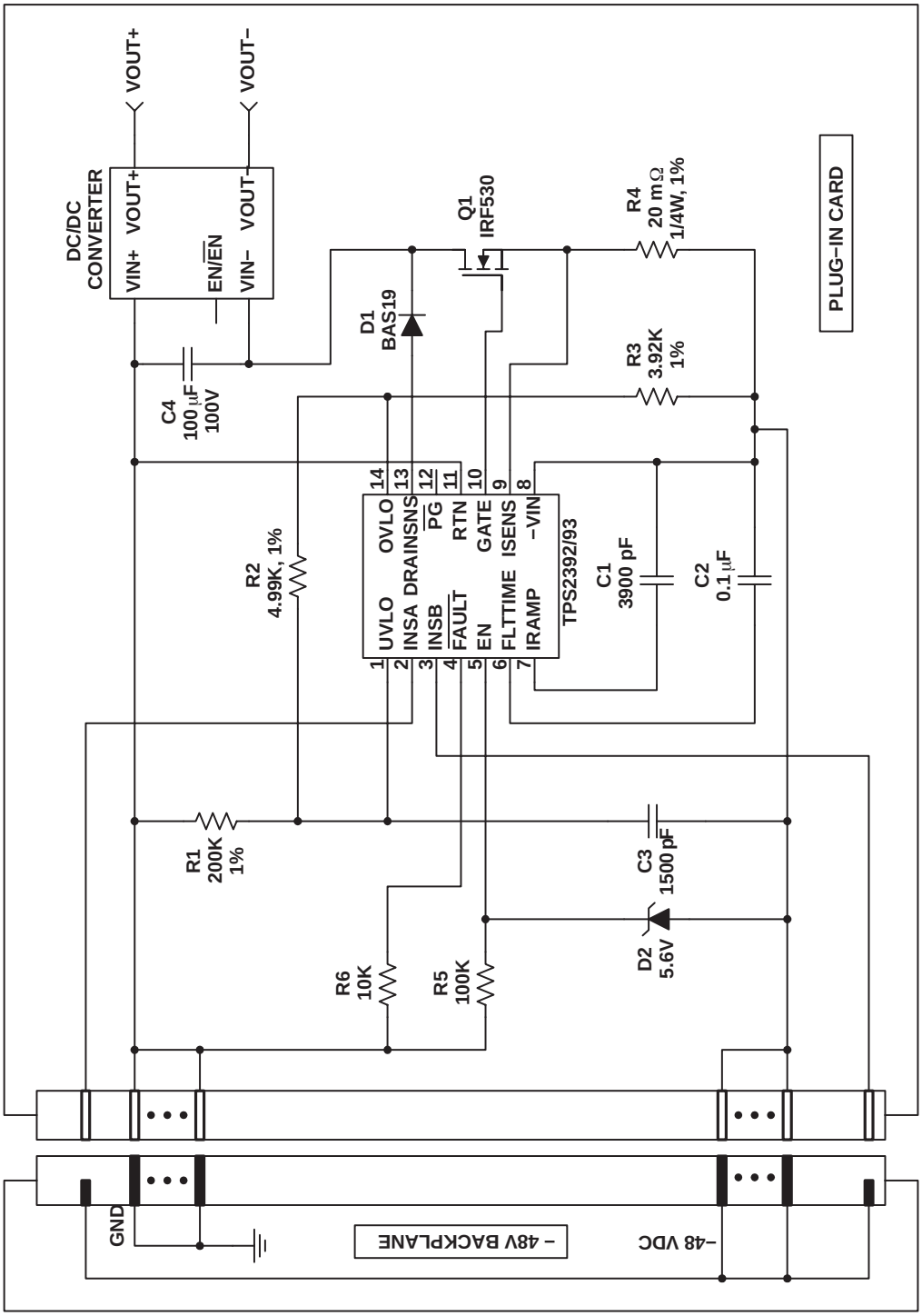

Figure 1. TPS2392/93 Basic Application Schematic

3 Fused Applications and Ensuring Robust Protection

The circuit of Figure 1 is a good hot swap design. It integrates many of the features needed for clean, low inrush insertion of unpowered modules, with controlled charging of the input bulk capacitance. Beyond the intervals of insertion events, it also continuously monitors the load against a user-programmable threshold, thereby integrating what is often referred to as an *electronic circuit breaker* function. Electronic circuit breakers, when compared to their mechanical, bi-metal counterparts, offer such improvements as a more predictable, reliable timing with reduced dependency on fault levels. This is because the fusing response is no longer a thermal function. In addition, they can be configured to be resettable by external control signals, or even provide an automatic fault retry mode. All combined, these features reduce service calls and downtime compared to the one-shot fuse.

However, the reality of safety and redundancy requirements is that the majority of applications of hot swap will also employ some sort of mechanical fusing. Fusing may be mandated by applicable equipment design standards, or simply included as good design practice. In this configuration, mechanical fusing serves as a back-up action to the electronic circuit breaker operation. The resettable silicon fuse of the hot swap prevents the one-shot from blowing in nearly all instances of excessive current draw. This includes initial, high-current charging of the module input bulk capacitance, load surges and faults, and hard shorts as may be encountered during equipment servicing. The fuse only actuates then after a failure of the hot swap circuit, combined with a subsequent load fault.

When a fuse is inserted in-line with the low-side power rail, as it typically is, the addition of two low-power resistors is needed to properly protect the TPS2392 or TPS2393 in the event of a fuse blow.

Given the back-up nature of the fuse action described above, a fuse blowing incident is only anticipated after a sequence of faults. First, the hot swap circuit must lose its control over the maximum current sourced to the load. This can happen if the external N-channel MOSFET (Q1 in the schematic) fails short. In this circumstance, the gate control of the HSPM can no longer interrupt the supply path by opening the FET switch. The same condition exists in the rare instances where the power manager itself fails, and either no longer detects overcurrent conditions, or can no longer discharge the pass FET gate. If these conditions exist on a given board, and the fuse’s rating is subsequently exceeded, the fuse blows according to its own characteristic.

For the circuit of Figure 1, the above scenario may result in permanent damage to the TPS2392/93, even if that device hadn't already failed and contributed to the catastrophic sequence. The reason for the damage is easily understood, and a simple modification protects against it. As with the pins of most of today's semiconductor devices, the INSA and INSB inputs of these devices incorporate some form of ESD protection provided on-chip, immediately where the external signals are applied to the die. These protection devices can be characterized as input diodes, and under normal operating conditions, are off and not conducting. They are only intended to conduct during an ESD strike applied to an input pin. However, in the above scenario, as the resistance of the mechanical fuse increases due to its own positive temperature coefficient, it develops a voltage drop which raises the potential of the −VIN and ISENS pins, relative to the fixed potential of the backplane −48 V. This backplane potential is also where the insertion inputs are tied. When this potential across the device exceeds the forward voltage of the diode-like protection devices, they turn on and conduct in the forward direction. This conduction causes excessive current flow in the device substrate, which can lead to latch-up, and excessive dissipation in the die, causing permanent damage. Once the fuse blows, this path is the next lowest impedance return path to the supply, and the device fails due to excessive heating.

The solution to this is shown in the Figure 2 schematic. Two 56.2-kΩ, ¼-W resistors are placed in series with the insertion detection input pins, one in each line as shown. These resistors work by limiting the current that can be conducted through the protection devices, should they become forward-biased. Under normal operation of the board, they cause a quiescent pin voltage of about 560 mV at each input. Though this reduces somewhat the noise margin over the direct-connect method, there is still sufficient margin, even under worst-case parametric conditions, for the circuit to function. The resistor value is perhaps non-critical; however, the 56.2-kΩ value recommended provides the anticipated best balance between the current-limiting needed and the logic-level margin.

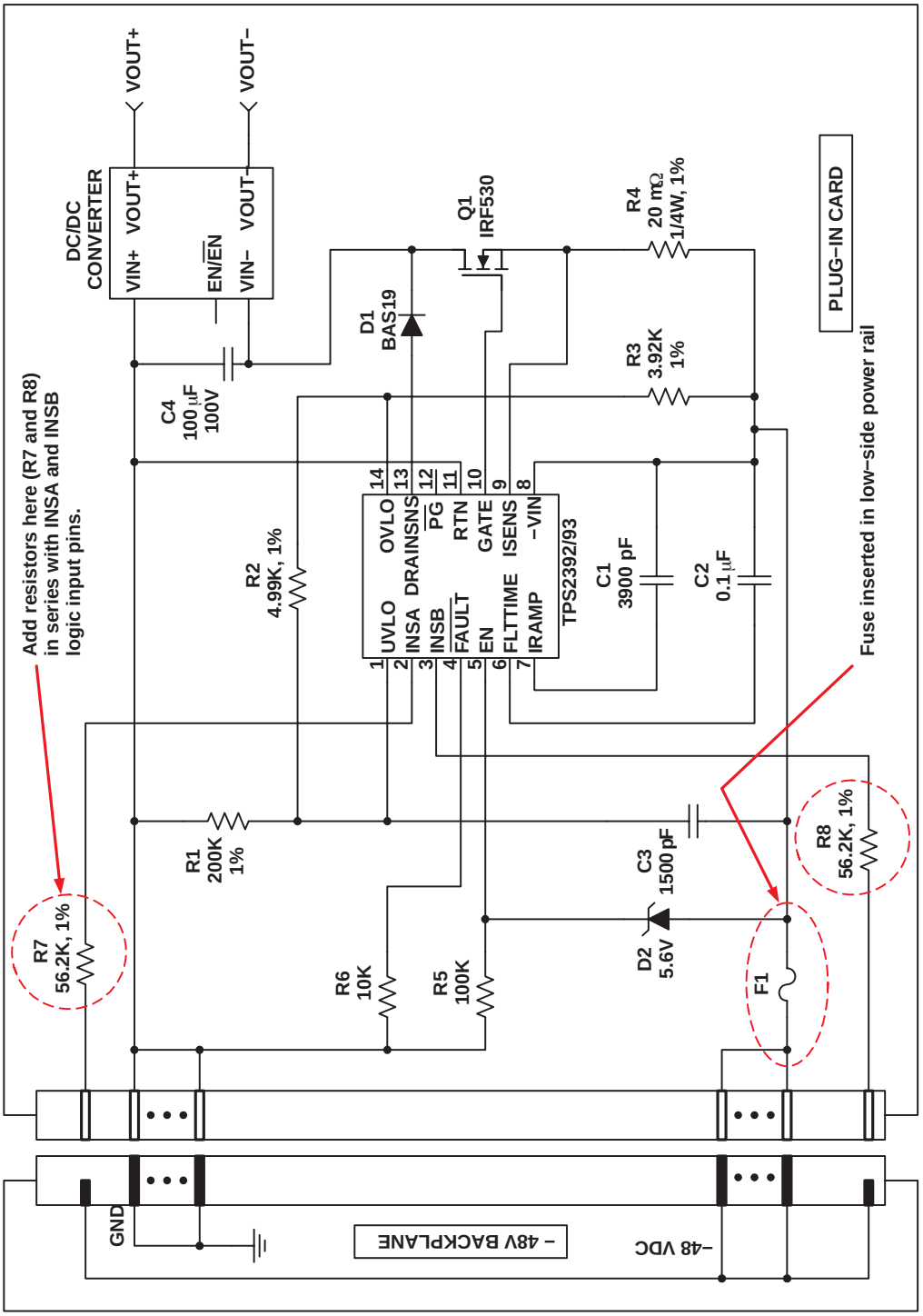

Figure 2. TPS2392/93 Circuit Connections with Back−Up Fusing Employed

Figure 3 is an oscilloscope plot demonstrating the function of the added current-limiting resistors. In this example, the controller device operation is thwarted by shunting the load high-side (the supply return node) to the pass FET source. This generates an excessive load, while at the same time defeating the hot swap controller's circuit breaker action. The fuse in this example was a 2-A rated, ¼-inch glass cartridge device (3AG type). For this scope plot, the scope reference was connected to the backplane −48-V node.

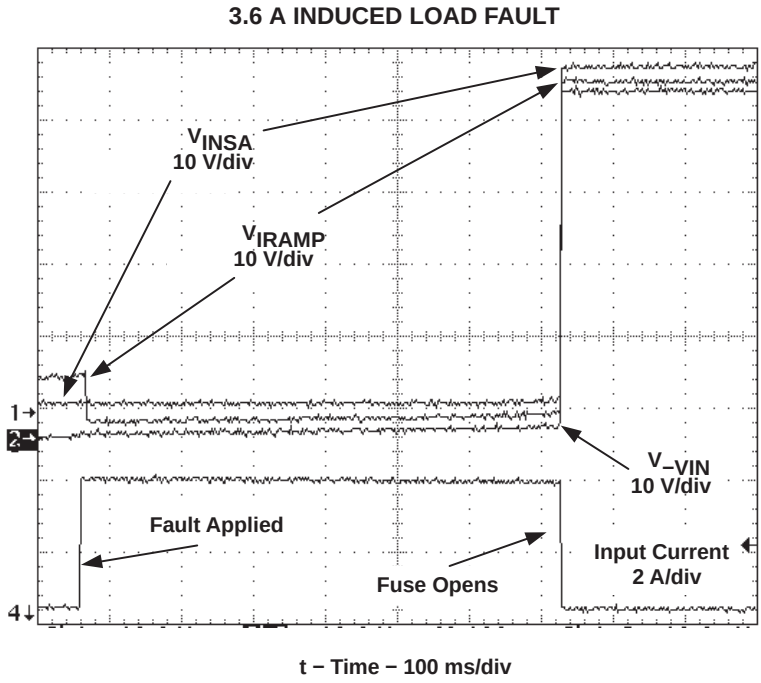

Figure 3.

The load fault was induced by suddenly applying a 3.6-A load across output and pass FET as described above. The application of the fault can be seen at the left side of the plot, at the load current step. The intended HSPM response is confirmed a few milliseconds later when the IRAMP pin voltage is pulled low as part of the device's fault shutdown operation. However, the fault condition is yet uninterrupted. When the fuse eventually blows about 660 ms later, the reference connection at −VIN is lost, and the three nodes displayed jump to the return potential. At this point, the circuit is effectively *floating* on the new insertion detection resistors. Supply voltage appears across the external resistors, but due to their value, only milliamp-level current can be conducted through the device. After this and many similar instances of fuse blowing, the controller device was still fully functional.

4 Summary

As seen here, applications may be able to implement the TPS2392/93 insertion detection directly as shown in the data sheet. However, when used in conjunction with a back-up mechanical fuse, the hot swap circuit should be modified as shown in Figure 2. The addition of the two small, 56.2-kΩ resistors improves the survivability of the controller device in catastrophic faults under which the fuse blows. This reduces repair times and system downtime, as the repair may again be reduced (depending on the original fault condition) to simply replacing the fuse.

5 References

1. *TPS2392 and TPS2393 Full-Featured −48-V Hot Swap Power Manager*, Data Sheet; Texas Instruments; Literature No. SLUS536; November 2002.

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