

PR213  
Spartan™-3 Design 1  
TPS64203 Switching DC/DC Controller-Based Power Management Solution Providing  
up to 3 A from  $V_{IN} = 5.0\text{ V}$  or  $3.3\text{ V}$

FEATURES:

- Tiny SOT-23 switching DC/DC controller, U2, delivers up to 3 A at low cost.
- Easily customizable design allows for maximum cost control by:
  - o Sizing Q3 for the amount of current up to 3 A to meet the application's  $I_{CCINT}$  requirement,
  - o Omitting current sense resistor R4 and connecting ISNS to the drain of Q3,
  - o Selecting the linear regulator from the TPS79xxx family to meet the application's  $I_{CCO}$  requirement.
- In-rush current (for charging decoupling capacitors and FPGA start-up) that places a demand on the input power supply is minimized by the use of the:
  - o External supervisory (SVS) IC, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
  - o Integrated soft-start of U2
  - o Soft-start circuit consisting of the external PMOS transistor Q4 and supporting passive components to provide 10 ms rise time for  $V_{CCO}$
  - o Sequential sequencing of  $V_{CCINT}$ ,  $V_{CCAUX}$  then  $V_{CCO}$ 
    - the discrete SVS circuit formed by bipolar transistors Q1 and Q2 and supporting passives enables the  $V_{CCAUX}$  regulator, U3
    - $V_{CCAUX}$  enables the  $V_{CCO}$  regulator, U4
- The design meets Xilinx's  $V_{CCINT}$  and  $V_{CCO}$  start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at <http://www.ti.com/xilinuxfpga> for more information and other reference designs.
- Link to datasheets at <http://focus.ti.com/lit/ds/symlink/tps64203.pdf>, <http://focus.ti.com/lit/ds/symlink/tps78601.pdf>, <http://focus.ti.com/lit/ds/symlink/tps79401.pdf>, and <http://focus.ti.com/lit/ds/symlink/tlc7705.pdf>.
- Link to application note SLVA156 <http://focus.ti.com/lit/an/slva156/slva156.pdf> for more details on the soft-start circuit.
- Link to application note SLVA118 <http://focus.ti.com/lit/an/slva118/slva118.pdf> to explore the thermal considerations when using linear regulators.
- Link to application note SLVA160 <http://focus.ti.com/lit/an/slva160/slva160.pdf> for guidance on selecting a different option from the TPS642xx family.

- Link to application note SLVA159  
<http://focus.ti.com/lit/an/slva159a/slva159a.pdf> when using 3.3-V JTAG ports.

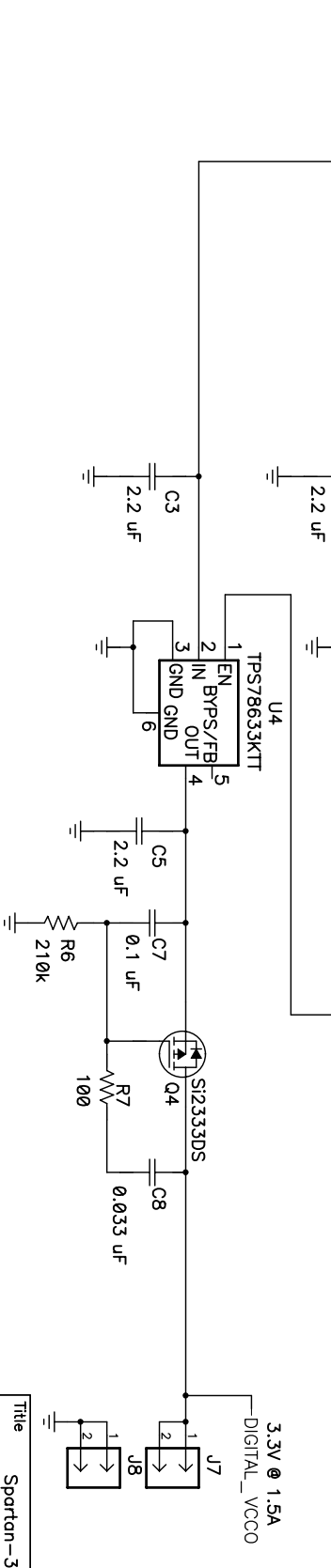
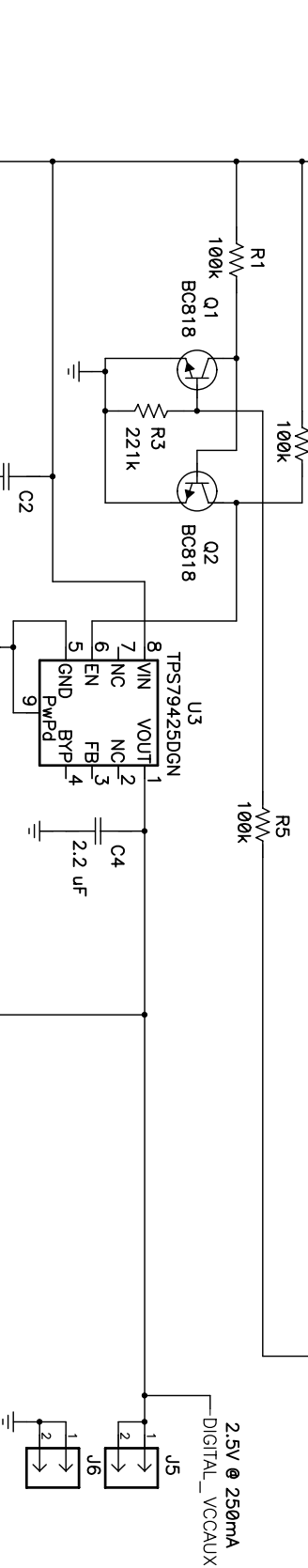
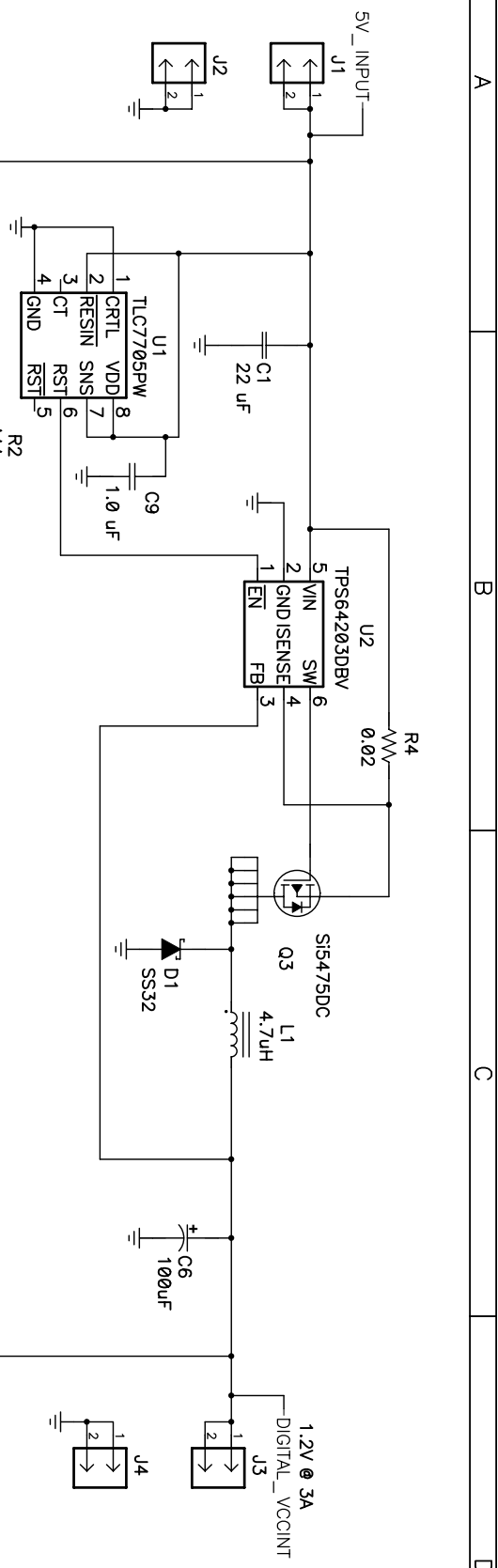
#### IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads all at once.
- **V<sub>CCO</sub> minimum ramp time:** Met by Q4 soft-start circuit
- **Power Dissipation/Thermal Issues:** Refer to the application section of the linear regulator datasheet for maximum power dissipation at different ambient conditions as well as guidance on sizing the ground plane area underneath the package for heatsinking.
- **Designing with the TPS64203:**
  - o The TPS64203 controller has limited current to drive the gate of the PMOS transistor, Q3. To ensure proper operation of the controller, a PMOS transistor with a maximum total gate charge,  $Q_g$ , of less than 50 nC is required.
  - o Omitting current sense resistor R4 and connecting ISNS to the drain of Q3, thereby using the  $R_{DSon}$  of Q3 as the current sense, results in an effective, but slightly less accurate, current limit function.
- **Soft Start Circuitry:**
  - o PMOS transistor Q4 should be selected so that its threshold voltage,  $V_{TH}$ , is at least 0.9 V below the  $V_{CCO}$  voltage or lower (e.g.,  $V_{TH} \leq 3.3 \text{ V} - 0.9 \text{ V} = 2.4 \text{ V}$ ). In addition, the transistor's  $R_{DSon}$  should be low enough when driven by the output of the linear regulator so that the voltage drop across the transistor at maximum current (e.g.,  $I_{CCINTmax} * R_{DSon}$ ) does not cause  $V_{CCO}$  to fall below its -5% tolerance.
  - o The drain of Q4 needs at least 10 uF of total capacitance in order for the soft-start circuit to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for the  $V_{CCO}$  rail of the FPGA will most likely meet this requirement.
- **Layout:** The 1.0 uF capacitor, C7, should be placed as close as possible between VDD and GND of the TLC77xx SVS IC.
- **Modifications:**
  - o CT of TLC7705 is not connected, but can be used with a capacitor to add a delay between the 5 V rail coming up and  $RST = /EN$  of TPS64203.
  - o Adapt for 3.3V supply by:
    - Omitting U4 circuit,
    - Replacing TLC7705 with TLC7733.
  - o For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).
- **3.3V Configuration**

- The Spartan-3 FPGA configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configurations and JTAG input pins, through the FPGA, to the  $V_{CCAUX}$  power rail. Therefore, please refer to application note SLVA159 <http://focus.ti.com/lit/an/slva159a/slva159a.pdf> for implementation guidance.

## QUESTIONS?

- Send an email to <mailto:fpgasupport@list.ti.com>



Title			
Spartan-3 Controller			
Size	Number	Rev	
B	PR213		
Date	4/22/04	Drawn by	
Filename	pr213.sch	Sheet	of

Filename: PR213_bom.xls					
Date: 04/22/2004					
		<b>PR213 BOM</b>			
COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, Ceramic, 22-uF, 10-V, X5R, 10%	1210	muRata	GRM32ER61A226KA65
4	C2, C3, C4, C5	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
1	C6	Capacitor, Tantalum, 100-uF, 10-V, 95-milliohm, 20%	7343 (D)	Vishay	594D107X0010C2T
1	C7	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E104KA01
1	C8	Capacitor, Ceramic, 0.033-uF, 16-V, X7R, 10%	603	muRata	GRM188R71C333KA01
1	C9	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
1	D1	Diode, Schottky Barrier Rectifier, 3-A, 20-V	SMC	Vishay	SS32
1	L1	Inductor, SMT, 4.7-uH, 4-A, 470-milliohm	0.543 x 0.512	Vishay	IHSM-4825-RE-4R7L
2	Q1, Q2	Bipolar, NPN, 30-V, 800-mA, 310-mW	SOT23	Vishay	BC818
1	Q3	MOSFET, P-ch, 20V,4.8-A, 76-milliohm	1206-8	Vishay	Si5475DC
1	Q4	MOSFET, P-ch, -12 V, 4 A, 51 milliohm	SOT23	Vishay	Si2333DS
3	R1, R2, R5	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	603	Std	Std
1	R3	Resistor, Chip, 221k-Ohms, 1/16-W, 1%	603	Std	Std
1	R4	Resistor, Chip, 0.02-Ohms, 1/4-W, 1%	1210	Std	Std
1	R6	Resistor, Chip, 75k-Ohms, 1/16-W, 1%	603	Std	Std
1	R7	Resistor, Chip, 100-Ohms, 1/16-W, 1%	603	Std	Std
1	U1	IC, Voltage Supervisor, Micropower	35630	TI	TLC7705PW
1	U2	IC, Step-Down Controller	SOT23-6	TI	TPS64203DBV
1	U3	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, 2.5V	MSOP 8	TI	TPS79425DGN
1	U4	IC, Ultra Low-Noise, High PSRR, Fast RF 1.5A LDO Linear Regulator	DDPAK-5	TI	TPS78633KTT

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