PR214

Spartan™-3 Design 2

Dual Linear Regulator Power Management Solution Providing up to 850 mA from V_{IN} = 3.3 V

FEATURES:

- Dual channel low-dropout (LDO) linear regulator in thermally enhanced PowerPAD^{TM} package saves cost and space.
- Linear regulators start-up fast, allowing large in-rush currents for charging decoupling capacitors and FPGA start-up. The current draw on the input power supply is minimized by the use of the optional:
    - External SVS, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
    - Soft-start circuit consisting of the external NMOS transistor Q1 and supporting passive components to provide 10 ms rise time for V_{CCINT}
        - Soft-start circuit (Q1) forces sequencing of V_{CCAUX}, then $V_{CCINT,}$ with EN1 and EN2 tied together.
- The design meets Xilinx's V_{CCINT} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/TPS70402.pdf and http://focus.ti.com/lit/ds/symlink/tlc7733.pdf.
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations when using linear regulators.
- Link to application note SLVA156 http://focus.ti.com/lit/an/slva156/slva156.pdf for more details on the soft-start circuit.
- Link to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf when using 3.3-V JTAG ports.

IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads.
- **Power Dissipation/Thermal Issues:** The dual regulator, U2, is limited to 2W @ $T_A = 55^o$ C and no airflow, due to power dissipation limitation of the PowerPAD^{TM} package.

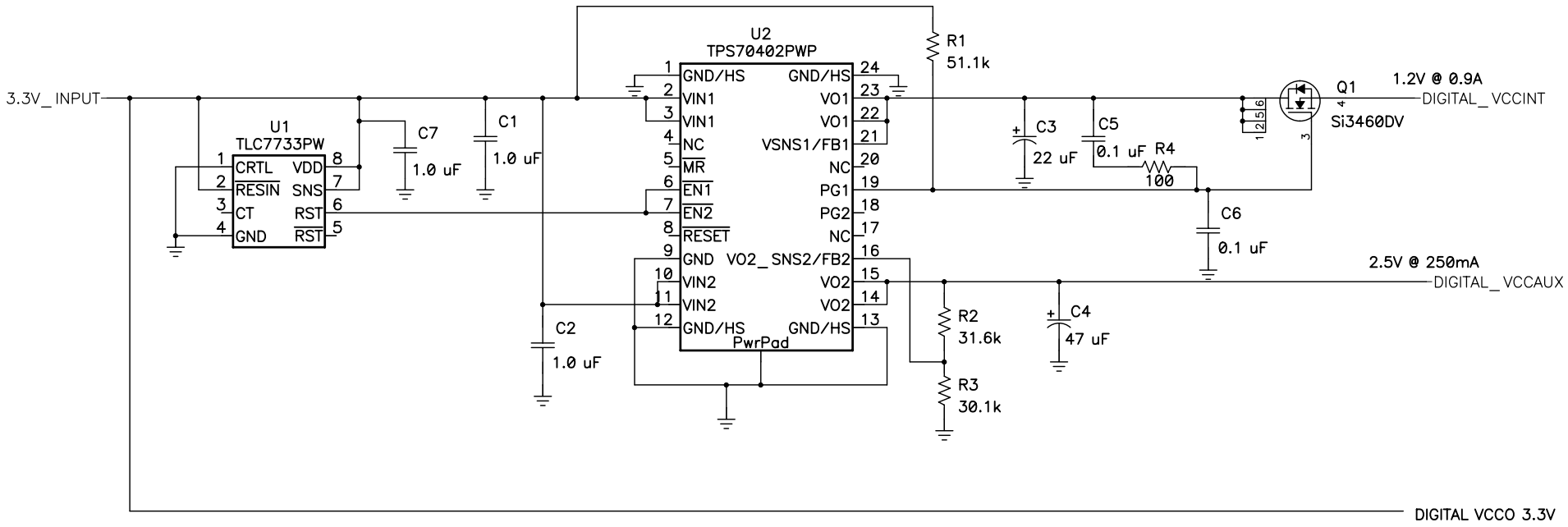
- Refer to the application section of the datasheet for maximum power dissipation at different ambient conditions and guidance on sizing the ground plane area underneath the package for heatsinking.
- The following equation can be used to solve for the maximum current on one rail if the other rail current is known:
  $P_{Dmax} = (V_{IN} - V_{CCINT}) * I_{CCINTmax} + (V_{IN} - V_{CCAUX}) * I_{CCAUXmax}$

  As an example, with V_{IN} = 3.3 V, V_{CCINT} = 1.2V, V_{CCAUX} = 2.5 V, P_{Dmax} = 2 W and assuming that the $I_{CCAUXmax}$ = 250 mA:
  - I_{CCINT}max = $[P_{Dmax} - (V_{IN} - V_{CCAUX}) * I_{CCAUXmax}] / (V_{IN} - V_{CCINT})$
  - $I_{CCINTmax}$ = 857 mA

- **Soft Start Circuitry:**
  - NMOS transistor Q1 should be selected so that its threshold voltage, V_{TH}, is at least 0.9 V below V_{IN} or lower (e.g., $V_{TH} \leq 3.3\ V - 0.9\ V = 2.4\ V$). In addition, the transistor's R_{DSon} of Q1 should be low enough, when driven by V_{IN}, that the voltage drop across the transistor at maximum current (e.g., $I_{CCINTmax} * R_{DSon}$) does not cause V_{CCINT} to fall below its -5% tolerance.
  - The source of Q1 needs at least 10 uF of total capacitance in order for the soft-start circuit to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for the V_{CCINT} rail of the FPGA will most likely meet this requirement.
- **Layout:** The 1.0 uF capacitor, C7, should be placed as close as possible between VDD and GND of the TLC7733 SVS IC.
- **Modifications:**
  - CT of TLC7733 is not connected, but can be used with a capacitor to add a delay between the 5V rail coming up and RST = /EN1=/EN2 of TPS70402.
  - Select the appropriate TLC77xx option to monitor the input supply voltage.
  - For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).
  - Note that with higher voltage input supplies, such as 5V, power dissipation in the linear regulator is of greater concern (see previously presented power dissipation calculations).
- **3.3V Configuration**
  - The Spartan-3 FPGA configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configurations and JTAG input pins, through the FPGA, to the V_{CCAUX} power rail. Therefore, please refer to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf for implementation guidance.

QUESTIONS?

- Send an email to mailto:**fpgasupport@list.ti.com**



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PR214 BOM

COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
3	C1, C2, C7	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
1	C3	Capacitor, Tantalum, 22-uF, 6.3-V	3528 (B)	Vishay	594D226X06R3B2T
1	C4	Capacitor, Tantalum, 47-uF, 10-V, 20%	3528 (B)	Vishay	594D476X010B2T
2	C5, C6	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E104KA01
1	Q1	MOSFET, N-ch, 60-V,3.2-A, 100-milliOhms	TSOP-6	Vishay	Si3460DV
1	R1	Resistor, Chip, 51.1k-Ohms, 1/16-W, 1%	603	Std	Std
1	R2	Resistor, Chip, 31.6k-Ohms, 1/16-W, 1%	603	Std	Std
1	R3	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	603	Std	Std
1	R4	Resistor, Chip, 100-Ohms, 1/16-W, 1%	603	Std	Std
1	U1	IC, Voltage Supervisor, Micropower	35630	TI	TLC7733PW
1	U2	IC, LDO Regulator, Adj-V, Dual	PWP24	TI	TPS70402PWP

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