MIC5165YMM Evaluation Board

Dual Regulator Controller for DDR3, GDDR3/4/5 Memory Termination

Power Good Signal

General Description

The MIC5165 is a dual regulator controller for high-speed bus termination that offers a simple, low-cost JEDEC-compliant solution for terminating high-speed, low-voltage digital buses (i.e., DDR, DDR2, DDR3, SCSI, GTL, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc) and features a Power Good output (PG) and an Enable input (EN).

The MIC5165 controls two external N-Channel MOSFETs to form a current source/sink circuit that responds adaptively for active high-speed bus termination. The output voltage V_{TT} is programmed by external voltage V_{DDQ}, where V_{TT} = ½ V_{DDQ}.

The evaluation board includes a MIC5165YMM, and a MIC22950YML buck regulator that provides the 1.2V high current termination source.

Data sheets and support documentation are found on the Micrel web site: www.micrel.com.

Requirements

The MIC5165YMM EV requires two input supply voltages and a test load. The input voltages are V_{IN} of 3.0V to 5.5V (typically 5V, 5A minimum) to power the ICs and the termination bus, and a V_{DDQ} supply of 0.75V to 6.0V from which the V_{TT} regulation reference is derived. The load can be active (electronic load), or passive (resistor).

Precautions

There is no reverse input protection on this board, when connecting supplies and signals ensure that correct polarities are observed.

Getting Started

1. **V_{IN} Supply**
   With the Enable input (EN) connected to GND, connect the V_{IN} supply (3.0V to 5.5V) across the V_{IN} and GND terminals; typically, V_{IN} = 5.0V. Monitor V_{IN} at the test board input terminals with a voltmeter. V_{IN} powers both the MIC22950 and the MIC5165. The MIC22950 steps down V_{IN} to generate the 1.2V that the MIC5165 further regulates to V_{TT}.

2. **V_{DDQ} Supply**
   Connect the V_{DDQ} supply (0.75V to 6.0V) across the V_{DDQ} and GND terminals. Typically, V_{DDQ} = 1.2V. The MIC5165 regulates V_{TT} to ½V_{DDQ}.

3. **Output Load**
   Connect the load across the V_{TT} and GND terminals. Monitor V_{TT} with a voltmeter at the V_{TT} and GND terminals.

4. **Enable the Circuit**
   Release the enable input (EN is pulled up to V_{IN} through a 1kΩ resistor). When the active high enable input EN is above 1.2V the output voltage V_{TT} regulates to ½V_{DDQ}. When EN is below 0.3V the MIC5165 is disabled and draws only microamps.

Ordering Information

Part Number	Description
MIC5165YMM EVB	Evaluation Board for the MIC5165YMM

Evaluation Board Features

MIC5165 Control and Monitor Signals

Note: See the MIC5165YMM datasheet for detailed explanations of these functions.

Enable (EN)

The MIC5165 features an active high enable input, EN. Enable is pulled up to V_{IN} through a 1kΩ resistor. With EN low, supply currents are reduced to microamperes. The enable input has thresholds compatible with TTL/CMOS for simple logic interfacing, with thresholds of 0.3V and 1.2V.

Power Good (PG)

MIC5165 features a Power Good (PG) output. PG is an open drain, active high signal, and is connected to V_{IN} through a 10kΩ resistor. PG pulls low if V_{TT} is more than 10% above or below ½V_{DDQ}.

MIC22950 Control and Monitor Signals

Note: See the MIC22950YML datasheet for detailed explanations of these functions.

Enable/Delay (EN/DLY)

Allows delayed turn on of the buck regulator. Increase the value of capacitor C13 to increase the start-up delay of the MIC22950.

Shutdown (SHDN)

SHDN allows enable/disable of the buck regulator. SHDN is pulled to GND through a 100kΩ resistor. When SHDN is low the buck regulator operates normally. Force SHDN high to disable the buck regulator.

Delay (DELAY)

DELAY allows a delayed buck regulator Power Good (PG) indication. Install capacitor C11 to increase the Power Good delay timing of the MIC22950. DELAY also delays the ramp down of the MIC22950 output at turn-off.

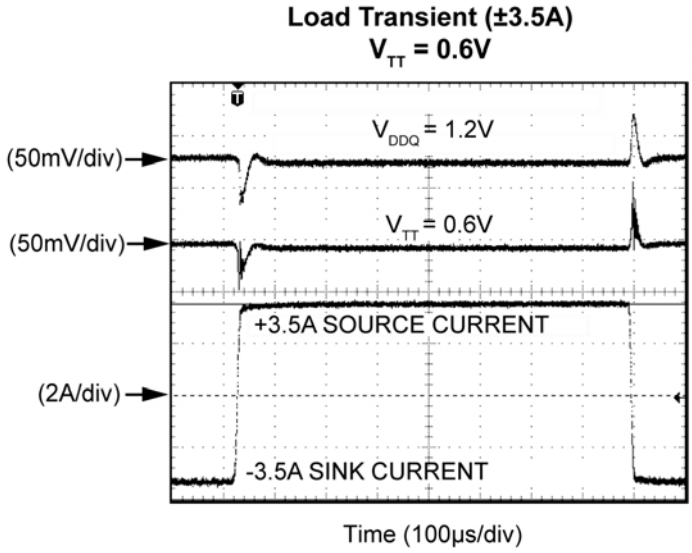
Ramp Control (RC)

Ramp control allows slowing the slew rate of the MIC22950 output. Increase the value of capacitor C12 to reduce the slew rate.

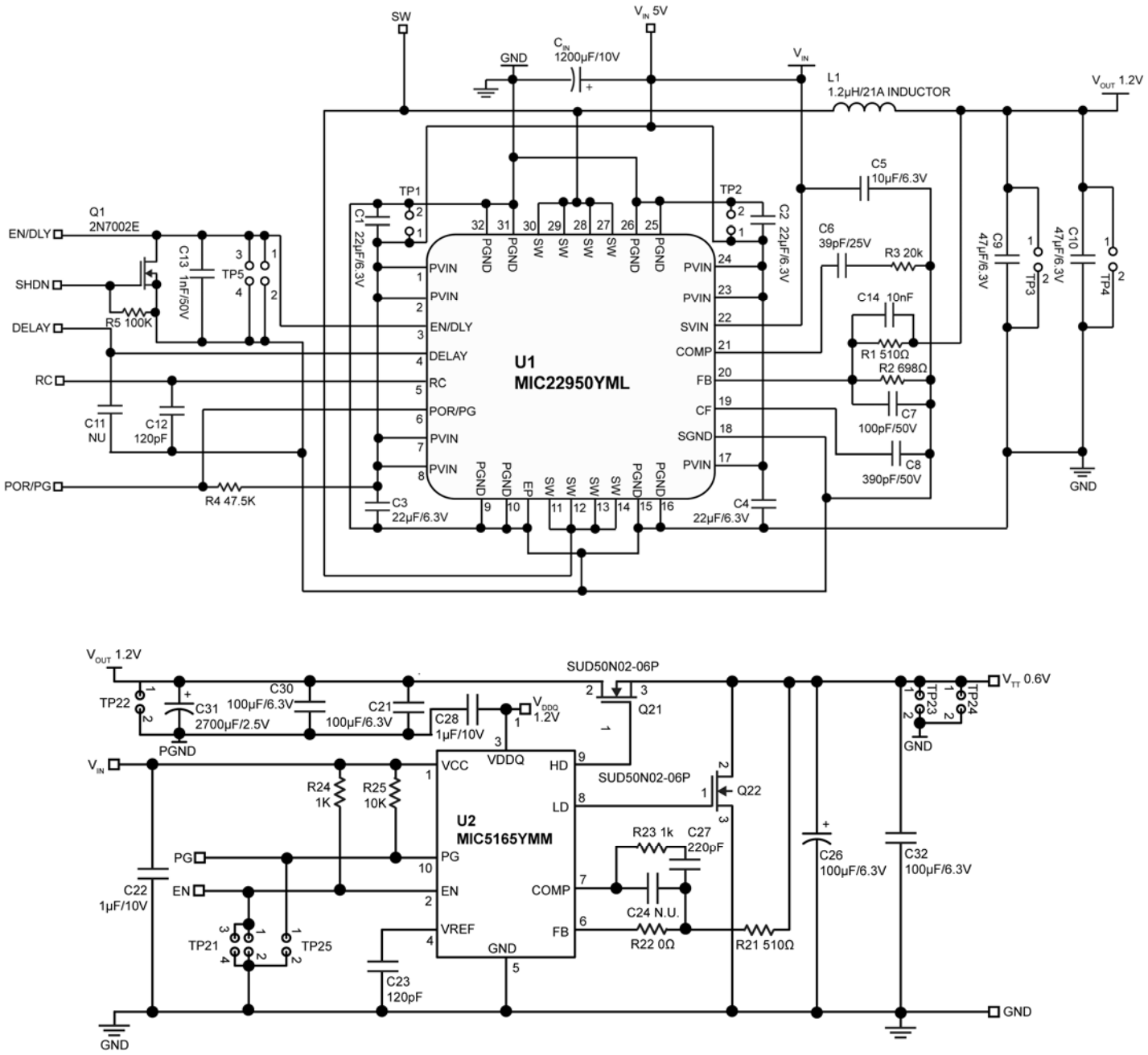
Power-On-Reset/Power Good (POR/PG)

Open drain output POR/PG pulls low when the output voltage of the MIC22950 is out of specification. POR/PG is pulled up to V_{IN} by a 47.5kΩ resistor.

Typical Characteristics



Evaluation Board Schematic



MIC5165 as a DDR3 Memory Termination Device for 3.5A Application
(V_{DDQ} and MOSFET Input are Separate Supplies)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	GRM21BR60J226ME39L	Murata[1]	22µF, 6.3V, Ceramic Capacitor, X5R, 0805	4
	C2012X5R0J226M	TDK[2]		
	08056D226MAT2A	AVX[3]		
C5	GRM188R60J106ME47D	Murata[1]	10µF, 6.3V, Ceramic Capacitor, X5R, 0603	1
	C1608X5R0J106M	TDK[2]		
	06036D106MAT2A	AVX[3]		
C6	GRM1885C1H390JA01D	Murata[1]	39pF, 50V, Ceramic Capacitor, NPO, 0603	1
	C1608C0G1H390J	TDK[2]	39pF, 25V, Ceramic Capacitor, NPO, 0603	
C7	06035C101MAT2A	AVX[3]	100pF, 50V, Ceramic Capacitor, X7R, 0603	1
C8	GRM188R71H391KA01D	Murata[1]	390pF, 50V, Ceramic Capacitor, X7R, 0603	1
C9, C10	GRM31CR60J476ME19L	Murata[1]	47µF, 6.3V, Ceramic Capacitor, X5R, 1206	2
	C3216X5R0J476M	TDK[2]		
	12066D476MAT2A	AVX[3]		
C13	GRM188R71H102KA01D	Murata[1]	1nF, 50V, Ceramic Capacitor, X7R, 0603	1
C14	GRM188R71H103KA01D	Murata[1]	10nF, 50V, Ceramic Capacitor, X7R, 0603	1
C22, C28	0603ZD105KAT2A	AVX[3]	1µF, 10V, Ceramic Capacitor, X5R, 0603	2
	GRM188R61A105K	Murata[1]		
C23, C12	VJ0603A121JXACW1BC	Vishay[4]	120pF, 25V, Ceramic Capacitor, NPO, 0603	2
	06033A121JAT2A	AVX[3]		
C27	VJ0603Y221KXACW1BC	Vishay[4]	220pF, 50V, Ceramic Capacitor, X7R, 0603	1
	06033C221JAT2A	AVX[3]	220pF, 25V, Ceramic Capacitor, X7R, 0603	
C26	TCJB107M006R0070	AVX[3]	100µF, 6.3V, Tantalum Capacitor, 1210	1
C24, C11			N.U. (Not Used) 0603 Ceramic Capacitor	
C30, C32, C21	C4532X5R0J107M	TDK[2]	100µF, 6.3V, Ceramic Capacitor, X5R, 1812	3
C31	Open (2SEPC2700M)	Sanyo[5]	2700µF, 2.5V Oscon Capacitor	1
CIN	EEE-FPA122UAP	Panasonic[6]	1200µF, 10V, Electrolytic Capacitor, SMD, 10x10.2-case	1
L1	CDEP105ME-1R2MC	Sumida[7]	1.2µH, 21A, Inductor, 10.4mmX10.4mm	1
Q1	2N7002E(SOT-23)	Vishay[4]	Signal MOSFET, SOT-23-6	1
Q21, Q22	SUD50N02-06P	Vishay[4]	Low VGS(th) N-Channel 20-V (D-S)	2

Notes:

1. Murata: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com.
4. Vishay: www.vishay.com.
5. Sanyo: www.sanyo.com.
6. Panasonic.: www.panasonic.com.
7. Sumida: www.sumida.com.

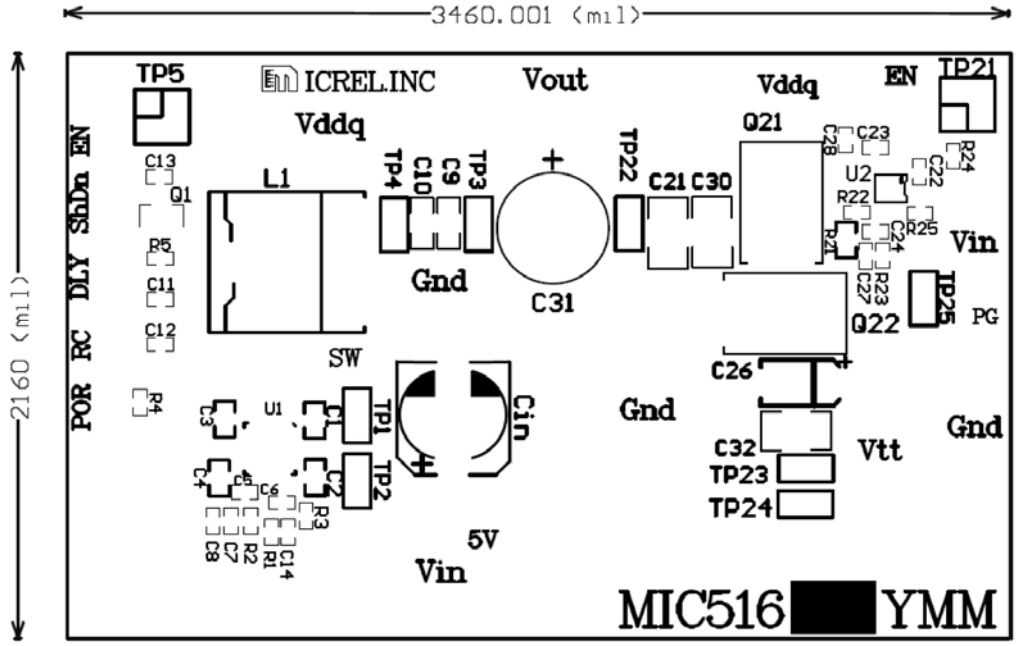
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R1	CRCW0603510RFRT1	Vishay Dale[4]	510Ω, Resistor, 1%, 0603	1
R2	CRCW0603698RFRT1	Vishay Dale[4]	698Ω, Resistor, 1%, 0603	1
R3	CRCW06032002FRT1	Vishay Dale[4]	20K, Resistor, 1%, 0603	1
R4	CRCW06034752FRT1	Vishay Dale[4]	47.5K, Resistor, 1%, 0603	1
R5	CRCW06031003FRT1	Vishay Dale[4]	100K, Resistor, 1%, 0603	1
R21	CRCW0805510RFKTA	Vishay Dale[4]	510Ω, Resistor, 1%, 0805	1
R23, R24	CRCW06031K00FKTA	Vishay Dale[4]	1K, Resistor, 1%, 0603	2
R22	CRCW06030000FKTA	Vishay Dale[4]	0Ω, Resistor, 1%, 0603	1
R25	CRCW06031002FRT1	Vishay Dale[4]	10K, Resistor, 1%, 0603	1
U1	**MIC22950YML**	**Micrel[8]**	**Buck Regulator 10A, 0.4MHz-2MHz Synchronous Buck Regulator**	1
U2	**MIC5165YMM**	**Micrel[8]**	**Dual Regulator Controller for DDR3**	1

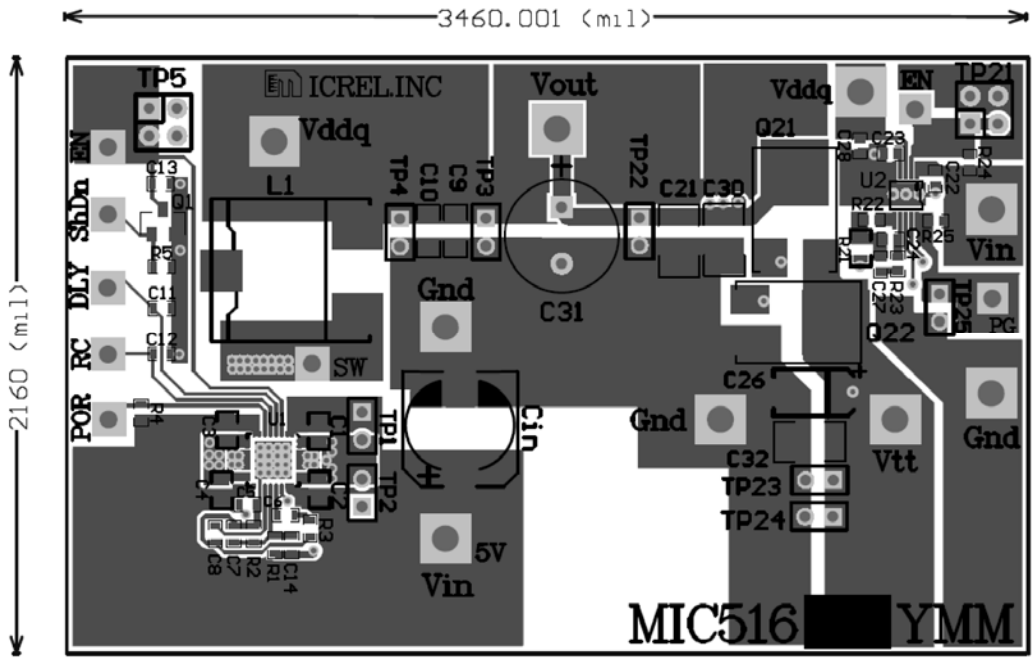
Note:

8. **Micrel, Inc**.: www.micrel.com.

Evaluation Board PCB Layout

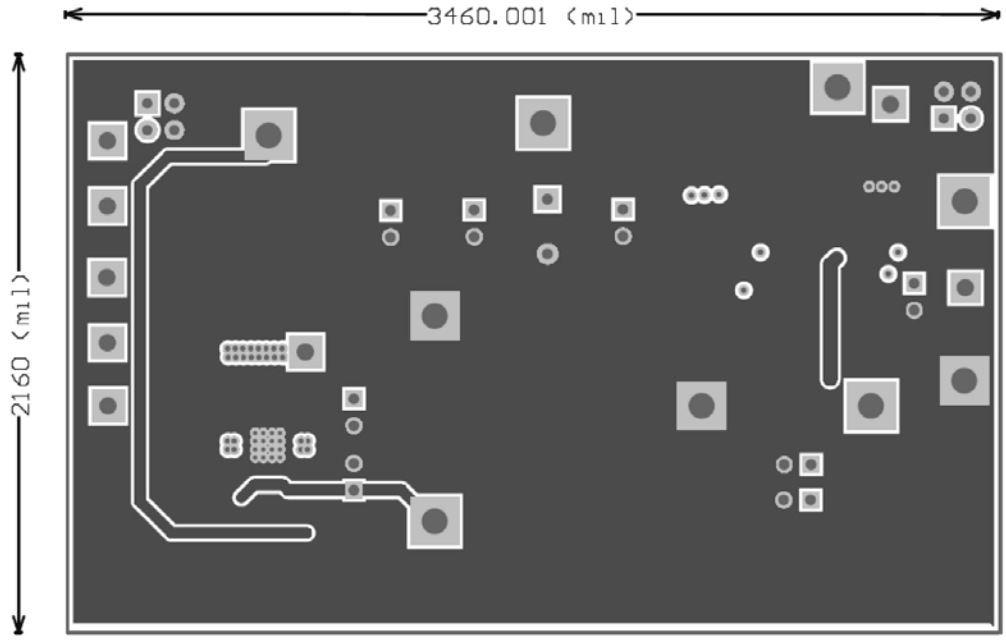


Top Silk

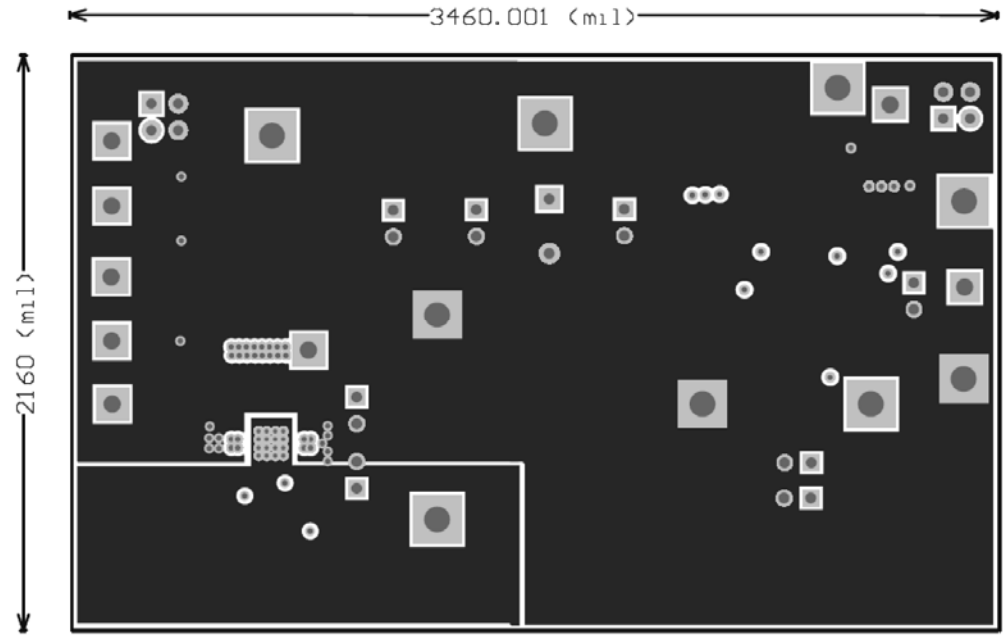


Top Layer

Evaluation Board PCB Layout (Continued)

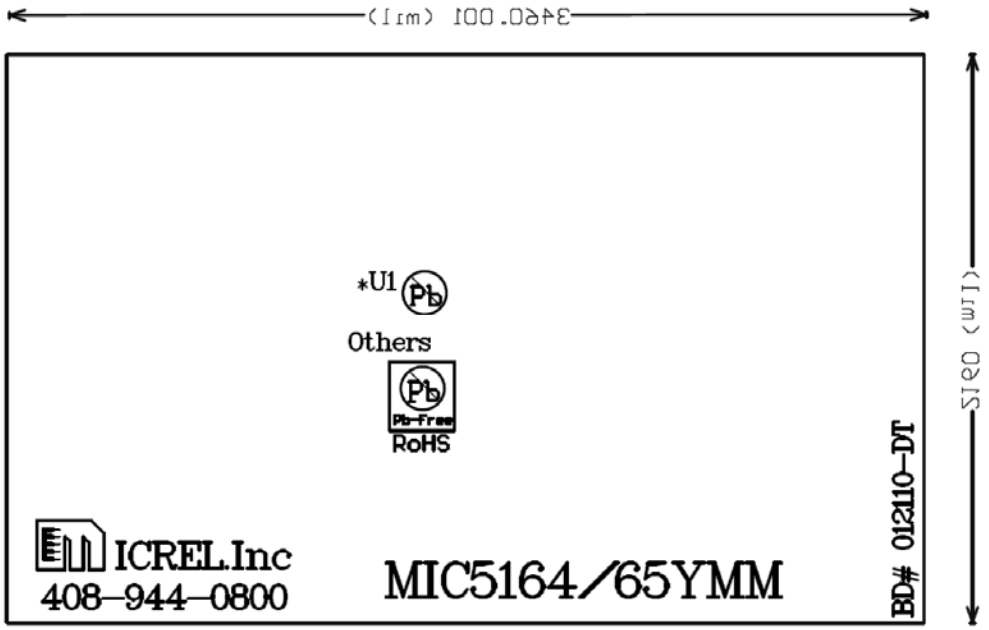


Middle Layer 1

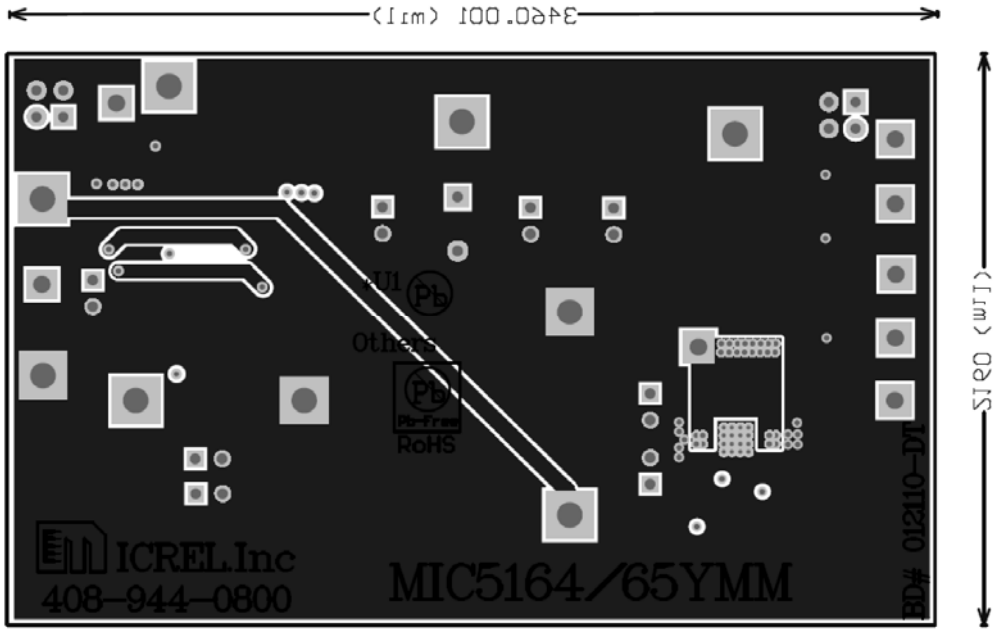


Middle Layer 2

Evaluation Board PCB Layout (Continued)



Bottom Silk



Bottom Layer

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