# AN3257
# Application note

## STEVAL-ISA080V1 90 W-HB LLC resonant converter based on the L6585DE combo IC

## Introduction

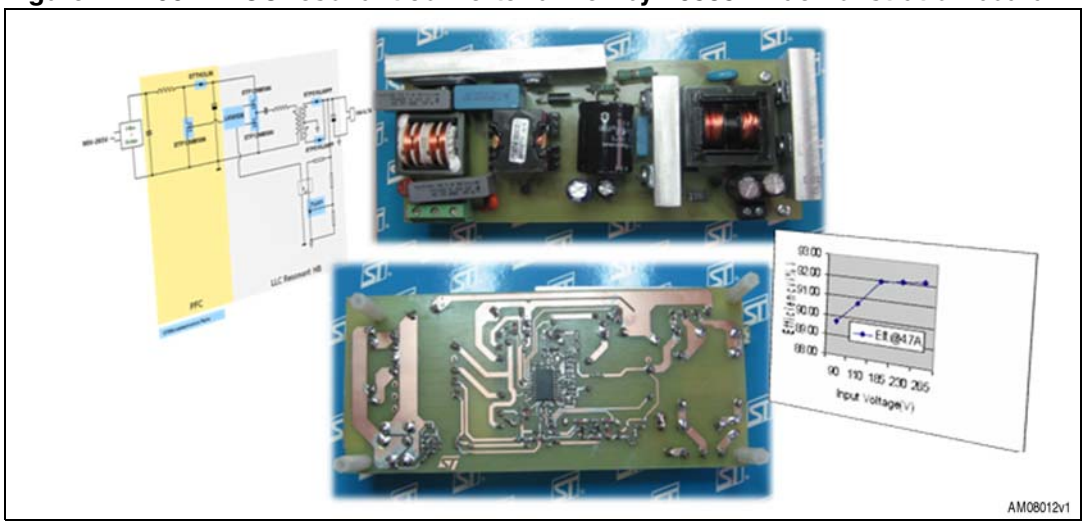
This application note describes the performance of a 90 W, wide range mains, power factor corrected AC-DC power supply demonstration board.

The architecture is based on a two-stage approach: a front-end PFC pre-regulator and a downstream multi-resonant half bridge converter. Both stages are controlled by the new IC - L6585DE- which integrates PFC and half bridge control circuits and the relevant drivers. Although this new device is dedicated to managing electronic ballast, it's possible to use it also for a HB-LLC resonant converter.

The PFC section achieves current mode control operating in transition mode, offering a highly linear multiplier including a THD optimizer which allows for an extremely low THD, even over a large range of input voltages and loading conditions.

The HB controller offers the designer a very precise oscillator, a logic that manages all the operating steps and a full set of protection features dedicated to lighting applications but useful also for the resonant converter.

**Figure 1. 90 W LCC resonant converter driven by L6585DE demonstration board**



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# 1 Basis of the HB-LLC resonant converter

The LLC resonant half bridge belongs to the family of multi-resonant converters. Actually, as the resonant tank includes three reactive elements (Cr, Ls and Lp, shown in *Figure 2*), there are two resonant frequencies associated with this circuit. One is related to the condition of the secondary winding(s) conducting, where the inductance Lp disappears because it is dynamically shorted out by the low-pass filter and the load (there is a constant Vout voltage across it):

**Equation 1**

$$f_{R1} = \frac{1}{2\pi\sqrt{L_S \cdot C_R}}$$

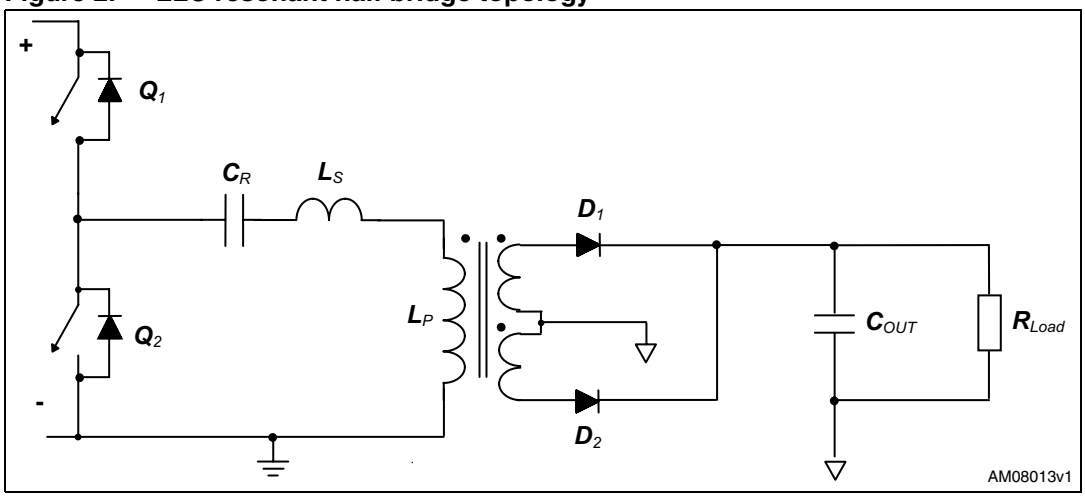
The other resonant frequency is relevant to the condition of the secondary winding(s) open, where the tank circuit turns from LLC to LC because Ls and Lp can be unified in a single inductor:

**Equation 2**

$$f_{R2} = \frac{1}{2\pi\sqrt{(L_S + L_P) \cdot C_R}}$$

It is possible to show that for frequencies $f > f_{R1}$, the input impedance of the loaded resonant tank is inductive and that for frequencies $f < f_{R2}$, the input impedance is capacitive. In the frequency region $f_{R2} < f < f_{R1}$, the impedance can be either inductive or capacitive depending on the load resistance $R_{out}$. The LLC resonant converter is normally operated in the region where the input impedance of the resonant tank has an inductive nature, i.e. it increases with frequency. This implies that power flow can be controlled by changing the operating frequency of the converter in such a way that a reduced power demand from the load produces a frequency rise, while an increased power demand causes a frequency reduction.

**Figure 2. LLC resonant half bridge topology**



The most significant advantages of this topology are:

- Soft-switching of all semiconductor devices: ZVS (zero-voltage switching) at turn on for the MOSFETs and ZCS (zero-current switching) at both turn on and turn off for the secondary rectifiers. The first property results from the correct design of the resonant tank. The second one is a natural feature of the topology.
- Ability to accommodate an extremely broad load range, including zero load, with an acceptable frequency variation. Also this property results from the correct design of the resonant tank.
- Magnetic integration, which allows the combination of different magnetic devices into a single physical device.

As a result of all the above factors, high efficiency, high switching frequency capability, and high power density are typical characteristics of the converters based on this topology.

Operation at resonance is the preferred operating point, where load regulation is ideally zero, where tank current is maximally sinusoidal, and where peak tank current is minimized for a given power throughput.

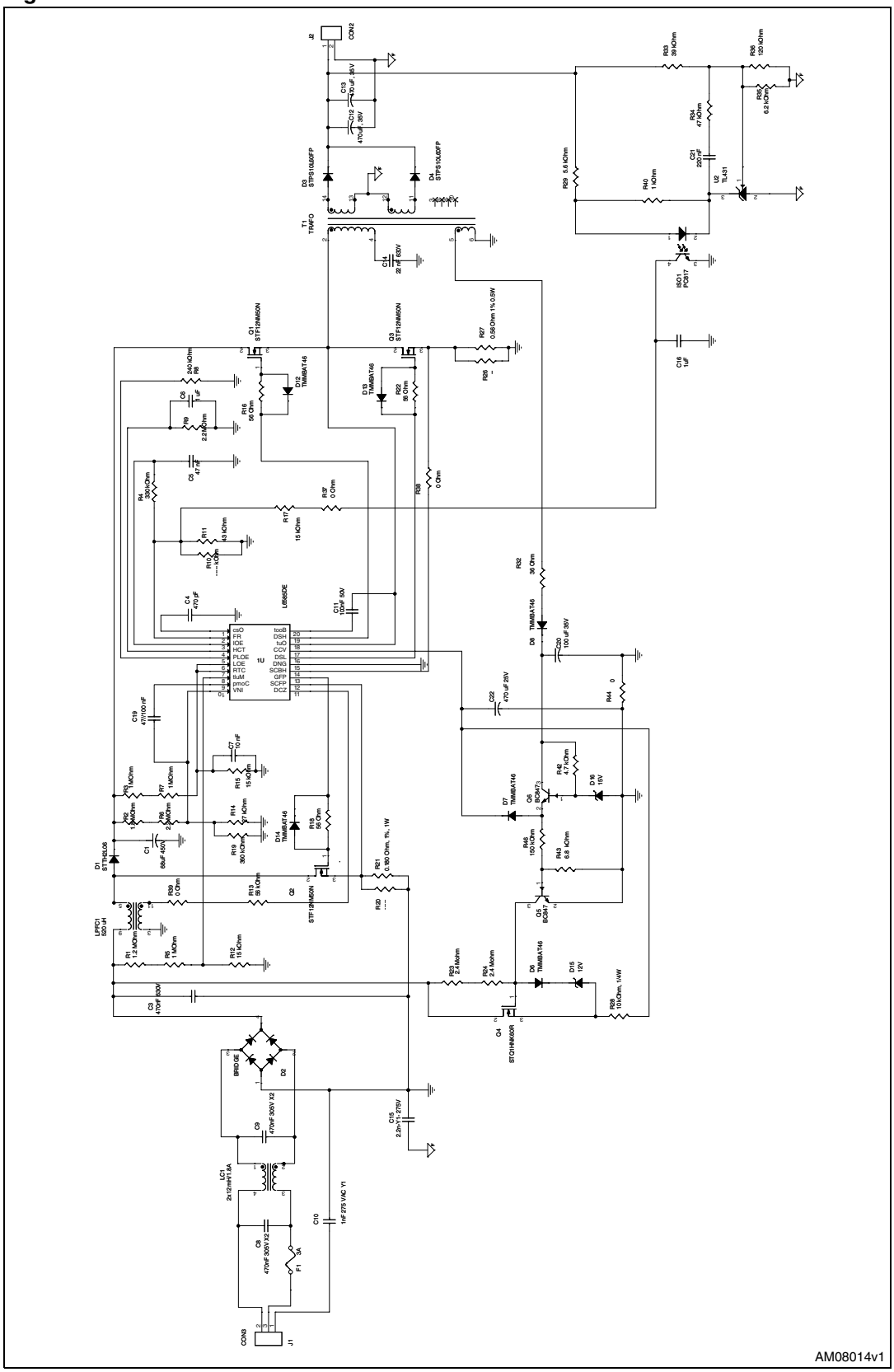
# 2 Main characteristics

The SMPS electrical specifications are shown in *Table 1* and the schematic is presented in *Figure 3*.

**Table 1. Electrical specifications**

| Input parameters | | |
|---|---|---|
| $V_{IN}$ | Input voltage range | 90 to 265 $V_{RMS}$ |
| $f_{line}$ | Line frequency | 50/60 Hz |
| Output parameters | | |
| $V_{OUT}$ | Output voltage | 19 V |
| $I_{OUT}$ | Output current | 4.7 A |

**Figure 3. Schematic**



# 3 SMPS design

The design of the major circuit parts is described in this section.

## 3.1 L6585DE biasing circuitry (pin-by-pin)

- Pin 1 OSC: is one of the two oscillator inputs. The value of the capacitor connected to ground defines the half bridge switching frequency in each operating state. $C_4$=470 pF value was chosen.
- Pin 2 RF: the component choice with oscillator capacitance defines the half bridge switching frequency in each operating state. A resistor $R_{11}$ connected to ground sets the run frequency that, for resonant converters, represents the minimum frequency. For a lamp ballast, during the preheating time (startup time) the switching frequency is set by the parallel of the above resistance with the one $R_4$ connected between pins RF and EOI; in this case (resonant converter design) it is true until the control loop take over by means and the optocoupler. Choosing the following frequencies:

**Equation 3**

$$f_{run} = f_{min} = 62.5kHz \quad f_{pre} = f_{start-up}\,70kHz \quad t_{ign} = 46ms$$

it is possible calculate $R_{11}$ by following the formula:

**Equation 4**

$$e = 1 - \frac{1.33}{(C_4)^{0.581}} \qquad k = \frac{499.6 \cdot 10^3}{(C_4)^{0.872}} \qquad R_{11} = \left(\frac{k}{f_{run}}\right)^{1/e} = 43k\Omega$$

and so the $R_4$ value is:

**Equation 5**

$$R_{11} // R_4 = \left(\frac{k}{f_{pre}}\right)^{1/e} \Rightarrow R_4 = 330k\Omega$$

- Pin 3 EOI: for lamp ballast applications, the net $C_5$-$R_4$ on the EOI pin is needed to set the frequency change from preheating mode to run mode. In the resonant converter this change, similar to the one between startup frequency and steady-state, is influenced at the start by the feedback response. However, the $C_5$-$R_4$ choice was made as it would be an electronic ballast; as $R_4$ value has already been calculated and $t_{ign}$ at start fixed, $C_5$ value is calculated by the following formula:

**Equation 6**

$$C_5 = \frac{t_{ign}}{3 \cdot R_4} = 47nF$$

- Pin 4 TCH: is the time counter and it is activated at startup as well as after a protection - HBCS crossing during run mode - triggering. To achieve this, an $R_9C_6$ parallel network is connected between this pin and ground. Fixing a protection time $t_{Tch,reduced}$=0.27 sec (needed for overcurrent protection) it is possible to calculate $C_6$:

**Equation 7**

$$C_6 \cong t_{Tch,reduced} \cdot \frac{1}{0.26974 \cdot 10^6} = 1.03\mu F \Rightarrow C_6 = 1\mu F$$

Choosing $t_{pre}$=1.25 sec and considering the internal current generator $I_{CH}$=31 µA, it's possible to calculate $R_9$:

**Equation 8**

$$R_9 = \frac{t_{pre} - \frac{C_6}{I_{CH}} \cdot 4.63}{C_6 \cdot \ln\frac{4.63}{1.5}} = 2.24M\Omega \Rightarrow 2.2M\Omega$$

- Pin 5 EOLP: is a 2 V reference and allows programming of the window comparator of pin6 (EOL) according to table 5 of the L6585DE datasheet. Working in CTR tracking configuration and choosing a window voltage amplitude ± 240 mV, $R_8$=240 kΩ was inserted.
- Pin 6 EOL: is the input for the window comparator dedicated to lighting application protection (lamp end of life detection). For the HB-LLC resonant converter it was disabled; to do this, the EOL pin was directly connected to the CTR pin.
- Pin 7 CTR: this is a multifunction pin (PFC overvoltage, feedback disconnection, reference for EOL pin in case of tracking reading), connected to a resistive divider to the PFC output bus. Establishing the maximum PFC overvoltage PFC output overshoot (e.g. at startup) of $V_{OVPBUSpfc}$=456 V and considering that the corresponding threshold on the CTR pin must be $V_{thrCTR}$=3.4 V it's possible to calculate $R_3$+$R_7$=2 MΩ and $R_{15}$=15 kΩ.
- Pin 8 MULT: first, the maximum peak value for $V_{MULT}$, $V_{MULTmax}$, is selected. This value, which occurs at maximum mains voltage, should be 3 V (linearity limit) or nearly so in wide range mains and less in case of single mains. The PFC sense resistor selected is $R_S$ = $R_{21}$=0.18 Ω and it is described in the information relating to pin12. Considering the maximum slope of multiplier maxslope=0.75, the maximum peak value, occurring at maximum mains voltage is:

**Equation 9**

$$V_{MULTmax} = \frac{I_{Lpk} \cdot R_{21}}{\text{max slope}} \cdot \frac{V_{ACmax}}{V_{ACmin}} = \frac{2 \cdot \sqrt{2} \cdot \frac{P_{out}}{\eta \cdot V_{ACmin} \cdot PF} \cdot R_{21}}{\text{max slope}} \cdot \frac{V_{ACmax}}{V_{ACmin}} = 2.46$$

it's possible to calculate the multiplier divider ε:

**Equation 10**

$$\varepsilon = \frac{R_{12}}{R_{12} + (R_5 + R_1)} = \frac{V_{MULTmax}}{\sqrt{2} \cdot V_{ACmax}} = \frac{2.46}{\sqrt{2} \cdot 265} = 6.58 \cdot 10^{-3}$$

Supposing 165 µA is the current flowing into the divider, the lower resistor $R_{12}$ value can be calculated and so the upper resistance $R_5$ + $R_1$ value is:

**Equation 11**

$$R_{12} = \frac{V_{MULTmax}}{165\mu A} = 15.2k\Omega \Rightarrow R_{12} = 15k\Omega$$

$$R_5 + R_1 = \frac{1-\varepsilon}{\varepsilon} \cdot R_{12} = 2.264M\Omega \Rightarrow R_5 + R_1 = 2.2M\Omega$$

The voltage on the multiplier pin with the selected component values is recalculated at minimum line voltage, 0.86 V, and at maximum line voltage, 2.53 V. So the multiplier works correctly within its linear region.

- Pin 9 COMP: is the output of the E/A and also one of the two inputs of the multiplier. The feedback compensation network, placed between this pin and INV (10), is just the $C_{19}$ network:

**Equation 12**

$$C_{19} = 147nF$$

- Pin 10 INV: to implement the voltage control loop, a resistive divider is connected between the regulated output voltage $V_{BUSpfc}$=400 V of the boost and the pin. The internal reference on the non inverting input of the E/A is 2.5 V, so $R_6$ and $R_2$ (*Figure 3*) is then selected (fixing $R_{14}$=27 kΩ, R19=360 kΩ, $\Rightarrow R_{14}//R_{19}$=25.11 kΩ), as follows:

**Equation 13**

$$\frac{R_6 + R_2}{R_{14} // R_{19}} = \frac{V_{BUSpfc}}{2.5} - 1$$

$$\Rightarrow R_6 + R_2 = 4M\Omega$$

- Pin 11 ZCD: is the input to the zero-current detector circuit. The ZCD pin is connected to the auxiliary winding of the boost inductor through a limiting resistor $R_{13}$. The ZCD circuit is negative-going edge triggered: when the voltage on the pin falls below 0.7 V the PWM latch is set and the MOSFET is turned on. To do so, however, the circuit must be first armed: prior to falling below 0.7 V the voltage on pin 11 must experience a positive-going edge exceeding 1.4 V (due to MOSFET's turn-off). The maximum main to-auxiliary winding turn ratio, m, has to ensure that the voltage delivered to the pin during MOSFET's OFF-time is sufficient to arm the ZCD circuit. Then:

**Equation 14**

$$m \leq \frac{V_{BUSpfc} - \sqrt{2} \cdot V_{inRMS(max)}}{1.4} = 33.10$$

m=10 was chosen.

Considering the upper and lower clamp voltage of the ZCD pin, its minimum current sink current capability, according to the max and min voltage of the PFC bus, it was possible to calculate and to choose $R_{13}$=56 kΩ.

- Pin 12 PFCS: is the inverting input of the current sense comparator. As the voltage across the sense resistor (proportional to the instantaneous inductor current) crosses the threshold set by the multiplier output, the power MOSFET is turned off. By following the indication reported below, it's possible to determinate the PFC sense resistor:

**Equation 15**

$$I_{Lmax} = \frac{2 \cdot \sqrt{2} \cdot \frac{P_{outTOT}}{\eta}}{V_{ACmin} \cdot PF} = 3.48A$$

$$R_{21} < \frac{V_{CSmin}}{I_{Lmax}} = 0.28\Omega$$

$R_{21}$=180 mΩ with a power rating of 1 W was chosen.

- Pin 13 PFG: to correctly drive the external MOSFET, a resistor R18=56 Ω was used.
- Pin 14 HBCS: considering the tank peak current of the LLC resonant converter (calculated as described in “Designing LLC resonant converter for optimum efficiency” EPE2009, Barcelona, Spain, September2009, ISBN:9789075815009) $I_{Rpk}$=0.86 A and considering the HBCS threshold during the run phase $V_{HBCS}$=1 V, it is possible to calculate $R_{27}$ as:

**Equation 16**

$$R_{27} < \frac{V_{HBCS}}{I_{Rpk}} = \frac{1}{0.86} = 1.16\Omega$$

$R_{27}$=0.56 Ω with a power rating of 1 W was chosen.

- Pin 15 GND: device ground
- Pin 16 LSD: to correctly drive the external half bridge low side MOSFET, resistor $R_{22}$=56 Ω was used. To reduce the MOSFET turn-off losses, a diode $D_{13}$=1N4148 was inserted, in parallel to $R_{22}$.
- Pin 17 Vcc: this pin is externally connected to the dynamic startup circuit (by means of $R_{23}$, $R_{24}$, $Q_4$, $D_6$, $D_{15}$, and $R_{28}$) and to the self supply circuit composed by the net ($R_{32}$, $D_8$, $C_{20}$, $R_{42}$, $D_{16}$, $Q_6$, $D_7$, $C_{22}$, $R_{46}$, $R_{43}$, and $Q_5$).
- Pin 18 out: high side driver floating reference. This pin is connected close to the source of the high side power MOSFET.
- Pin 19 HSD: to correctly drive the external half bridge low side MOSFET, a resistor $R_{16}$=56 Ω was used . To reduce the power MOSFET turn-off losses, a diode $D_{12}$=1N4148 was inserted, in parallel to $R_{16}$.
- Pin 20 boot: for the high side section $C_{11}$= 100 nF was selected.

## 3.2 PFC power section design

### Input capacitor

The input high frequency filter capacitor must attenuate the switching noise due to the high frequency inductor current ripple. The worst conditions occur on the peak of the minimum rated input voltage $V_{ACmin}$=90 V. Establishing the following values:

- the coefficient of maximum high frequency voltage ripple r= 0.12
- total system efficiency η=0.9

It is possible, considering the minimum PFC switching frequency $f_{minpfc}$=36 kHz and the total output power $P_{outTOT}$=90 W, to determinate input capacitor $C_3$ in the following way:

**Equation 17**

$$C_3 = \frac{\frac{P_{outTOT}}{\eta \cdot V_{ACmin}}}{2 \cdot \pi \cdot f_{minpfc} \cdot V_{ACmin} \cdot r} = 457nF$$

$C_3$=470 nF was inserted.

### Output capacitor

The output bulk capacitor $C_1$ selection depends on the DC output voltage, the admitted overvoltage, the output power, and the desired voltage ripple. Establishing the following values:

- PFC output voltage $V_{busPFC}$=400 V
- the coefficient of low frequency (twice the mains frequency $f_{main}$=50 Hz) voltage ripple $r_1$=0.05

It is possible to calculate the bulk capacitor in the following way:

**Equation 18**

$$C_1 = \frac{\frac{P_{outTOT}}{V_{busPFC}}}{2\pi \cdot 2f_{main} \cdot V_{busPFC} \cdot r_1} = 17.9\mu F$$

To have a smaller ripple and good reliability, the following commercial capacitor was chosen: C1=68 µF, 450 V.

### Boost inductor

The inductance $L_{pfc}$ is usually determined so that the minimum switching frequency $f_{minpfc}$ is greater than the maximum frequency of the internal starter, to ensure a correct TM operation. Considering the minimum suggested value for PFC section $f_{minpfc}$=20 kHz, and that this last one can occur at the either the maximum $V_{ACmax}$=265 V or the minimum $V_{ACmin}$=90 V mains voltage, the inductor value is:

**Equation 19**

$$L_{pfc} = \frac{V_{AC}^2 \cdot \left(V_{busPFC} - \sqrt{2} \cdot V_{AC}\right)}{2 \cdot f_{minpfc} \cdot \frac{P_{out}}{\eta} \cdot V_{busPFC}}$$

To margin from $f_{minpfc}$, $f_{pfc}$=36 kHz was chosen. In this condition the lower value for the inductor is determined by $V_{AC}$=$V_{ACmin}$ and results $L_{pfc}$=0.7 mH with, as explained in the PFCS pin description, a maximum current $I_{Lmax}$=3.48 A. (the inductor 1974.0002 was used, manufactured by MAGNETICA).

### Power MOSFET

The choice of the MOSFET concerns mainly its $R_{DS(on)}$, which depends on the output power and its breakdown voltage; this last voltage is fixed just by the output voltage $V_{buspfc}$=400 V, plus the overvoltage $\Delta V_{OVPpfc}$=60 V admitted and a safety margin.

The MOSFET's power dissipation depends on conduction and switching losses. Establishing a maximum total power loss, $P_{lossesAdm}$=1 % $P_{out}$=0.9 W, it is easy to verify that

choosing MDmesh II power MOSFET STF12NM50N, the estimated total MOSFET power loss, in the worst case, is about $P_{lossesEst}$=0.75 W so this choice was the definitive one. To dissipate the power losses in a better way, a heatsink was added.

### Boost diode

The boost freewheeling diode is a fast recovery one. The breakdown voltage is fixed following a similar criterion as that for the MOSFET 1.2* ($V_{out}$ + $\Delta V_{OVP}$). The value of its DC and RMS current, needed to choose the current rating of the diode, are:

**Equation 20**

$$I_{D1dc} = \frac{P_{outTOT}}{V_{BUSpfc}} = 0.225A$$

$$I_{D1rms} = 2\sqrt{2} \cdot I_{ACmax} \cdot \sqrt{\frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{ACmin}}{V_{BUSpfc}}} = 0.62A$$

As the PFC works in transition mode, the Turbo 2 Ultrafast high voltage rectifier, STTH2L06, was selected.

## 3.3 LLC resonant circuit design

Using what is commonly known as the “first harmonic approximation” (FHA) technique, the LLC resonant circuit was designed. Considering the following converter specifications:

- Nominal input DC voltage: 400 V
- Output Voltage: 19 V @ 4.7 A
- Resonance frequency: 90 kHz
- Minimum operating frequency: 60 kHz
- Maximum operating frequency: 230 kHz
- Delay time (L6585DE datasheet): 1.2 µs
- Foreseen capacitance at half bridge node: 120 pF.

It was possible, by means of the AN2450 application note, to calculate the resonant power transformer and the resonant capacitor specification. The transformer 1860.0045 was used, manufactured by MAGNETICA:

  - $L_p$=1200 µH
  - $L_r$=200 µH

and the resonant capacitor $C_r$=22 nF.

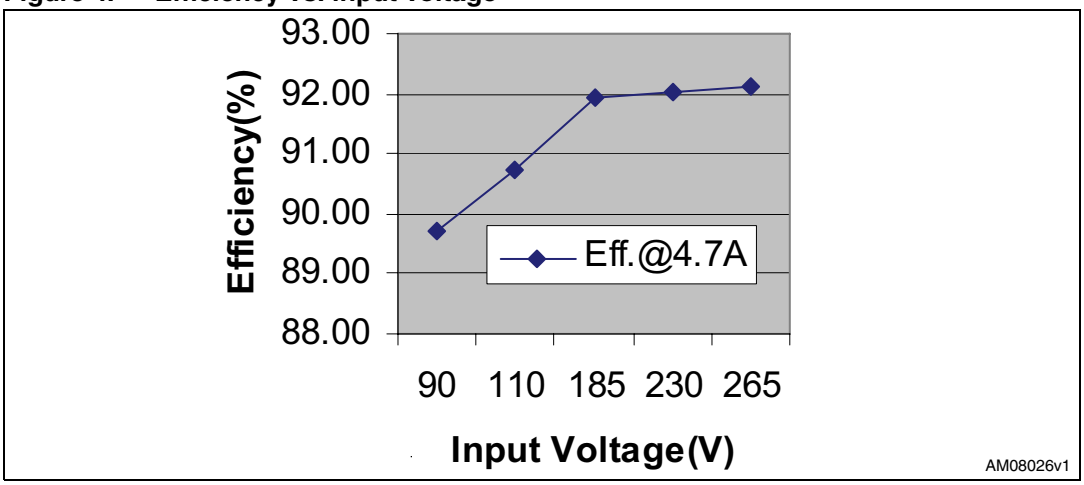
# 4 Experimental results

The schematic of the tested board is shown in *Figure 3*. First of all, the board was tried in terms of efficiency, power factor, total harmonic distortion, and thermal behavior for the input voltage range at nominal load; below, in *Table 2* and *Table 3.*, the results obtained for a 60 min test are shown.

**Table 2. Board performance**

| Vin (V) | Iout (A) | Vout (V) | Pout (W) | Pin (W) | Efficiency (%) | THD (%) | PF |
|---|---|---|---|---|---|---|---|
| 90 | 4.7 | 18.86 | 88.64 | 98.8 | 89.72 | 2.3 | 0.999 |
| 110 | 4.7 | 18.86 | 88.64 | 97.7 | 90.73 | 2.2 | 0.999 |
| 185 | 4.7 | 18.86 | 88.64 | 96.4 | 91.95 | 3.4 | 0.994 |
| 230 | 4.7 | 18.86 | 88.64 | 96.3 | 92.05 | 5.5 | 0.987 |
| 265 | 4.7 | 18.86 | 88.64 | 96.2 | 92.14 | 7.8 | 0.977 |

**Figure 4. Efficiency vs. input voltage**




The high efficiency of the PFC, working in transition mode, and the very high efficiency of the resonant stage, working in ZVS, provides, on average, an efficiency better than 91 %. For low input mains voltage the efficiency is just a little lower because PFC conduction losses increase.

**Table 3. Thermal results**

| $V_{IN}$(V) | Ambient temp (°C) | $MOS_{PFC}$ (°C) | $DIODE_{PFC}$ (°C) | $L_{PFC}$ (°C) | $MOS_{HB}$ (°C) | $L_{Resonant}$ (°C) | $DIODE_{output}$ (°C) | L6585DE (°C) |
|---|---|---|---|---|---|---|---|---|
| 90 | 25 | 59 | 65 | 53 | 37 | 61 | 72 | 44 |
| 110 | 25 | 53 | 62 | 50 | 37 | 60.5 | 70 | 44 |
| 185 | 25 | 44.5 | 55 | 41 | 40 | 57 | 70 | 44 |

**Table 3. Thermal results (continued)**

| $V_{IN}$(V) | Ambient temp (°C) | $MOS_{PFC}$ (°C) | $DIODE_{PFC}$ (°C) | $L_{PFC}$ (°C) | $MOS_{HB}$ (°C) | $L_{Resonant}$ (°C) | $DIODE_{output}$ (°C) | L6585DE (°C) |
|---|---|---|---|---|---|---|---|---|
| 230 | 25 | 40.2 | 52 | 39.8 | 39.7 | 57 | 70 | 44 |
| 265 | 25 | 40.2 | 50 | 37.8 | 39.7 | 57 | 70 | 44 |

*Table 4* and *5* show the output voltage and efficiency measurement at nominal mains with different load conditions powering the board at the two nominal input mains voltages.

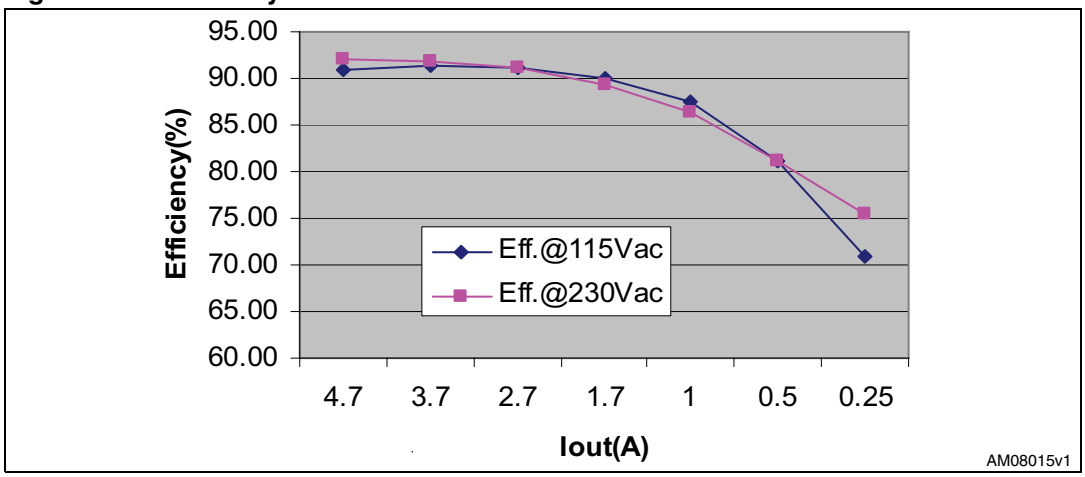
**Table 4. Efficiency measurements @ Vin=115 Vac**

| $V_{in}$(V) | $V_{out}$(V) | $I_{out}$(A) | $P_{out}$(W) | $P_{in}$(W) | Efficiency(%) |
|---|---|---|---|---|---|
| 115 | 18.86 | 4.7 | 88.60 | 97.4 | 90.96 |
| 115 | 18.88 | 3.7 | 69.82 | 76.5 | 91.27 |
| 115 | 18.92 | 2.7 | 51.06 | 56 | 91.17 |
| 115 | 18.95 | 1.7 | 32.22 | 35.8 | 89.99 |
| 115 | 18.98 | 1 | 18.98 | 21.7 | 87.47 |
| 115 | 18.99 | 0.5 | 9.50 | 11.7 | 81.15 |
| 115 | 19 | 0.25 | 4.75 | 6.7 | 70.90 |

**Table 5. Efficiency measurements @ Vin=230 Vac**

| $V_{in}$(V) | $V_{out}$(V) | $I_{out}$(A) | $P_{out}$(W) | $P_{in}$(W) | Efficiency(%) |
|---|---|---|---|---|---|
| *230* | 18.86 | 4.7 | 88.64 | 96.3 | 92.05 |
| *230* | 18.88 | 3.7 | 69.86 | 76 | 91.92 |
| *230* | 18.92 | 2.7 | 51.08 | 56 | 91.22 |
| *230* | 18.95 | 1.7 | 32.22 | 36.1 | 89.24 |
| *230* | 18.98 | 1 | 18.98 | 22 | 86.27 |
| *230* | 18.99 | 0.5 | 9.50 | 11.7 | 81.15 |
| *230* | 19 | 0.25 | 4.75 | 6.3 | 75.40 |

**Figure 5. Efficiency vs. Pout**

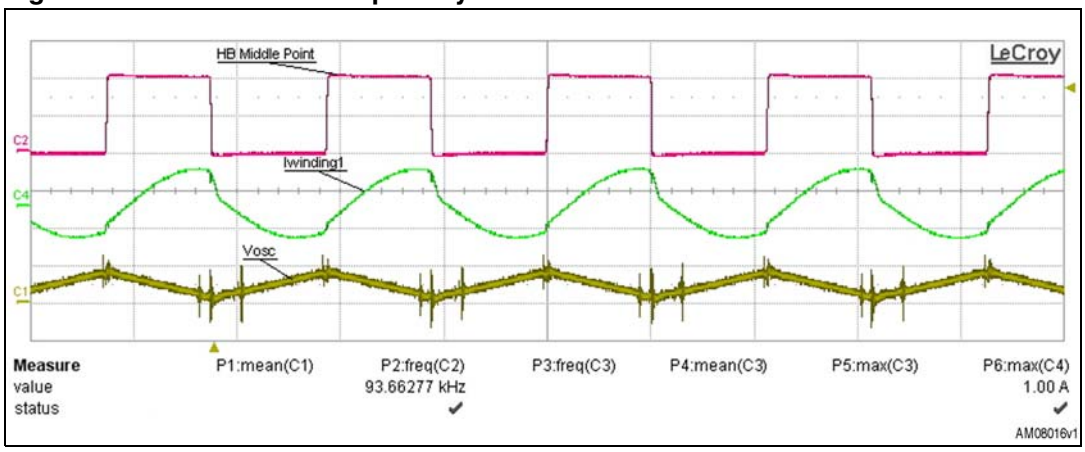



At lower loads the efficiency decreases because HB works at high frequency so the switching losses increase.

## Resonant stage operating waveforms

In *Figure 6* some waveforms are shown (HB middle point voltage, primary winding current, and oscillator voltage) during steady-state operation of the circuit at full load.

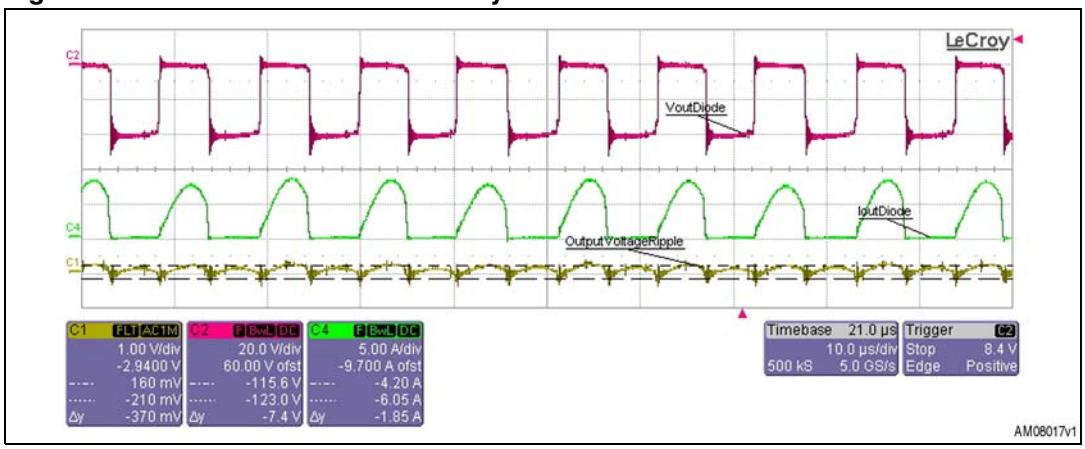
**Figure 6. Resonant circuit primary side waveforms**




The transformer primary current wave is almost sinusoidal because the operating frequency is slightly above the resonance one. In this condition, the circuit has a good margin for ZVS operations, providing good efficiency, and the almost sinusoidal wave shape provides for an extremely low EMI generation.

In *Figure 7* some waveforms relevant to the secondary side (output voltage ripple, current of one output diode, and output diode voltage) are shown.

**Figure 7. Resonant circuit secondary side waveforms**




The current in the diode is almost a sine wave and its average value is half of the output current while the rectifiers reverse voltage is, according to theoretical value, $2V_{OUT}+V_F$. The high frequency ripple of the output voltage is only 180 mV (0.93 %).

## No load power consumption and Load transition

In *Table 6* the power consumption in no load condition is given, while *Figure 8* shows the waveforms of the output voltage and the current during a load variation from 0 % to 100 %; the circuit response is fast enough to avoid output voltage dips. In *Figure 9*, the opposite load transition is checked (100 % to 0 %). Also in this case the transition doesn't show any problems for the output voltage regulation.

**Table 6. No load consumption**

| $V_{in}$ (V) | $I_{out}$ (A) | $V_{out}$ (V) | $P_{out}$ (W) | $P_{in}$ (W) |
|---|---|---|---|---|
| 90 | 0 | 19.01 | 0 | 1.3 |
| 110 | 0 | 19.01 | 0 | 1.2 |
| 185 | 0 | 19.01 | 0 | 1.1 |
| 230 | 0 | 19.01 | 0 | 1.1 |
| 265 | 0 | 19.01 | 0 | 1.1 |

**Figure 8. Load transition 0 % ==> 100 %**

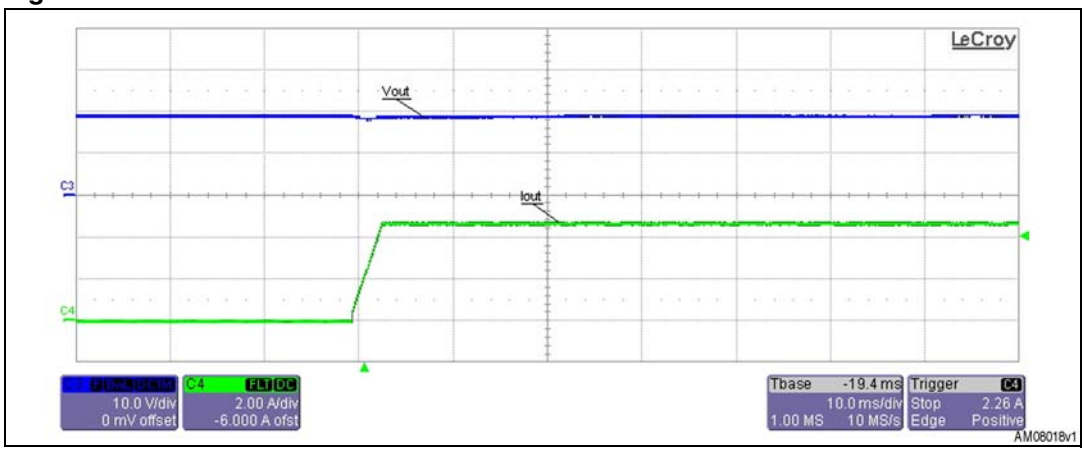
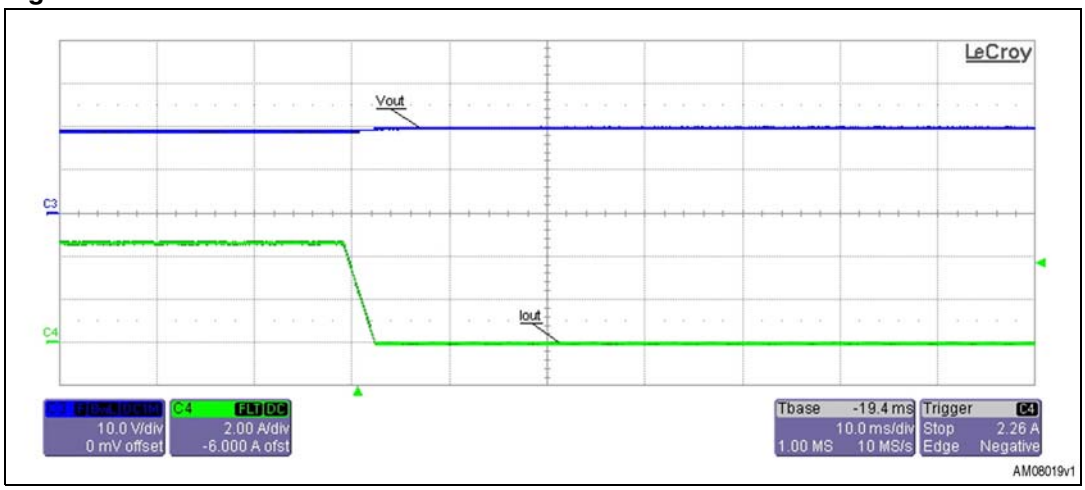



**Figure 9. Load transition 100 % ==> 0 %**




## Short-circuit protections and startup sequence

The L6585DE is equipped with, in the HB section, a current sensing input (pin14, HBCS) and a dedicated overcurrent management system. The current flowing in the circuit is detected and the signal is fed into the HBCS pin. It is internally connected to the input of the first comparator referenced to 1.6 V and to that of a second comparator referenced to 2.75 V. When one of the two comparators is activated, the IC is latched in low consumption mode.

In *Figure 10* the response system in short-circuit condition during run mode is shown; as soon as HBCS=1.6 V the IC is stopped.

**Figure 10. Short-circuit during run mode**

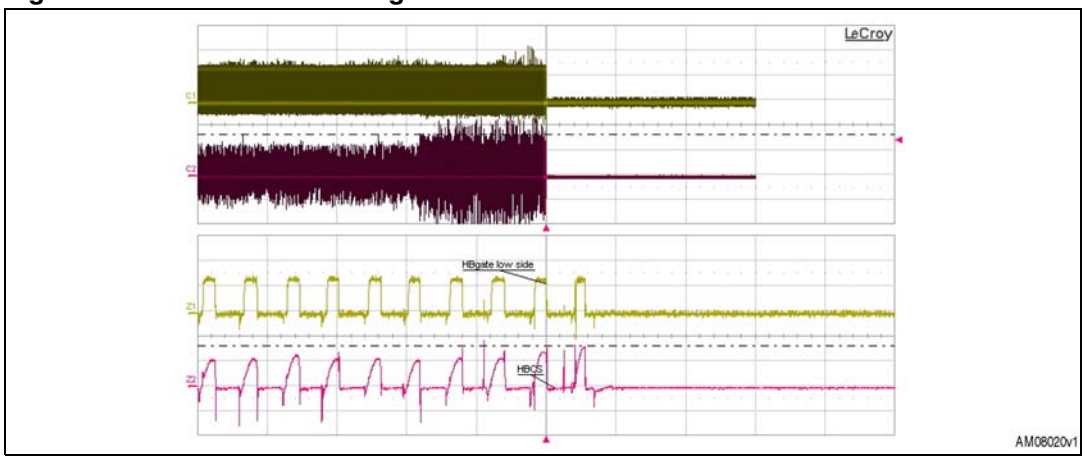
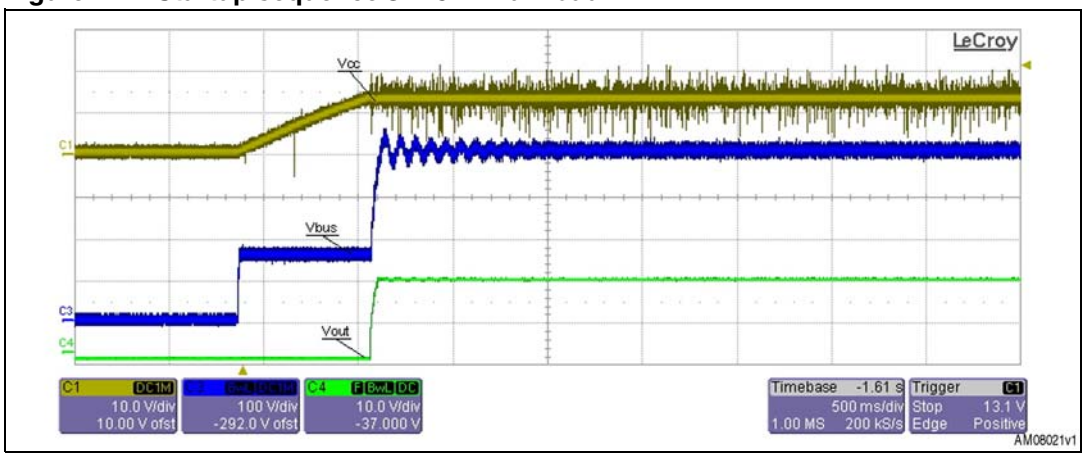



*Figure 11* shows the waveforms during startup at 115 Vac and full load.

**Figure 11. Startup sequence@115 V - full load**



# 5 Conducted emission pre-compliance test

The limits indicated on both diagrams at 115 Vac and 230 Vac comply with EN55022 Class-B specifications. The values are measured in peak detection mode.

**Figure 12. CE at 115 Vac 50 Hz - line 1 peak detector**

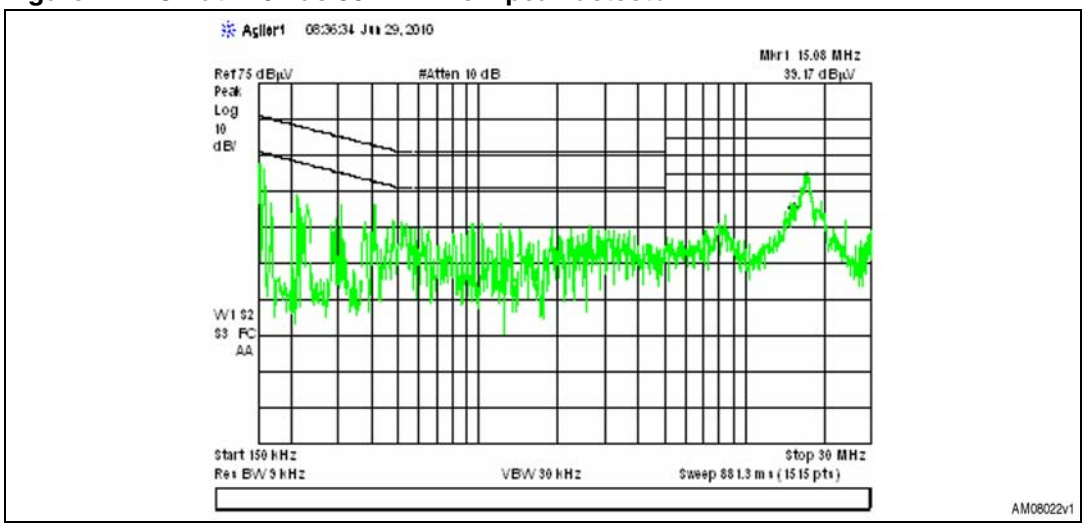



**Figure 13. CE at 115 Vac 50 Hz - line 2 peak detector**

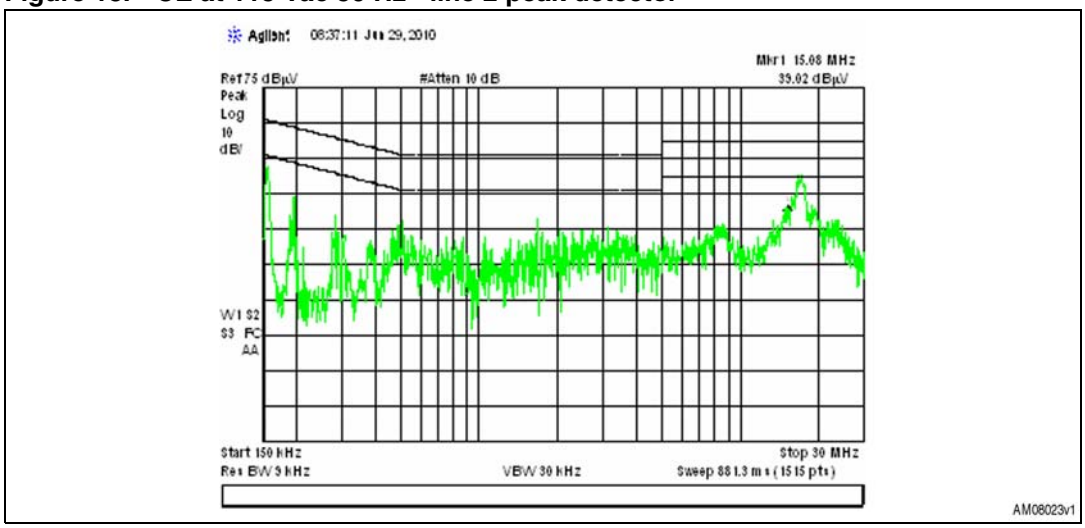


**Figure 14. CE at 230 Vac 50 Hz - line 1 peak detector**

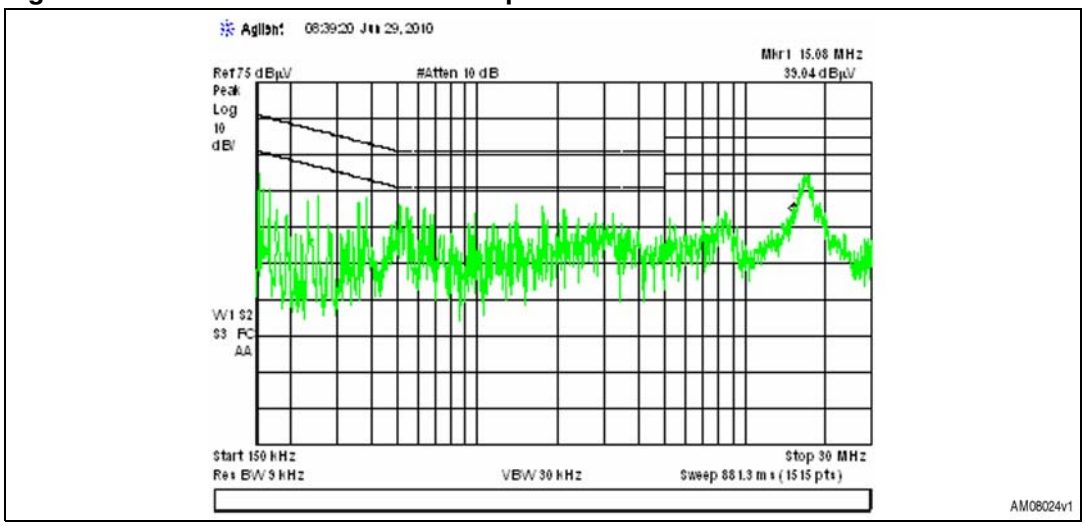
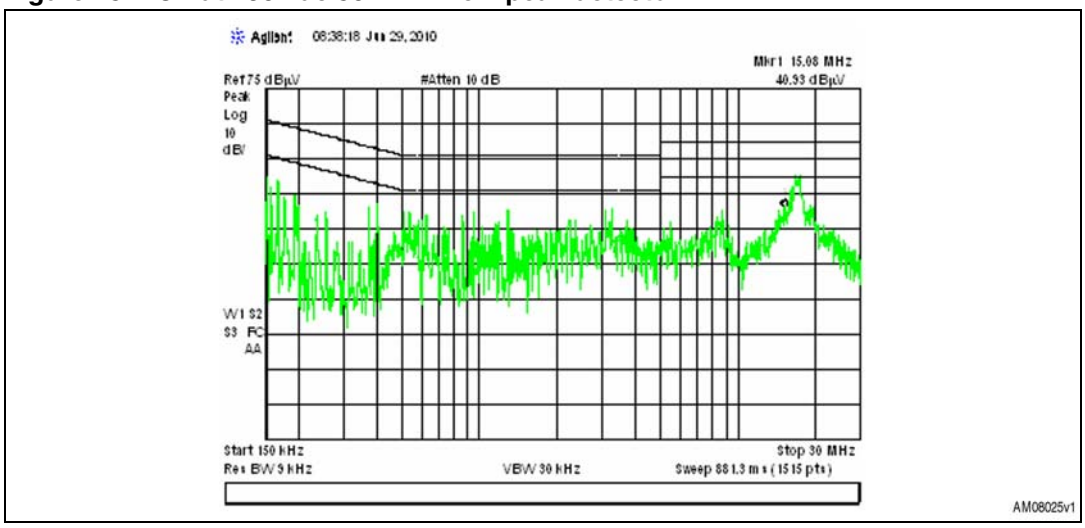



**Figure 15. CE at 230 Vac 50 Hz - line 2 peak detector**



# 6 BOM list

**Table 7. BOM list**

| Reference | Part / value | Technology information | Package | Manufacturer code |
|---|---|---|---|---|
| C1 | 68 µF 450 V | Electrolytic aluminium capacitor | TH Radial | EPCOS B43890A5686M000 |
| C3 | 470 nF 630 Vdc | Metallized polypropylene film capacitor | TH Radial | EPCOS B32653A6474K000 |
| C4 | 470 pF, 25 V | Ceramic capacitor COG, 5 % | SMD 0805 | |
| C5 | 47 nF, 25 V | Ceramic capacitor | SMD 0805 | |
| C6 | 1 µF, 25 V | Ceramic capacitor | SMD 0805 | |
| C7 | 10 nF, 25 V | Ceramic capacitor | SMD 0805 | |
| C8,C9 | 305 V X2, 470 nF, 10 % | Polypropylene | TH Radial | EPCOS B32922C3474K000 |
| C10 | 1 nF 250 V Y1 | Ceramic capacitor | TH Radial | |
| C11 | 100 nF 50 V | Ceramic capacitor | SMD 1206 | |
| C12 | 470 µF, 35 V | Electrolytic aluminium capacitor | TH Radial | |
| C13 | 470 µF, 35 V | Electrolytic aluminium capacitor | TH Radial | |
| C14 | 22 nF 630 V | Polypropylene | TH Radial | |
| C15 | 2.2n-Y1- 250 V | Ceramic capacitor | TH Radial | |
| C16 | 1 µF, 25 V | Ceramic capacitor | SMD 0805 | |
| C19 | 150 nF, 25 V | ceramic capacitor | SMD 0805 | |
| C20 | 100 µF 35 V | Electrolytic aluminium capacitor | TH Radial | |
| C21 | 220 nF, 25 V | ceramic capacitor | SMD 0805 | |

**Table 7. BOM list**

| Reference | Part / value | Technology information | Package | Manufacturer code |
|---|---|---|---|---|
| C22 | 470 µF 25 V | Electrolytic aluminium capacitor | TH radial | |
| D1 | 600 V, 3 A | Turbo 2 ultrafast high voltage rectifier | DO41 | STMicroelectronics STTH2L06 |
| D2+heatsink | 800 V, 4 A | Bridge | TH | GBU8K |
| D3,D4 +heatsink | 10 A, 60 V | Power schottky rectifier | TO-220 | STMicroelectronics STPS10L60FP |
| D6,D7,D8, D12, D13,D14 | 150 mA, 100 V | Schottky rectifier | Minimelf | STMicroelectronics TMMBAT46 |
| D15 | 12 V | Zener diode | Minimelf | |
| D16 | 15 V | Zener diode | Minimelf | |
| F1 | 3 A | Fuse | TH | |
| ISO1 | PC817 | Photo Coup | TH | |
| J1 | CON3 | Terminal pin distance 7.62 mm | TH | |
| J2 | CON2 | Terminal pin distance 5 mm | TH | |
| LC1 | 2x12 mH/1.8 A | Common choke | TH | TDK HF2826-123Y1R8-T01 |
| LPFC1 | 520 µH,1.4 A | PFC inductor | TH | Magnetica 1974.002 |
| Q1,Q2,Q3+ heatsink | STF12NM50N | MDMESH™ II MOSFET | TO220-FP | STMicroelectronics STF12NM50N |
| Q4 | STQ1HNK60R | SuperMESH™ MOSFET | TH | STMicroelectronics STQ1HNK60R |
| Q5,Q6 | BC847 | Small signal bipolar | SMD SOT 23 | |
| R1 | 1.2 MΩ, 1 %, 1/4 W | | SMD 1206 | |

**Table 7. BOM list**

| Reference | Part / value | Technology information | Package | Manufacturer code |
|---|---|---|---|---|
| R2 | 1.8 MΩ, 1 %, 1/4 W | | SMD 1206 | |
| R3,R5,R7 | 1 MΩ, 1 %, 1/4 W | | SMD1206 | |
| R4 | 330 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R6 | 2.2 MΩ, 1 %, 1/4 W | | SMD1206 | |
| R9 | 2.2 MΩ, 1 %, 1/8 W | | SMD 0805 | |
| R8 | 240 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R10 | Not mounted | | SMD 0805 | |
| R11 | 43 kΩ,1 %, 1/4 W | | SMD 0805 | |
| R12,R15 | 15 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R17 | 15 kΩ, 1 %, 1/4 W | | SMD 1206 | |
| R13 | 56 kΩ, 1 %, 1/4 W | | SMD 1206 | |
| R14 | 27 kΩ, 1 %, 1/4 W | | SMD 1206 | |
| R16,R18,R22 | 56 Ω, 1 %, 1/4 W | | SMD 1206 | |
| R19 | 360 kΩ, 1 %, 1/4 W | | SMD 1206 | |
| R20 | Not mounted | | TH, 1 W | |
| R21 | 0.180 Ω, 1 %, 1 W | | TH radial | |
| R23,R24 | 2.4 MΩ, 1 %, 1/4 W | | SMD 1206 | |
| R26 | Not mounted | | TH, 1 W | |
| R27 | 0.56 Ω, 1 %, 1 W | | TH Radial | |
| R28 | 10 kΩ, 5 %,1/4 W | | SMD 1206 | |
| R29 | 5.6 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R32 | 36 Ω,1 %, 1 W | | SMD 1206 | |
| R33 | 39 kΩ, 1 %,1/8 W | | SMD 0805 | |
| R34 | 47 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R35 | 6.2 kΩ, 1 %, 1/8 W | | SMD 0805 | |

**Table 7. BOM list**

| Reference | Part / value | Technology information | Package | Manufacturer code |
|---|---|---|---|---|
| R36 | 120 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R37,R38,R39, R44 | 0 Ω, 1/4 W, 5 % | | SMD 1206 | |
| R40 | 1 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R42 | 4.7 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R43 | 6.8 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| R46 | 150 kΩ, 1 %, 1/8 W | | SMD 0805 | |
| T1 | TRAFO | | TH | MAGNETICA<br>1860.0045 |
| U1 | L6585DE | | SMD SO20 | STMicroelectronics<br>L6585DE |
| U2 | TL431 | | TH TO92 | STMicroelectronics<br>TL431 |

# 7 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 31-Mar-2011 | 1 | Initial release. |