DEMO MANUAL DC040
High Speed A/D Demo Board

LTC1278 12-Bit 500ksps A/D Converter Demo Board

DESCRIPTION

The LTC1278 is a 1.6µs, 500ksps, sampling 12-bit A/D converter which draws only 75mW from a single 5V or ±5V supplies. The LTC1278 demo board provides the user with a way to evaluate the LTC1278 high speed A/D converter. In addition, the LTC1278 demo board is intended to illustrate the layout and bypassing techniques required to obtain optimum performance from this part. The LTC1278 demo board is designed to be easy to use and requires only ±7V to ±15V supplies, a conversion start signal and an analog input signal. As shown in the Board Photo, the LTC1278 is a very space efficient solution for A/D users. By combining a 12-bit A/D, sample-and-hold, reference and clock circuitry into a single SOIC package, all the data acquisition circuitry including the bypass caps can be placed into an area of only 0.43 square inches.

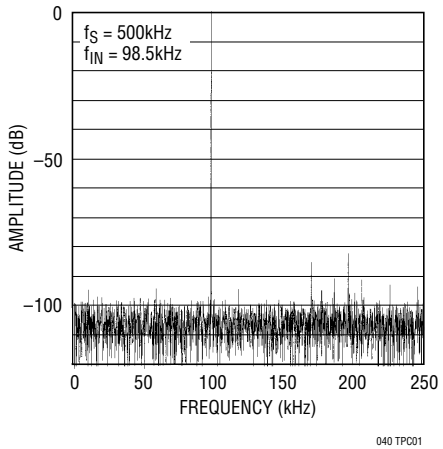
This manual shows how to use the demo board. Included are timing diagrams, power supply requirements and analog input range information. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout and bypass strategies used in this board is also included so that anyone designing a PC board using the LTC1278 will be able to get the maximum performance from the device.

FEATURES

- Proven 500ksps 12-Bit ADC Surface Mount Layout
- Actual ADC Footprint Only 0.43 Inch^2 Including Bypass Capacitors
- 72dB SINAD and 82dB THD at 100kHz Inputs
- Gerber Files for This Circuit Board Are Available. Call the LTC Factory.

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

4096 Point FFT of LTC1278 Demo Board



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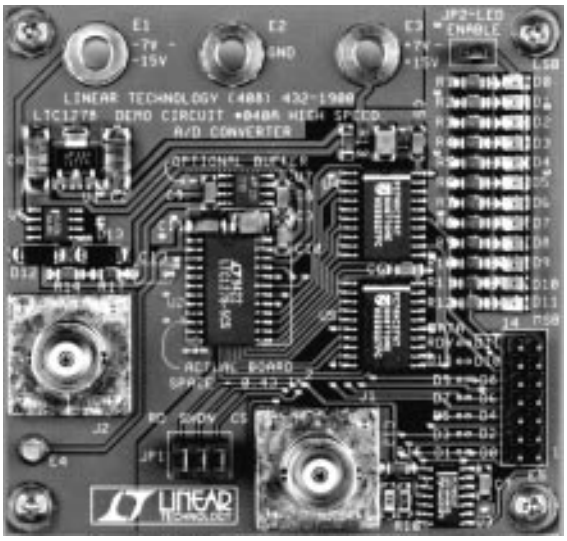
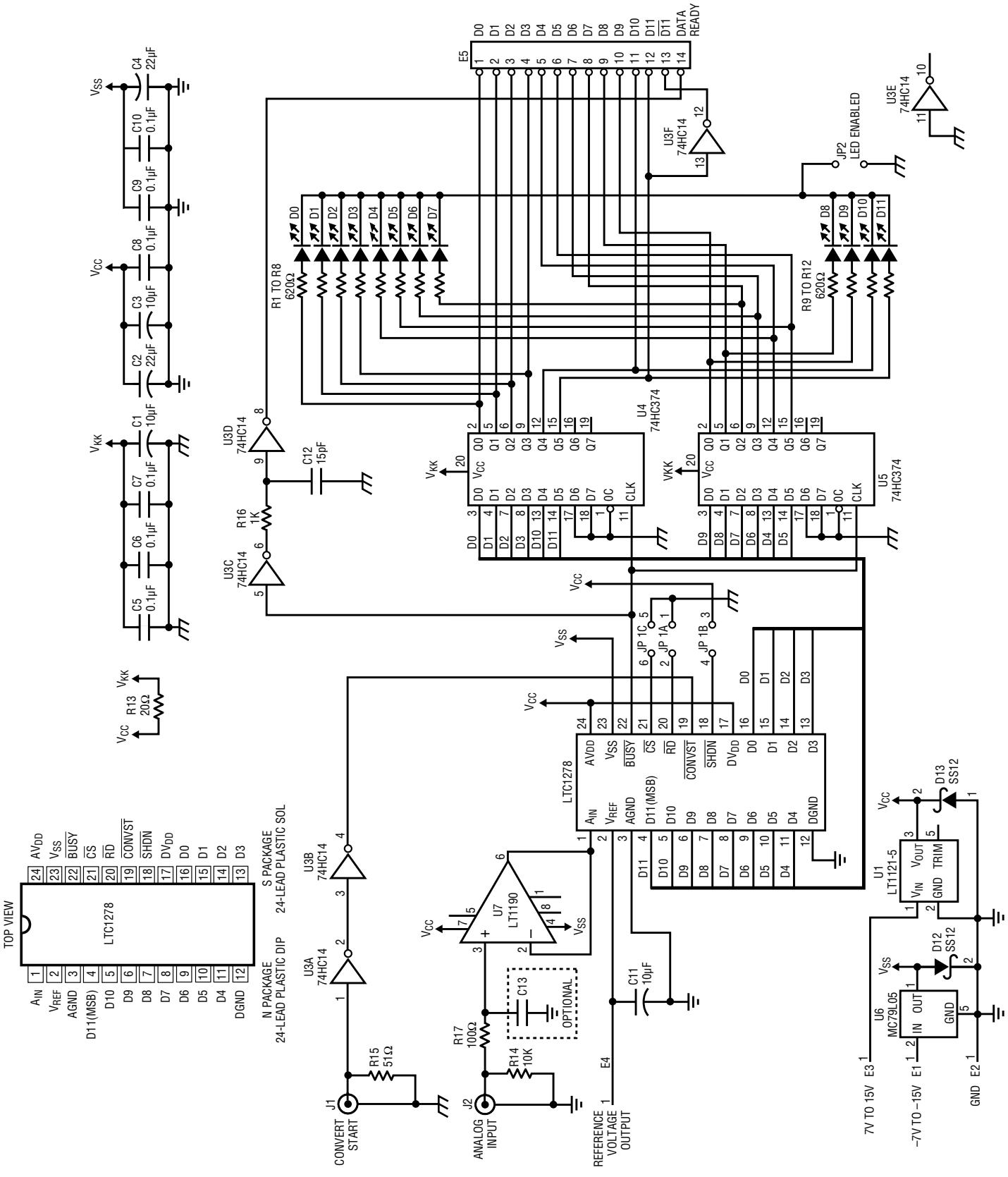


040 TPC02

Actual Size

SCHEMATIC DIAGRAM



PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C3	2	TAJB106M010	10µF 10V 20% Tantalum Capacitor	AVX	(803) 946-0690
C2, C4	2	TAJC226M010	22µF 10V 20% Tantalum Capacitor	AVX	(803) 946-0690
C5 to C10	6	VJ1206Y104KXAMT	0.1µF 50V 10% Chip Capacitor	Vitramon	(203) 268-6261
C11	1	TAJA106006	10µF 6V 20% Tantalum Capacitor	AVX	(803) 946-0690
C12	1	12062R150K9BB2	15pF 50V 10% Chip Capacitor	Philips	(407) 744-4200
D0 to D11	12	LN1251C	LED	Panasonic	(714) 373-7323
D12, D13	2	SS12	Schottky Diode	General Instrument	(516) 847-3222
E1 to E3	3	#575-4	Banana Jack	Keystone	(718) 956-0666
E4	1	#1502-2	Solder Post	Keystone	(718) 956-0666
E5	1	TSW-107-07-6-D	14-Pin Header	Samtec	(800) 726-8329
JP1	1	TSW-103-07-6-D	6-Pin Header	Samtec	(800) 726-8329
JP2	1	TSW-101-07-6-D	2-Pin Header	Samtec	(800) 726-8329
J1, J2	2	227699-3	BNC Female	AMP	(717) 564-0100
R1 to R12	12	CR32-621J-T	620Ω 1/8W 5% Resistor	AVX	(803) 448-9411
R13	1	CR32-200J-T	20Ω 1/8W 5% Resistor	AVX	(803) 448-9411
R14	1	CR32-103J-T	10KΩ 1/8W 5% Resistor	AVX	(803) 448-9411
R15	1	9C12063A651ROFL	51Ω 1/4W 5% Resistor	Philips	(817) 325-7871
R16	1	CR32-102J-T	1KΩ 1/8W 5% Resistor	AVX	(803) 448-9411
R17	1	CR32-101J-T	100Ω 1/8W 5% Resistor	AVX	(803) 448-9411
U1	1	LT1121CST-5	5V Regulator	LTC	(408) 432-1900
U2	1	LTC1278S	12-Bit ADC	LTC	(408) 432-1900
U3	1	74HC14	Inverter	Philips	(408) 991-2000
U4, U5	2	74HC374	Latch	Harris	(800) 442-7747
U6	1	MC79L05ACD	–5V Regulator	Motorola	(602) 244-3576
U7	1	LT1190CS8	Op Amp	LTC	(408) 432-1900
	4	SNT-100-BK-T	Shunt	Samtek	(800) 726-8329
	4		Screw 4 × 40-3/8		
	4	HTSP-3	Standoff	Micro Plastic	(501) 453-8861

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply ±7V to ±15V at 200mA to the banana jacks (E1 to E3). Be careful to observe the correct polarity. Internal regulators provide ±5V to the LTC1278. A LT1121-5 regulator provides 5V for analog and digital circuitry while –5V is provided for the A/D and buffer by the MC79L05 regulator.

The Analog Input

Analog signals are applied to the LTC1278 demo board using BNC Connector J2. The analog signal input range is ±2.5V. Optimum performance is achieved using a signal source that has low output impedance, is low noise and has low distortion. Signal generators, such as the B&K Type 1051 Sine Generator, give excellent results. Further, this generator can be configured to operate referenced to a master clock signal as shown in Figure 1. If this or other low noise generators are not available, the LTC1278 demo

OPERATION

board has an optional capacitor, C13. Installing C13 creates a lowpass filter that reduces signal-source noise.

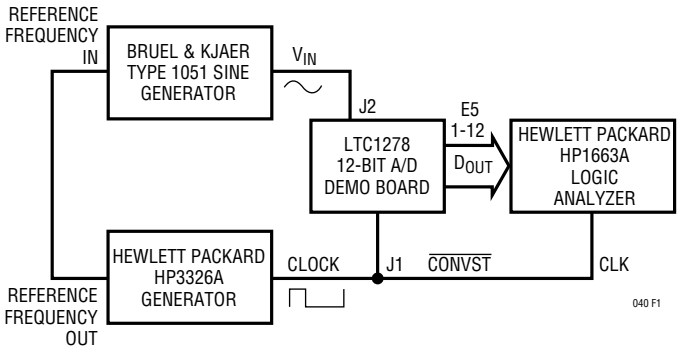


Figure 1. Typical Setup for LTC1278 Demo Board

The LT1190 buffer (U7) provides the LTC1278 with a fast settling, low impedance signal that allows the A/D input voltage to completely settle before starting a conversion. This buffer is optional and is provided only as an example of how to drive the LTC1278. The unbuffered performance of the LTC1278 is very good but can only be accurately evaluated by removing the buffer and shorting across pins 2 and 3 of U7 on the board.

Applying the Conversion Start Signal

A conversion is initiated by a falling edge on the $\overline{\text{CONVST}}$ input (BNC J1). The $\overline{\text{CONVST}}$ input uses TTL or CMOS levels. $\overline{\text{CONVST}}$ should remain low as shown in Figure 2 until the conversion is completed or it should be returned high within 120ns of the negative going edge as shown in Figure 3. During a conversion, transition of the $\overline{\text{CONVST}}$ input can result in errors in the D_{OUT} word.

Reading the Output Data

The ADC data outputs are buffered by the two 74HC374 latches and are available on connector E5. The latches are used to drive the LEDs and connector. In a practical circuit, latches are not required unless the ADC is to be tied to a noisy data bus. (Refer to the LTC1278 data sheet for details on different digital interface modes.)

The LTC1278 output data is in two's complement format. The data can be converted to offset binary by using $\overline{\text{D11}}$ instead of D11. Offset binary is used when an FFT is to be performed on the sampled data. A Data Ready line (E5 pin 14) is provided to latch the D_{OUT} word. D_{OUT} is valid on the rising edge of Data Ready. A ground line is not provided on the connector and must be added if the receiving system is not otherwise grounded to the board.

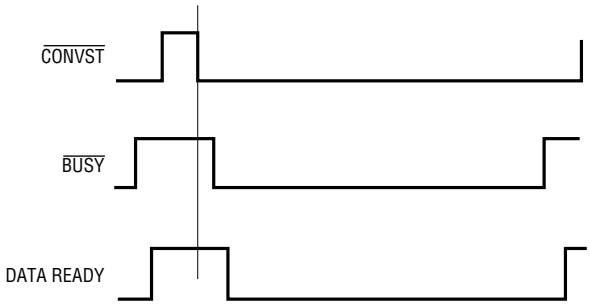


Figure 2. Timing Diagram

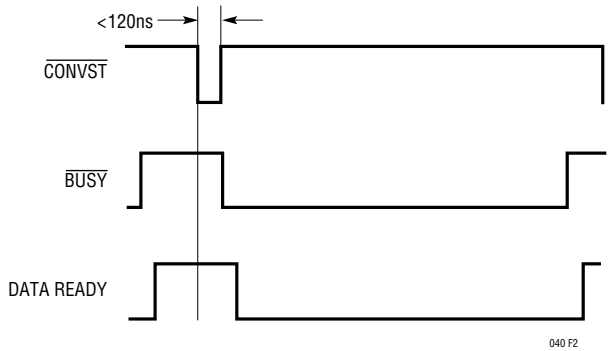


Figure 3. Alternative Timing Diagram

The LTC1278 D_{OUT} word can be acquired with a logic analyzer. Conversion data can be stored on a disk and easily transferred to a PC by using a logic analyzer that has a PC-compatible floppy drive (such as an HP1663A). Once the data is transfered to a PC, programs such as MathCAD or Excel can be used to calculate FFTs. The FFTs can be used to obtain LTC1278 AC specifications such as signal-to-noise ratio and total harmonic distortion.

LEDs D0 to D11 provide a visual display of the LTC1278 digital output word. D0 is the LSB and D11 is the MSB. Jumper JP2 can be removed to disable the LEDs reducing supply consumption by up to 36mA.

Driving $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{SHDN}}$ Pins

Jumpers for $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{SHDN}}$ (JP1A to JP1C) are shorted for normal operation. The jumpers can be removed and these lines externally driven if desired. See the LTC1278 data sheet for details on driving these lines.

OPERATION

LAYOUT

The use of separate analog and digital ground planes is a good practice for a well designed PC board using the LTC1278. The proper way to make the analog and digital ground planes can be seen by examining the solder side of the PCB layout. The two ground planes are completely isolated except for one connection near the top of the board. The two ground planes follow the same path on the component and solder sides of the board to reduce coupling between the ground planes. Further, any trace that opens a portion of the ground plane may reduce the ground plane's efficiency. Therefore, ensure that the ground plane's solderside has a limited number of plane-breaking traces within it. The analog and digital traces do not cross each other (whether on the board's top or bottom side) or run adjacent to each other. Both analog and digital ground pins (pin 3 and pin 10) of the LTC1278 are tied directly to the Analog Ground Plane. This produces the lowest noise condition.

BYPASS

It is important that the supply and reference bypass capacitors for the LTC1278 be placed as close as possible to the supply and reference pins. The ground side of the capacitors should have very short paths to analog ground. The AV_{DD} and V_{REF} pins should be bypassed with high quality (low ESR) tantalum capacitors of at least 10µF. V_{SS} is less critical and should be bypassed with a ceramic capacitor of at least 0.1µF. DV_{DD} does not require a separate bypass capacitor and it should be tied directly to the AV_{DD} pin.

Table 1.

JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1A	$\overline{RD}$	Shorted for normal operation. If open, the $\overline{RD}$ line can be driven externally to control whether the D_{OUT} lines are active or high impedance.
JP1B	$\overline{SHDN}$	Shorted for normal operation. If open, the $\overline{SHDN}$ line can be driven externally to put the LTC1278 into the shutdown mode.
JP1C	$\overline{CS}$	Shorted for normal operation. If open, the $\overline{CS}$ line can be driven externally to select or deselect the LTC1278.
JP2	LED Enable	Shorted to enable LEDs. Open to disable the LEDs.

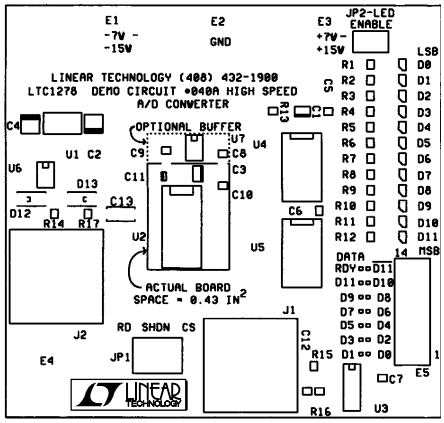
Table 2.

INPUT/OUTPUT PIN	FUNCTION
J1	Conversion Start 0V to 5V
J2	Analog Input ±2.5V
E1	–7V to –15V at 100mA
E2	Ground
E3	7V to 15V at 200mA
E4	V_{REF} Output (2.42V Typical)
E5-1	$D_{OUT}0$ (LSB)
E5-2	D_{OUT1}
E5-3	D_{OUT2}
E5-4	D_{OUT3}

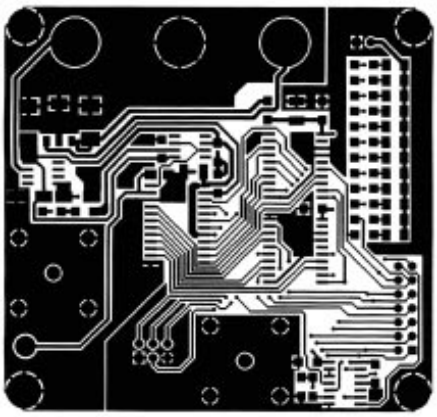
INPUT/OUTPUT PIN	FUNCTION
E5-5	D_{OUT4}
E5-6	D_{OUT5}
E5-7	D_{OUT6}
E5-8	D_{OUT7}
E5-9	D_{OUT8}
E5-10	D_{OUT9}
E5-11	D_{OUT10}
E5-12	D_{OUT11} (MSB)
E5-13	D_{OUT11} Inverted
E5-14	Data Ready*

* Can be used by an external system to latch the ADC's output. Latch data on the rising edge.

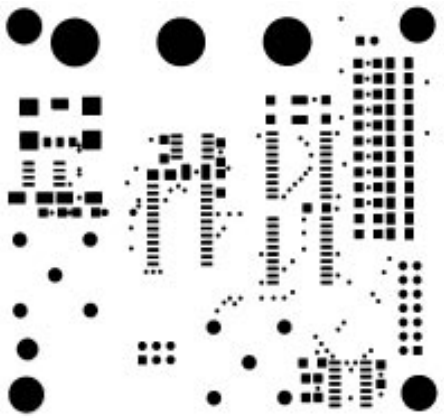
PCB LAYOUT AND FILM



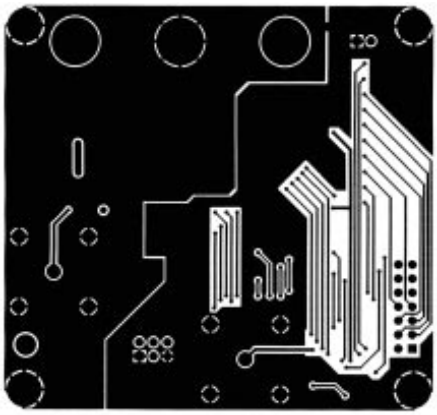
Component Side Silkscreen



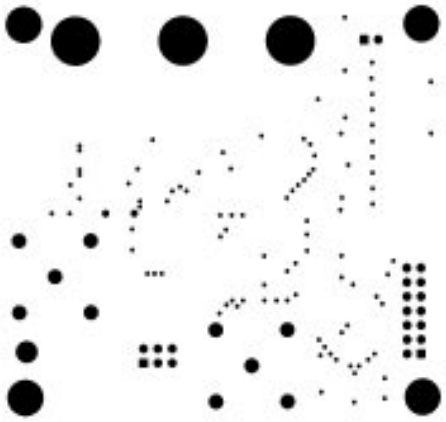
Component Side



Component Side Solder Mask

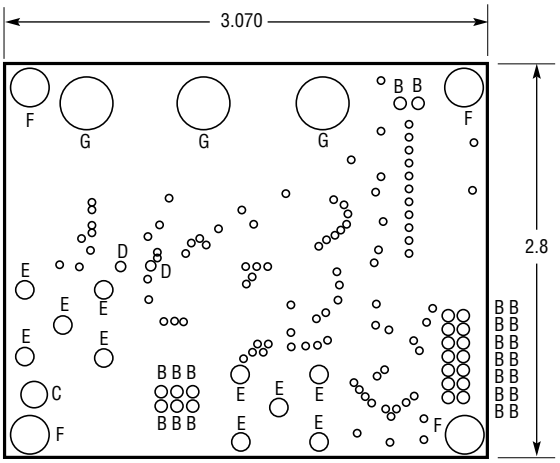


Solder Side



Solder Side Solder Mask

PC FAB DRAWING



SYMBOL	DIAMETER	# OF HOLES
A	0.125	3 (TOOLING)
B	0.040	264
C	0.094	30
D	0.030	24
E	0.045	120
F	0.120	48
G	0.210	36
UNMARKED	0.018	1236
	TOTAL HOLES	1761

NOTES:
1. MATERIAL IS FR4, .062″ THICK WITH 2 OUNCE COPPER.
2. PCB WILL BE DOUBLE-SIDED WITH PLATED THROUGH HOLES.
3. HOLE SIZES ARE AFTER PLATING. PLATED THROUGH HOLE WALL THICKNESS MINIMUM .0014″(1OZ.).
4. USE PADMASTER PROCESS.
5. SOLDER MASK BOTH SIDES WITH PC401 USING FILM PROVIDED.
6. SILKSCREEN COMPONENT SIDE USING FILM PROVIDED.
7. ALL DIMENSIONS ARE IN INCHES.
8. ALL PANELS IN ORDER MUST BE THE SAME.
9. DO NOT PLATE TOOLING HOLES - 0.125.
10. DO NOT PLATE SCORING HOLES - 0.094, (18 HOLES AT PANEL EDGE).
11. SCORE PANELS AFTER MANUFACTURING - 0.020 BOTH SIDES.
12. ONLY ONE IMAGE SHOWN FOR DRAWING SIMPLICITY.

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