



SANYO Semiconductors

DATA SHEET

LV5747TT — Bi-CMOS LSI 1-channel Step-down Switching Regulator

Overview

The LV5747TT is a 1-channel step-down switching regulator.

Functions

- 1 channel step-down switching regulator controller.
- Frequency decrease function at pendent.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	V_{IN} max		45	V
Allowable pin voltage	V_{IN} , SW		45	V
	HDRV, CBOOT		52	V
	LDRV		6.0	V
	Between CBOOT to SW, Between CBOOT to HDRV		6.0	V
	EN, ILIM		$V_{IN}+0.3$	V
	Between V_{IN} to ILIM		1.0	V
	V_{DD}		6.0	V
	SS, FB, COMP		$V_{DD}+0.3$	V
Allowable Power dissipation	P_d max	Mounted on a specified board. *	0.75	W
Junction temperature	T_j max		150	$^\circ\text{C}$
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Specified board: 35mm × 32mm × 1.6mm, glass epoxy 2-layer board.

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LV5747TT

Recommended Operating Ranges at $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{IN}		8.0 to 42	V
Error amplifier input voltage	V_{FB}		0 to 1.6	V

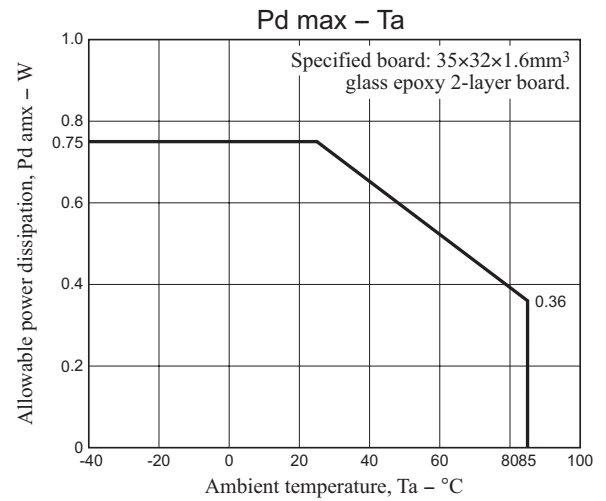
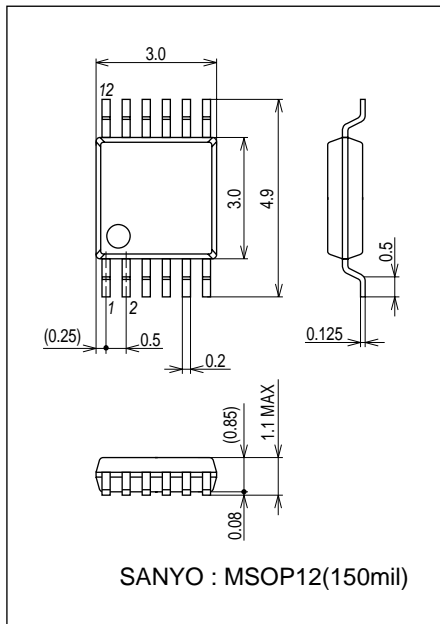
Electrical Characteristics at $T_a = 25^{\circ}\text{C}$, $V_{\text{IN}} = 24\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	Vref	Including offset of E/A	0.698	0.708	0.718	V
5V power supply	VDD	IOUT = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	FOSC		335	385	435	kHz
Frequency variation	FOSC DV	VIN = 8 to 42V		1		%
Oscillation frequency fold back detection voltage	VOSC FB	FB voltage detection after SS ends		0.5		V
Oscillatory frequency after fold back	FOSC FB	VFB = 0V	25	45	60	kHz
ON/OFF circuit block						
IC start-up voltage	VEN on	VIN = 8 to 42V		3.4	4.3	V
start-up voltage hysteresis	VEN hys		1.0	1.2		V
Soft start circuit block						
Soft start source current	ISS SC	EN > 4.3V	4	5	6	μA
Soft start sink current	ISS SK	EN < 1V, VDD = 5V		2		mA
Soft start end voltage	VSS END		0.9	1.1	1.3	V
UVLO circuit block						
UVLO lock release voltage	VUVLO		7.0	7.4	7.8	V
UVLO hysteresis	VUVLO H			0.6		V
Error amplifier						
Input bias current	IEA IN				100	nA
Error amplifier gain	GEA		1000	1400	1800	μA/V
Common mode input range	VEA R	VIN = 8 to 42V	0.0		1.6	V
Sink output current	IEA OSK	FB = 1.0V		-100		μA
Source output current	IEA OSC	FB = 0V		100		μA
Current detection amplifier gain	GISNS			1.3		
over current limiter circuit block						
Reference current	ILIM		-10%	20	+10%	μA
Over current detection comparator offset voltage	VLIM OFS		-5		+5	mV
Over current detection comparator common mode input range			VIN-0.45		VIN	V
PWM comparator						
Input threshold voltage	Vt max	Duty cycle = DMAX, SW = VIN	1.0	1.1	1.2	V
	Vt0	Duty cycle = 0%, SW = VIN	0.4	0.5	0.6	V
Maximum ON duty	DMAX		85	90	95	%
Output block						
Output stage ON resistance (the upper side)	RONH			5		Ω
Output stage ON resistance (the under side)	RONL			5		Ω
Output stage ON current (the upper side)	IONH		240			mA
Output stage ON current (the under side)	IONL		240			mA
The whole device						
Standby current	ICCS	EN < 1V			60	μA
Mean consumption current	ICCA	EN > 4.3V		3.3		mA

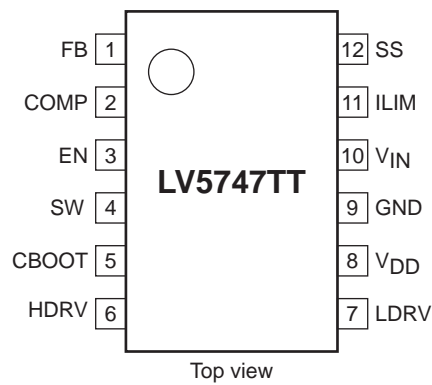
Package Dimensions

unit : mm (typ)

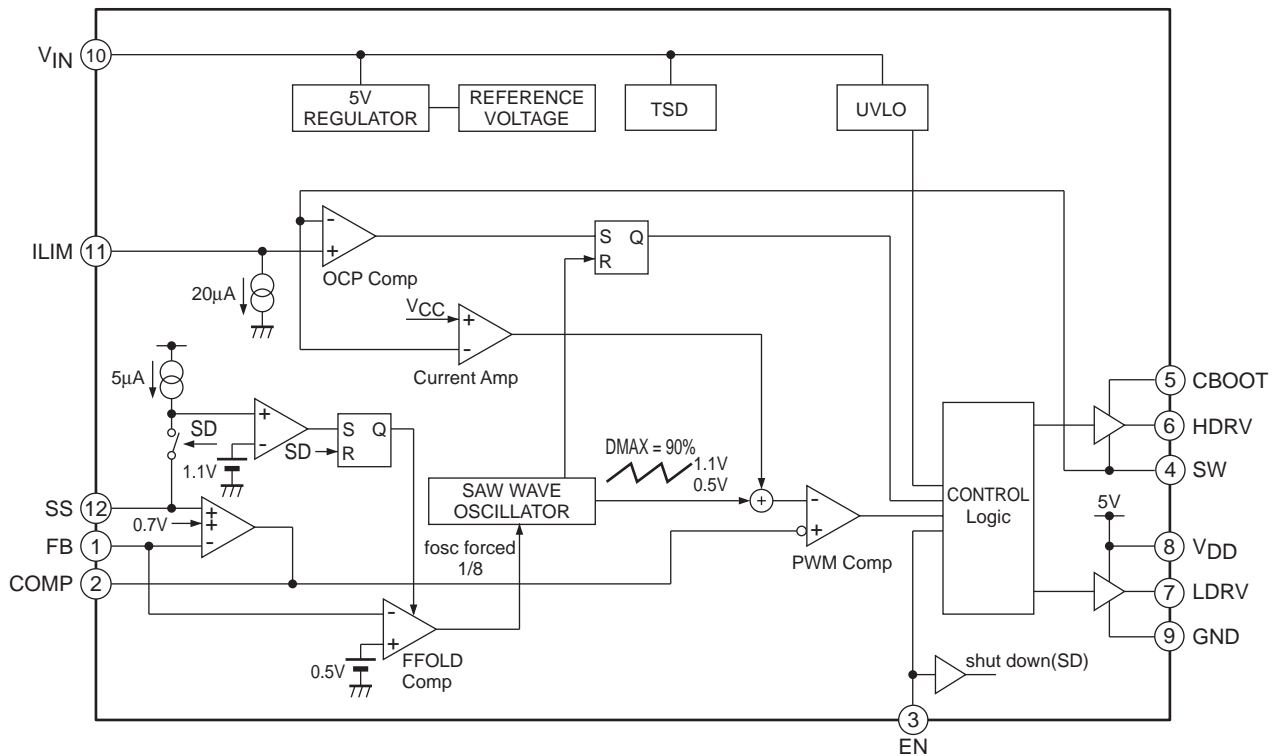
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Pin Assignment

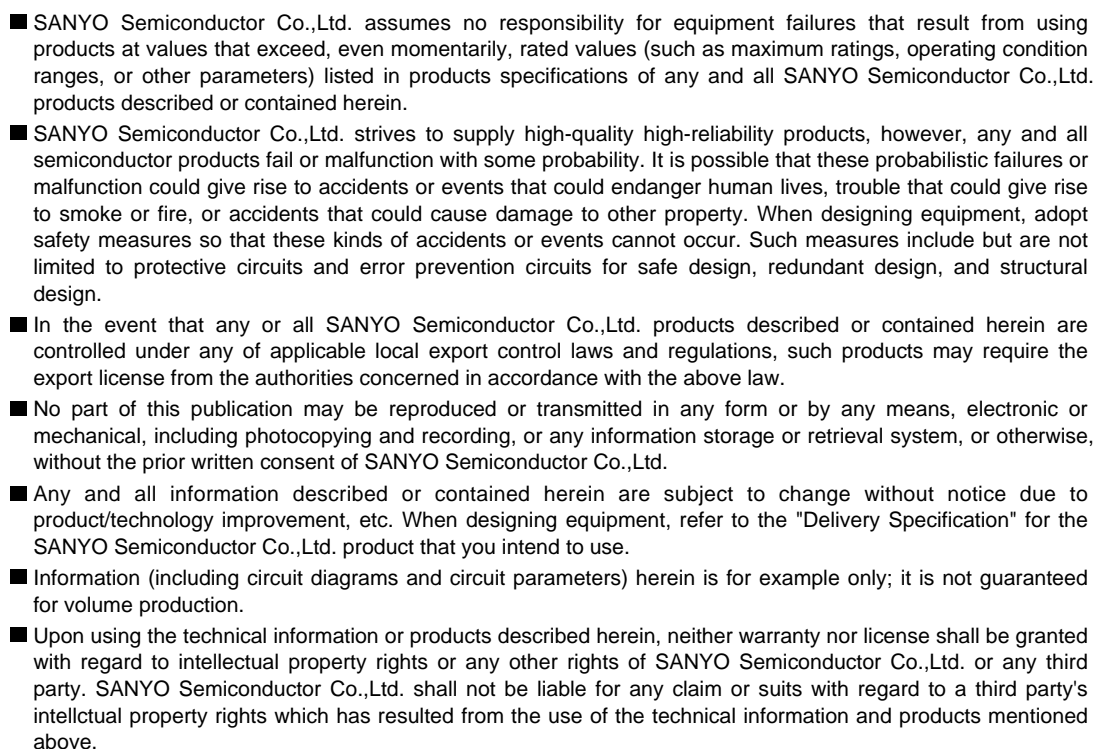


Block Diagram



Pin Function

Pin No.	Pin name	Description
1	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.708V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Moreover, when this pin voltage becomes 0.5V or less after a soft start ends, the frequency fold back function operations, and the oscillating frequency is falling with the FB voltage.
2	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.
3	EN	ON/OFF pin.
4	SW	Pin to connect with switching node. The source of NchMOSFET connects to this pin.
5	CBOOT	Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external NchMOSFET. Connect a bypath capacitor between CBOOT and SW.
6	HDRV	An external the upper MOSFET gate drive pin.
7	LDRV	An external the lower MOSFET gate drive pin.
8	VDD	Power supply pin for an external the lower MOS-FET gate drive.
9	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.
10	V_{IN}	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 7.8V or more by UVLO function, The IC starts and the soft start function operates.
11	ILIM	Reference current pin for current detection. The sink current of about 20μA flows to this pin. When a resistance is connected between this pin and V_{IN} outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper NchMOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWM pulse.
12	SS	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 5μA. This pin ends the soft start period by using the voltage of about 1.1V and the frequency fold back function becomes active.



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