

SANYO Semiconductors DATA SHEET

LV5747TT — 1-channel Step-down Switching Regulator

Overview

The LV5747TT is a 1-channel step-down switching regulator.

Functions

- 1 channel step-down switching regulator controller.
- Frequency decrease function at pendent.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
supply voltage		V _{IN} max		45	V
pin voltage	V _{IN} , SW			45	V
	HDRV, CBOOT			52	V
	LDRV			6.0	V
	Between CBOOT to SW, Between CBOOT to HDRV			6.0	V
able	EN, ILIM			V _{IN} +0.3	V
Allowable	Between V _{IN} to ILIM			1.0	V
	V_{DD}			6.0	V
	SS, FB, COMP			V _{DD} +0.3	V
Allowable Power dissipation		Pd max	Mounted on a specified board. *	0.75	W
Junction temperature		Tj max		150	°C
Operating temperature		Topr		-40 to +85	°C
Storage temperature		Tstg		-55 to +150	°C

^{*} Specified board: 35mm x 32mm x 1.6mm, glass epoxy 2-layer board.

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LV5747TT

Recommended Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage range	V _{IN}		8.0 to 42	V	
Error amplifier input voltage	V _{FB}		0 to 1.6	V	

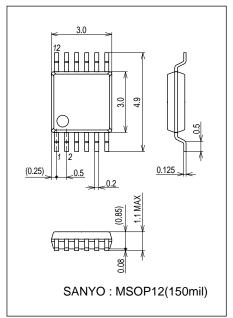
Electrical Characteristics at Ta = 25°C, $V_{\mbox{\footnotesize{IN}}} = 24V$

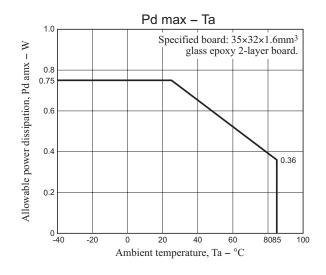
				Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Reference voltage block			· · · · · · · · · · · · · · · · · · ·			
Internal reference voltage	Vref	Including offset of E/A	0.698	0.708	0.718	V
5V power supply	V _{DD}	I _{OUT} = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator blo		,	L	l l		
Oscillation frequency	Fosc		335	385	435	kHz
Frequency variation	FOSC DV	V _{IN} = 8 to 42V		1		%
Oscillation frequency fold back	VOSC FB	FB voltage detection after SS ends		0.5		V
detection voltage	03016					
Oscillatory frequency after fold back	FOSC FB	V _{FB} = 0V	25	45	60	kHz
ON/OFF circuit block	•				'	
IC start-up voltage	V _{EN} on	V _{IN} = 8 to 42V		3.4	4.3	V
start-up voltage hysteresis	V _{EN} hys		1.0	1.2		V
Soft start circuit block		1	L	II.		
Soft start source current	I _{SS} SC	EN > 4.3V	4	5	6	μА
Soft start sink current	I _{SS} SK	EN < 1V, V _{DD} = 5V	·	2	-	mA
Soft start end voltage	V _{SS} END		0.9	1.1	1.3	V
UVLO circuit block	1 ,99 -145	1	0.0	1.1	1.0	v
UVLO lock release voltage	V. n. n. o		7.0	7.4	7.8	V
	VUVLO		7.0		7.0	V
UVLO hysteresis	VUVLO H			0.6		V
Error amplifier	Ι.	T	- 		400	
Input bias current	IEA IN				100	nA
Error amplifier gain	G _{EA}		1000	1400	1800	μA/V
Common mode input range	V _{EA} R	V _{IN} = 8 to 42V	0.0		1.6	V
Sink output current	IEA OSK	FB = 1.0V		-100		μΑ
Source output current	IEA OSC	FB = 0V		100		μΑ
Current detection amplifier gain	GISNS			1.3		
over current limiter circuit block						
Reference current	l _{LIM}		-10%	20	+10%	μΑ
Over current detection comparator	V _{LIM} OFS		-5		+5	mV
offset voltage						
Over current detection comparator			V _{IN} -0.45		v_{IN}	V
common mode input range PWM comparator	1	1				
	\/t may	Duty cycle = DMAX, SW = V _{IN}	10	4.4	1.2	V
Input threshold voltage	Vt max	, ,	1.0	1.1		
Mayimum ON district	Vt0	Duty cycle = 0%, SW = V _{IN}	0.4	0.5	0.6	V
Maximum ON duty	DMAX		85	90	95	%
Output block	T _	1		Т	1	
Output stage ON resistance (the upper side)	RONH			5		Ω
Output stage ON resistance (the under side)	R _{ONL}			5		Ω
Output stage ON current (the upper side)	IONH		240			mA
Output stage ON current (the under side)	IONL		240			mA
The whole device	<u> </u>	I.	1			
Standby current	loco	EN < 1V	<u> </u>		60	μА
	Iccs	EN > 4.3V		3.3	00	mA
Mean consumption current	ICCA	LIV > 4.JV		3.3		ША

Package Dimensions

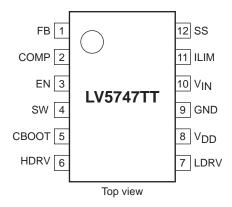
unit: mm (typ)

3375

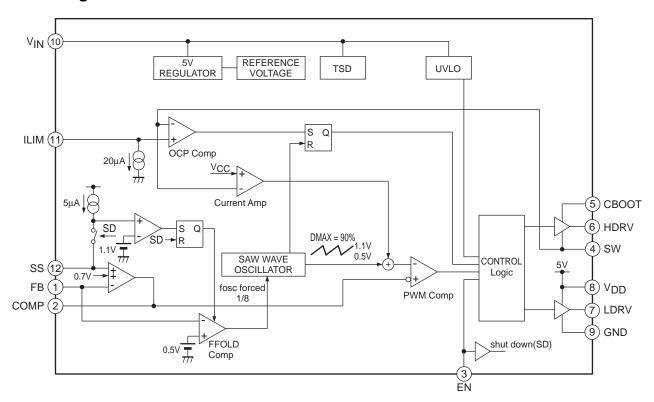




Pin Assignment



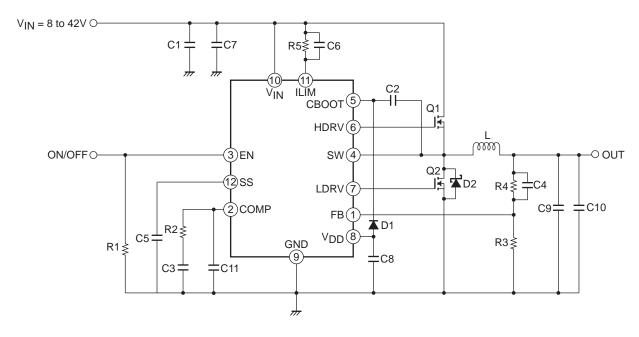
Block Diagram



Pin Function

Pin No.	Pin name	Description
1	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.708V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Moreover, when this pin voltage becomes 0.5V or less after a soft start ends, the frequency fold back function operations, and the oscillating frequency is falling with the FB voltage.
2	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.
3	EN	ON/OFF pin.
4	SW	Pin to connect with switching node. The source of NchMOSFET connects to this pin.
5	CBOOT	Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external NchMOSFET. Connect a bypath capacitor between CBOOT and SW.
6	HDRV	An external the upper MOSFET gate drive pin.
7	LDRV	An external the lower MOSFET gate drive pin.
8	V _{DD}	Power supply pin for an external the lower MOS-FET gate drive.
9	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.
10	V _{IN}	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 7.8V or more by UVLO function, The IC starts and the soft start function operates.
11	ILIM	Reference current pin for current detection. The sink current of about 20µA flows to this pin. When a resistance is connected between this pin and V _{IN} outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper NchMOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWM pulse.
12	SS	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 5µA. This pin ends the soft start period by using the voltage of about 1.1V and the frequency fold back function becomes active.

Sample Application Circuit



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