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Evaluation Board for Fractional-N PLL Frequency Synthesizer

FEATURES

Self-contained board, including
- **Synthesizer**
- **VCO**
- **10 MHz TCXO for reference frequency**
- **Loop filter (5.8 GHz)**

Designed for
- **10 MHz PFD frequency**
- **200 kHz channel spacing**
- **Minimum charge pump current**
- **20 kHz loop bandwidth**

Accompanying software allows complete control of synthesizer function from a PC

Battery operated: choice of 3 V or 5 V supply

Typical phase noise performance of −85 dBc/Hz at 1 kHz offset from a 5.8 GHz carrier

GENERAL DESCRIPTION

This board allows the user to evaluate the performance of the ADF4156 frequency synthesizer for PLLs (phase-locked loops).

A block diagram of the evaluation board is shown in Figure 1. It contains the ADF4156 synthesizer, a PC connector, and SMA connectors for the power supplies and RF output. There is also a low-pass loop filter (20 kHz) and a VCO (Z-COMM V940ME03-LF 5.8 GHz) on board.

The evaluation board is set up for a 10 MHz PFD comparison frequency. An on-board TCXO provides the 10 MHz reference frequency. A cable is included with the board to connect to a PC printer port.

The package also contains Windows® software to allow easy programming of the synthesizer.

FUNCTIONAL BLOCK DIAGRAM

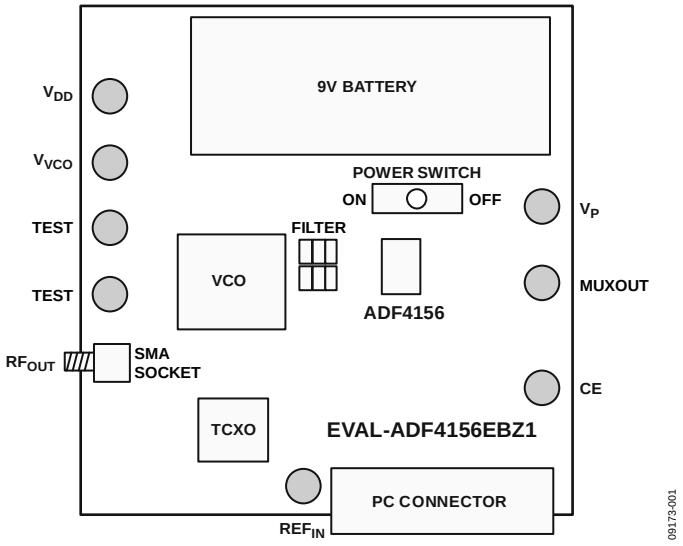

Figure 1.

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REVISION HISTORY

6/11—Rev. 0 to Rev. A

Document Title, Format, and Content Changed from EVAL-ADF4156, Revision 0, to UG-171, Rev. A ..... Universal

5/07—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The evaluation board comes with a cable for connecting to the printer port of a PC (see Figure 2 for a PC cable diagram and Figure 4 for a test setup configuration).

The evaluation board schematics are shown in Figure 6 and Figure 7.

POWER SUPPLIES

The board is powered from a single 9 V battery. The power cupply circuitry allows the user to choose 3 V for the ADF4156 V_{DD} and either 3 V or 5 V for the ADF4156 V_P and VCO supply. The default settings are 3 V for the ADF4156 V_{DD} and 5 V for the ADF4156 V_P and the VCO supply.

It is important to note that the ADF4156 V_{DD} should never exceed the ADF4156 V_P. This can cause damage to the device. If desired, external power supplies can be used. In this case, the user must insert SMA connectors as shown in Figure 3 and in the block diagram (see Figure 1).

LOCAL OSCILLATOR COMPONENTS

The 10 MHz TCXO provides the reference frequency. The on-chip R divider should be set to 1 so that the PFD frequency is also 10 MHz. The PLL is made up of the 10 MHz TCXO, the ADF4156, a passive loop filter (20 kHz bandwidth), and the V940ME03-LF VCO from Z-Communications, Inc. The output is available at RF_{OUT} through a standard SMA connector.

The on-board loop filter has been designed for a charge pump current of 0.3125 mA. ADIsimPLL™ can be used to design other loop filters.

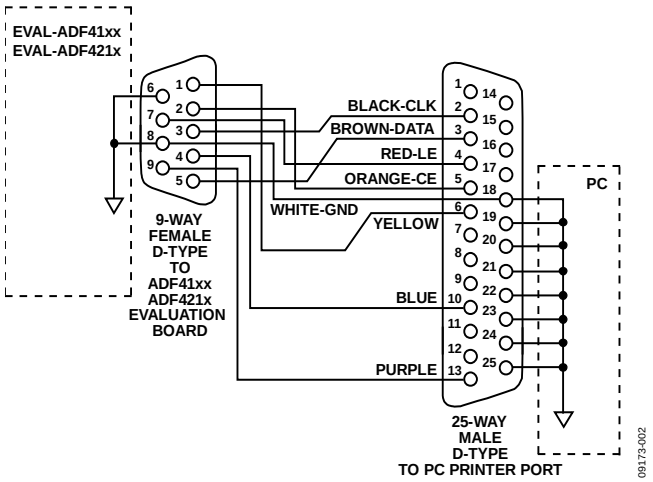

Figure 2. PC Cable Diagram

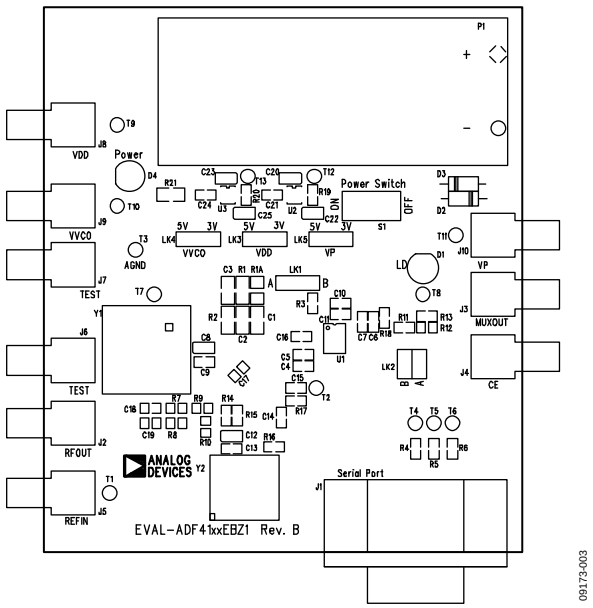

Figure 3. Evaluation Board Silkscreen

TEST SETUP

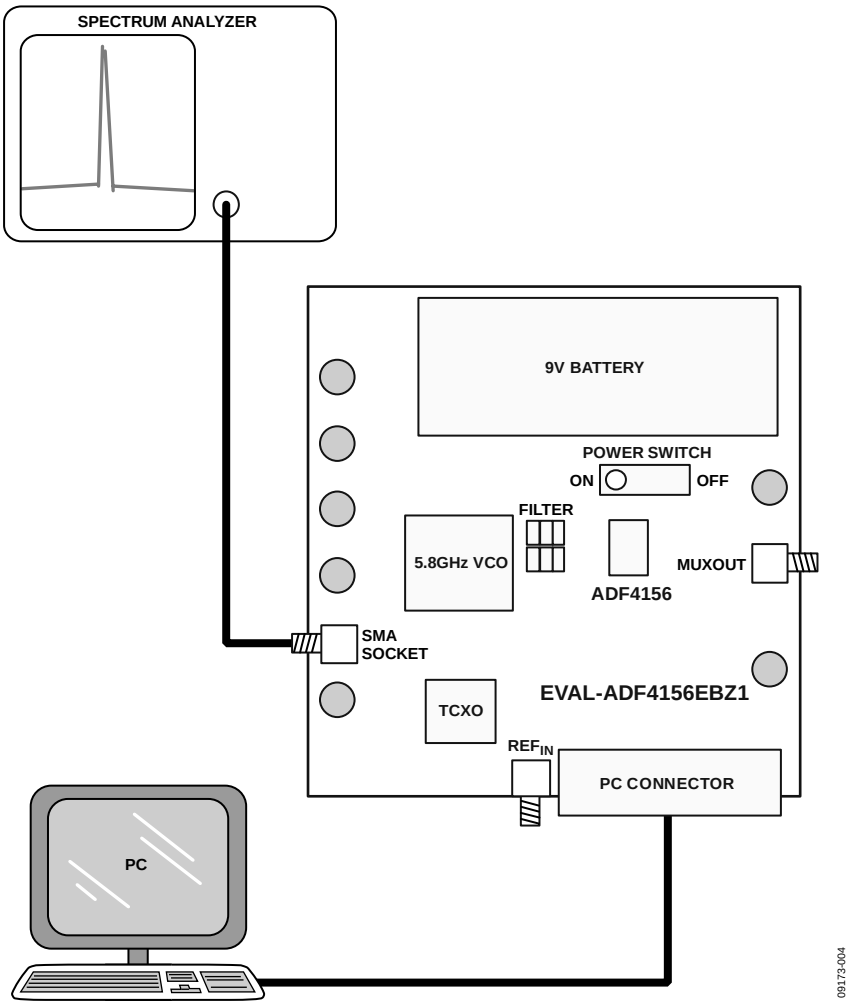

Figure 4. Test Setup

EVALUATION BOARD SOFTWARE

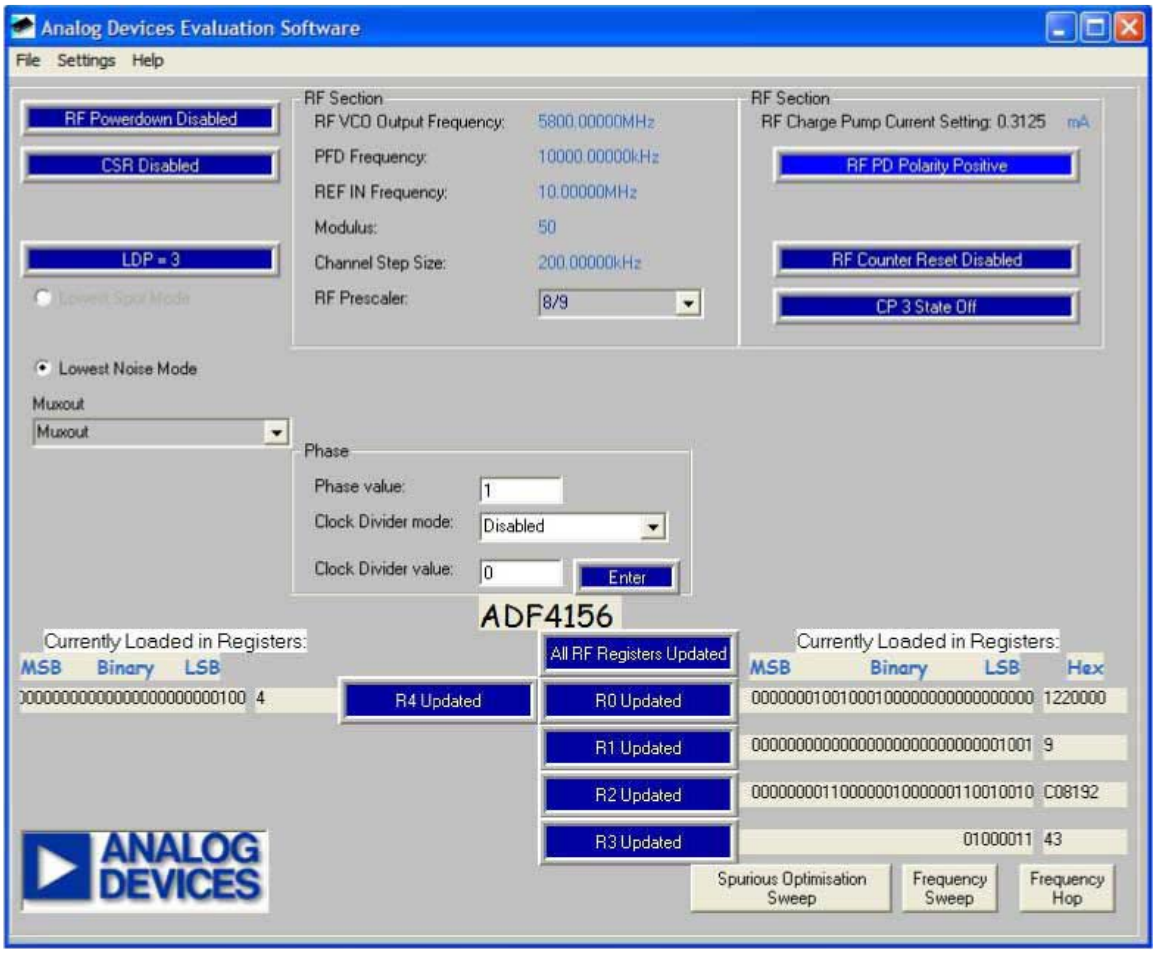

Figure 5. Evaluation Software, Main Window

SOFTWARE INSTALLATION AND SETUP

The evaluation board software is provided on the CD that accompanies the board. To install the software,

1. Click the **setup.exe** file.
2. Follow the on-screen instructions. The software is installed in a default directory called **C:/Program Files/Analog Devices/ADF4x5x**.
3. To run the software, click **ADF_Frac_Rev2_7.exe**.
4. Before the main window appears (see Figure 5), the device window opens, prompting you to choose the device to evaluate.
5. Select **ADF4156** and click **OK**.

SOFTWARE OPERATION

When the main window (shown in Figure 5) opens, perform the following tasks:

1. In the left **RF Section** panel in the window, click **REF IN Frequency**. When a new window appears, change the reference frequency to 10 MHz.
2. Click **Update R0 and R1 (Normal Mode)** and then click **Exit Window**. Note that these fields have been replaced by the **Rx Updated** fields shown in blue.
3. Click **Update All Registers** (this has been replaced by **All RF Registers Updated** in Figure 5). The data is now set up. The window should look like Figure 5.

Other features can now be examined. For example, to change the VCO output frequency and/or channel spacing, click **RF VCO Output Frequency**. The output frequency window then appears, and the values can be changed. The on-board loop filter has been designed for a charge pump current of 0.3125 mA.

To examine the cycle slip reduction feature, click the **CSR Disabled** button in the main window. Note that the PFD duty cycle must be 50:50, and the charge pump current must be set to minimum to take advantage of this feature. See the ADF4156 data sheet for more information on cycle slip reduction.

EVALUATION BOARD SCHEMATICS

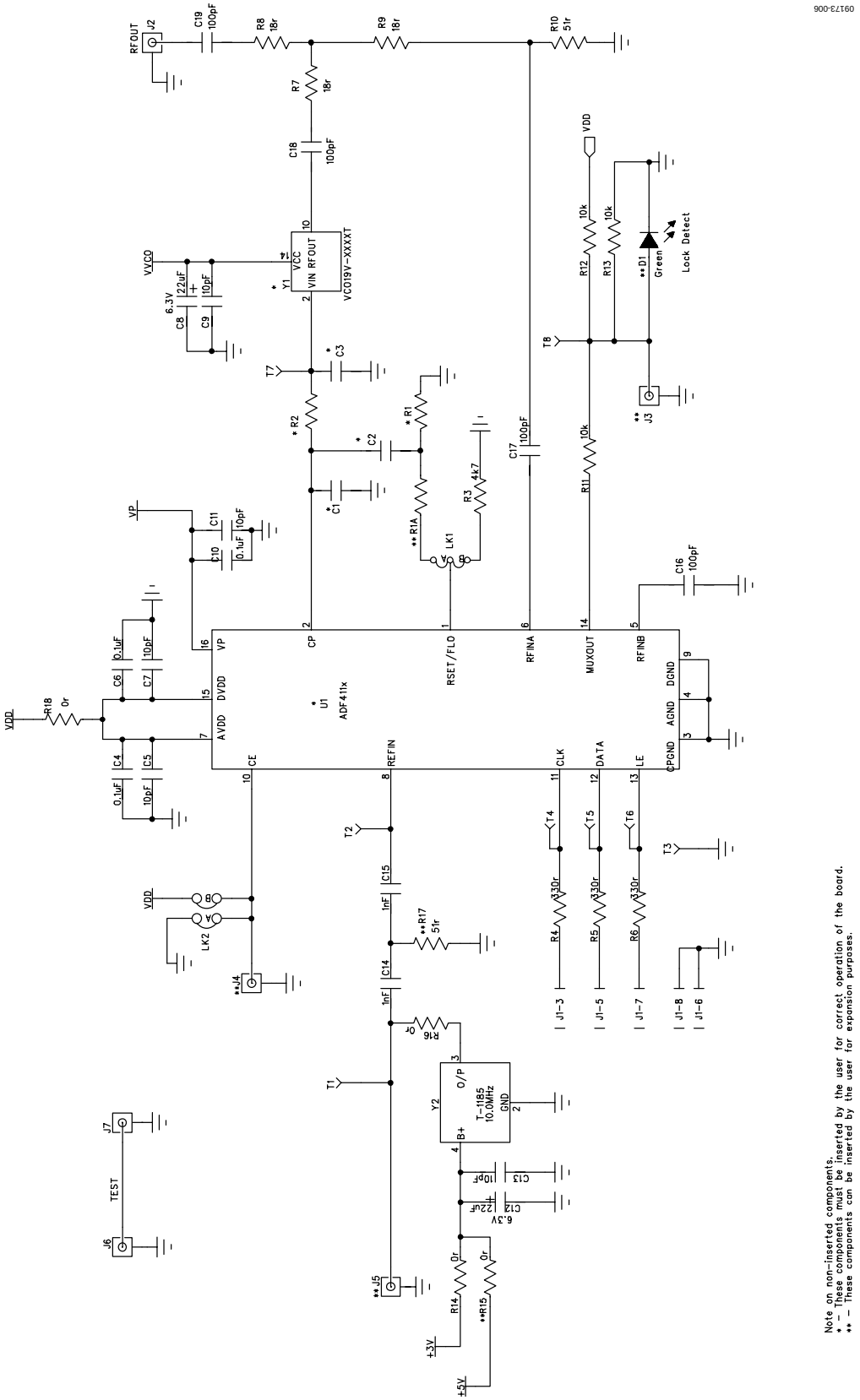

Figure 6. Evaluation Board Schematic (Page 1)

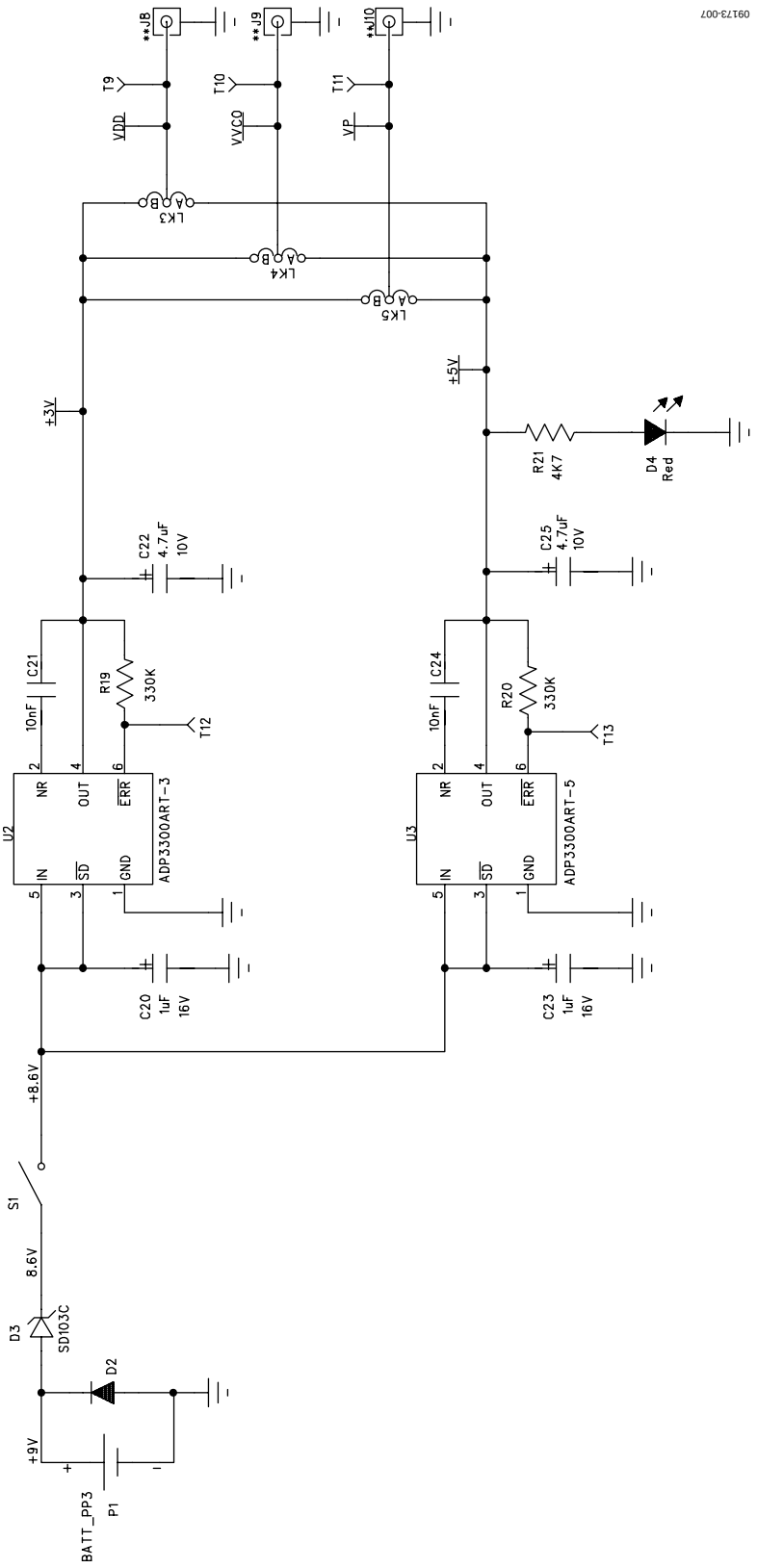

Figure 7. Evaluation Board Schematic (Page 2)

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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