Single Device Combines Pushbutton On/Off Control, Ideal Diode PowerPath and Accurate System Monitoring

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Introduction

The proliferation of handheld and battery powered devices has made controlling the power paths of two or more power sources a common power supply design task. Some designers turn to discrete components and onboard microprocessors to manage the power path between power sources and the systems they run. However, discrete component and microprocessor solutions tend to be incomplete, inconsistent and large. A better alternative is to use the LTC2952 PowerPath controller in solutions that are more robust, easier to design and more efficient than discrete and microprocessor solutions.

The LTC2952 integrates three important power management functions into a single device: pushbutton ON/OFF control, ideal diode PowerPath control and accurate system monitoring. The LTC2952's pushbutton input, which provides ON/OFF control of system power, has independently adjustable ON and OFF de-bounce times. A simple microprocessor interface involving an interrupt signal allows for proper system housekeeping prior to power down.

The ideal diode power paths provide low loss switchover between two DC sources by regulating two external P-channel MOSFETs to have a small 20mV forward drop. High reliability systems can utilize the LTC2952's system monitoring features to ensure system integrity. These monitoring features include: power-fail, voltage monitoring and µP watchdog.

Features

The overall power path management solution offered by LTC2952 is compact and low power. LTC2952 is available in a 20-pin QFN 4mm × 4mm or 20-pin TSSOP. In standby mode it only consumes 25µA of quiescent current. For systems that require efficient management of more than two power paths, multiple LTC2952s can be used together in a single system. Other features include:

- ❑ Low loss switchover between DC sources
- ❑ User control or automatic management of low loss PowerPath
- ❑ PowerPath priority
- ❑ Pushbutton ON/OFF control
- ❑ Accurate comparator for digital ON/OFF control
- ❑ Wide operating voltage range: 2.7V to 28V
- ❑ Guaranteed threshold accuracy: ±1.5% of monitored voltage over temperature
- ❑ Adjustable pushbutton ON/OFF timers
- ❑ Simple interface allows graceful µP controlled shutdown
- ❑ Extendable house keeping wait time prior to shutdown
- ❑ 200ms reset delay and 1.6s watch dog time out
- ❑ ±8kV HBM ESD on $\overline{PB}$ input
- ❑ PowerPath selection status

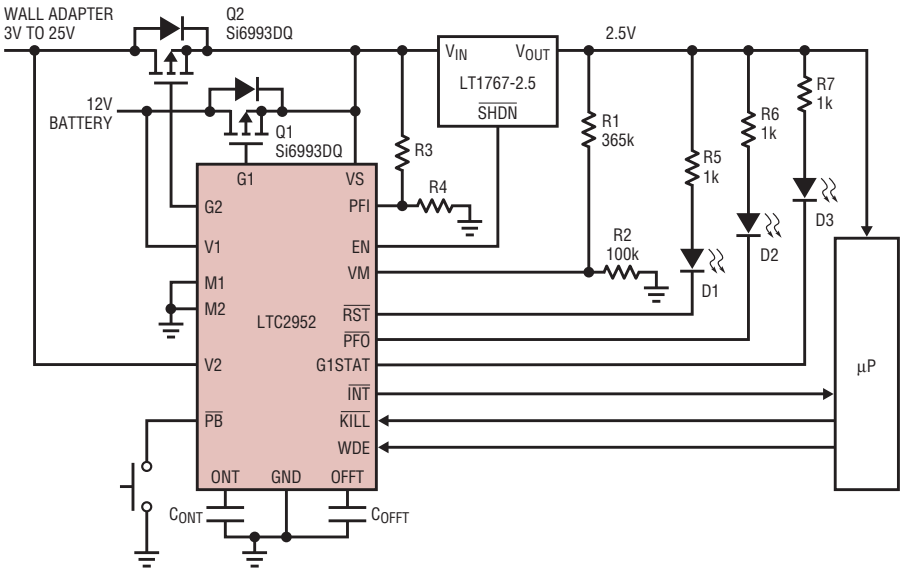

Figure 1. Typical application of LTC2952 with automatic power-ORing between wall adapter and battery and pushbutton control of a DC/DC converter

Operation

The LTC2952 is designed to simplify applications requiring management of multiple power sources. The three main features of the part are: pushbutton control, ideal diode PowerPaths and system monitoring. Figure 1 shows a typical application of the LTC2952 where it drives the output voltage (VS) to the higher of the V1 (wall adapter) or V2 (battery) inputs.

The ideal diode drivers regulate two external P-channel MOSFETs to achieve the ideal diode PowerPath behavior that allows for a low loss switchover between two DC sources. Each driver regulates the gate of the PFET such that the voltage drop across its source and drain is 20mV. When

the load current is larger than the PFET's ability to deliver the current with a 20mV drop across its source and drain, the gate drive voltage clamps at 7V and the PFET behaves like a fixed value resistor.

The pushbutton function debounces any pushbutton event on the $\overline{PB}$ pin. Note that the ON and OFF debounce times can be programmed independently by using two separate capacitors on the ONT and OFFT pins respectively. A valid pushbutton ON sets the EN pin to high impedance and a valid pushbutton OFF drives the EN pin low. In a typical application the EN pin is tied to the shutdown pin of a DC/DC converter. Therefore by toggling the EN pin, the pushbutton pin has direct control over the enabling/disabling of an external DC/DC converter. This control of system turn ON/OFF is accompanied by a graceful interface to a µP to ensure proper system power up and power down.

The LTC2952 also provides system monitoring functions via the VM, WDE, $\overline{RST}$ and PFI, $\overline{PFO}$ pins. The VM and WDE pins are respectively the voltage monitoring and the watchdog input pins that determine the state of the $\overline{RST}$ output with 200ms reset time and 1.6s watchdog time. The PFI and $\overline{PFO}$ pins are the input and output of an accurate comparator that can be used as an early warning power fail monitor.

The $\overline{KILL}$, M1 and M2 pins are inputs to accurate comparators with 0.5V thresholds. The outputs of these comparators interact with the internal logic to alter the ideal-diode power paths and the pushbutton control behavior. Specifically, the $\overline{KILL}$ input provides any application with a capability to turn off system power at any point during operation. M1 and M2 pins are mode pins that configure the part to have slightly different behavior in the power path switchover of the two DC sources.

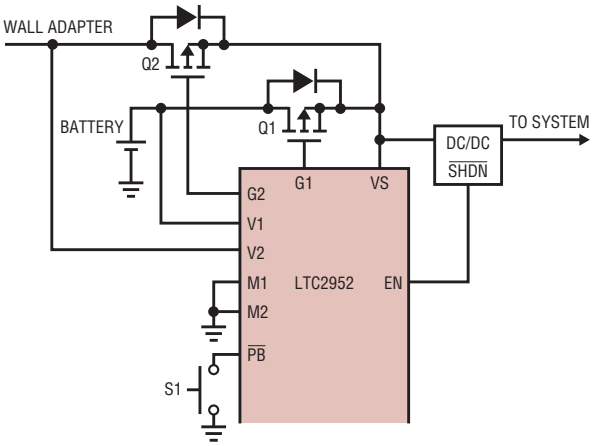

Figure 2. Power path configuration A: pushbutton controller with automatic power-ORing between wall adapter and battery

Power Path Configurations

Configuration A: Pushbutton Controller with Automatic Power-ORing between Wall Adapter and Battery

Figure 2 shows both the M1 and M2 pins connected to ground, which enables both of the ideal diodes. In this setup, power from the VS node to the system is controlled via the EN pin, which is connected to the shutdown pin of a DC/DC converter. Pushbutton control at the $\overline{PB}$ input toggles the EN pin.

Configuration B: Pushbutton Controller with Preferential Wall Adapter Operation and Automatic Switchover to Battery

In Figure 3 the M1 pin is connected to ground and the M2 pin monitors the wall adapter input. When the wall adapter voltage is below the trip threshold, both ideal diodes are enabled. When the wall adapter voltage is above the trip threshold, the primary ideal diode driver is disabled (shutting off Q1 and Q3) and the secondary ideal diode driver is enabled (turning on Q2). This means the load current is supplied from the wall adapter (V2) regardless of the voltage level at the battery (V1).

Because of the possible current path through the PFET body diode, a back-to-back PFET configuration must be used for Q1, Q3 to make sure that no current flows from the battery (V1) to VS even if the wall adapter (V2) voltage is less than the battery (V1) voltage.

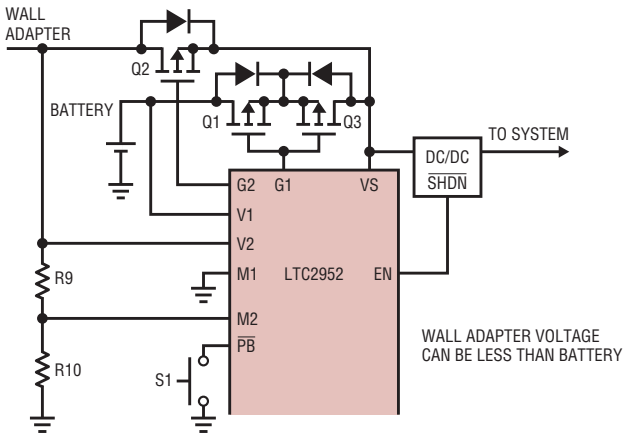

Figure 3. Power path configuration B: pushbutton controller with preferential wall adapter operation and automatic switchover to battery

Configuration C: Pushbutton Control of Ideal Diode Drivers

In Figure 4, the M2 pin is tied to the M1 pin. Since the M1 pin has a 3µA internal pull-up current, this current causes both M1 and M2 to pull

up above 0.515V (the typical M1 and M2 pins rising threshold). This setup causes the device to operate such that the $\overline{PB}$ pin has complete control on both the ideal diode drivers and the EN pin. The first valid pushbutton input turns on both of the ideal diode drivers, causing the VS pin to be driven to the higher of either the wall adapter or the battery input. Conversely, the second valid pushbutton input turns off the ideal diodes after a shutdown sequence involving an interrupt to the system.

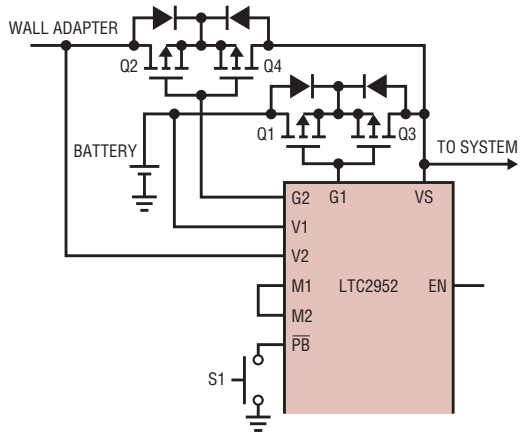

Figure 4. Power path configuration C: pushbutton control of ideal diode drivers

Configuration D: Battery Backup with Pushbutton Power Path Controller

In this configuration the M1 pin is left floating, causing its 3µA (typ) internal pull-up to pull it above its rising threshold. With M1 high, the device operates such that the rising edge and the falling edge on the M2 pin are interpreted as digital ON and OFF commands respectively.

In this particular battery back up application (Figure 5), the M2 pin monitors the wall adapter voltage. When power is first applied to the wall adapter so that the voltage at the M2 pin rises above its rising trip threshold (a digital ON command), both of the ideal diode drivers and the DC/DC converter are enabled. Thus, power is delivered to the system. As soon as the wall adapter voltage falls below its trip threshold (a digital OFF command), a shutdown sequence is immediately started. At the end of the shutdown sequence, the ideal diode drivers and the DC/DC converter are disabled. As a result power is cut off from the load and the system is in shutdown.

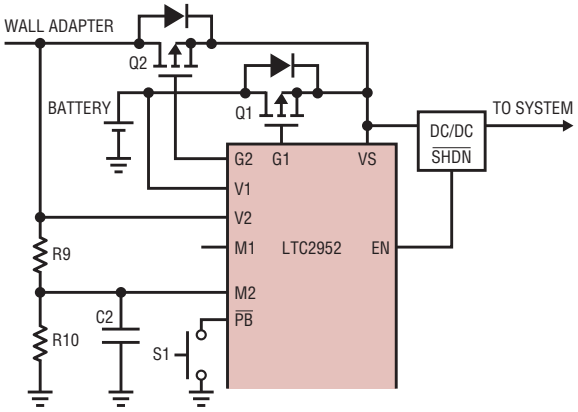

Figure 5. Power path configuration D: battery backup with pushbutton power path controller

Once power is delivered to the system, the $\overline{PB}$ pin can be used to turn off the power. If $\overline{PB}$ is used to turn off the power in this configuration, there are two methods to turn the power back on: a valid pushbutton ON at the $\overline{PB}$ pin, or cycling of the wall adapter voltage (bringing the voltage level at the M2 pin down below its threshold and then back up above its threshold—a digital ON command).

The voltage threshold of the wall adapter input (as monitored at the M2 pin) is usually set higher than the battery input voltage. Therefore, the only time power is drawn from the battery (V1 pin) is during the shutdown sequence when the voltage at the wall adapter input (V2 pin) has collapsed below the battery input voltage level.

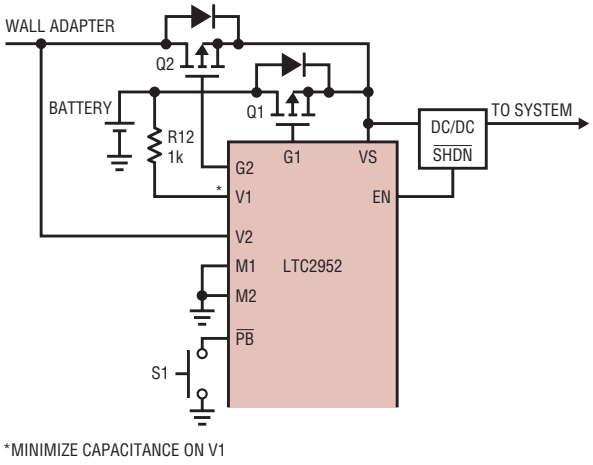

Figure 6. Reverse battery protection on V1

Reverse Battery Protection

To protect the LTC2952 from a reverse battery connection, place a 1k resistor in series with the respective supply pin intended for battery connection (V1 and/or V2) and remove any capacitance on the protected pin. In Figure 6, R12 protects the V1 pin from a reverse battery connection.

Pushbutton Bounce

When a pushbutton is pressed, the voltage on the pin does not seamlessly switch from the pull-up voltage to ground. The voltage fluctuates as the pushbutton makes and breaks contacts for quite a number of cycles before finally settling.

Figure 7 shows a scope photo with significant bounce on the pushbutton pin. The LTC2952 ignores all the noise and sets a clean internal ON/OFF signal only after the pushbutton stops bouncing for 26ms plus the additional programmed time determined by the external capacitors CONT and COFFT.

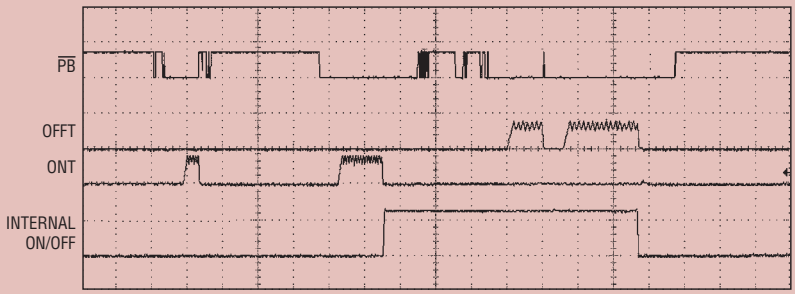

Figure 7. Scope photo of a typical pushbutton bounce

The value of the reverse battery protection resistor should not be too large because the V1 and the V2 pins are also used as the anode sense pins of the ideal diode drivers. When the ideal diode driver is on, the VS pin supplies most of the quiescent current of the part (60µA) and each of the supply pins supplies the remaining quiescent current (20µA each). Therefore, the recommended 1kΩ reverse battery protection resistor amounts to an additional 20mV (1kΩ• 20µA) drop across the P-channel MOSFET.

Pushbutton Input

The $\overline{PB}$ pin is a high impedance input to an accurate comparator with a 10µA pull up to an internal low voltage supply (4.5V). The $\overline{PB}$ input comparator has a 0.775V falling trip threshold with 25mV of hysteresis. Due to novel protection circuitry, the $\overline{PB}$ pin can operate over a wide operating voltage range (–6V to 28V) as well as having an ESD HBM rating of ±8kV.

The pushbutton circuitry's main function is to debounce the input to the $\overline{PB}$ pin into a clean signal that initiates a turn-on or a turn-off power sequence. A complete pushbutton consists of a push event and a release event.

The push event debounce duration on the $\overline{PB}$ pin can be increased beyond the fixed internal 26ms by using an external capacitor. Specifically, placing a capacitor on the ONT and OFFT pins increases the debounce duration for the push event to turn on and the push event to turn off, respectively. The following equations describe the additional debounce time that a push event at the $\overline{PB}$ pin must satisfy before it is recognized as a valid pushbutton ON or OFF command.

$t_{ONT} = C_{ONT} \bullet 9.3[M\Omega]$

$t_{OFFT} = C_{OFFT} \bullet 9.3[M\Omega]$

C_{ONT} and C_{OFFT} are the ONT and OFFT external programming capacitors respectively.

During a turn-off push event (Figure 8), the $\overline{INT}$ pin is asserted low after the initial 26ms debounce duration. The $\overline{INT}$ pin continues to assert low while the $\overline{PB}$ pin is held low during the OFFT debounce duration. If the $\overline{PB}$ pin pulls high before the OFFT time ends, the $\overline{INT}$ immediately turns high impedance. On the other hand, if the $\overline{PB}$ pin is still low at the end of the OFFT time, the $\overline{INT}$ continues to assert low throughout the ensuing shutdown sequence.

On a release event (rising edge) on the $\overline{PB}$ pin following a valid push event, the $\overline{PB}$ pin must be continuously held above its rising threshold (0.8V) for a fixed 26ms internal debounce time before the next push event is recognized. Figure 8 shows a particular sequence of $\overline{PB}$ signals being debounced into a clean internal ON/OFF signal, and its effect on the state of the $\overline{INT}$ pin.

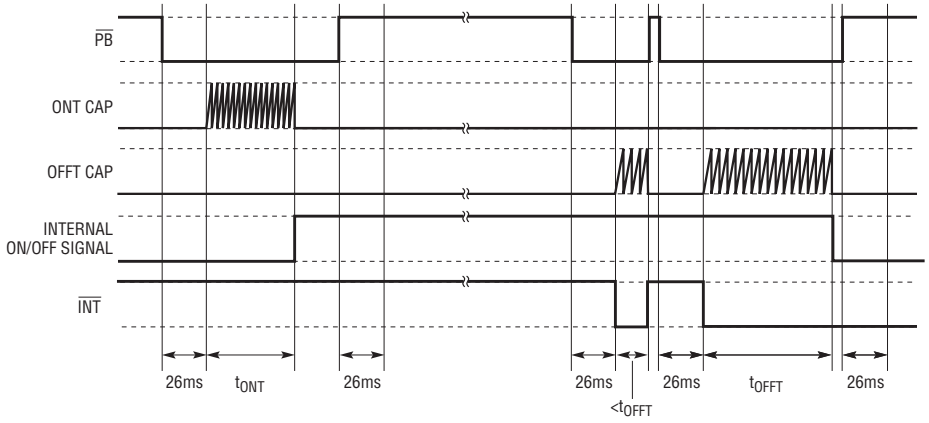

Figure 8. Pushbutton debounce timing

Accurate Comparator Input Pins VM, PFI, $\overline{KILL}$, M1 and M2

VM, PFI, $\overline{KILL}$, M1 and M2 are all high impedance input pins to accurate comparators with a falling threshold

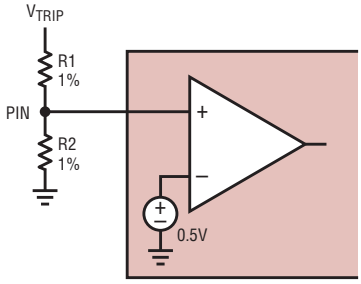

Figure 9. Setting the comparator input trip point

of 0.5V (typ). Note the following differences between some of these pins: the VM pin comparator has no hysteresis while the other comparators have 15mV of hysteresis and the M1 pin has a 3µA pull up current while the other inputs pins do not.

Figure 9 shows a typical application where the VM, PFI, $\overline{KILL}$ or M2 pin connects to a tap point on an external resistive divider between a positive voltage and ground. The following formula shows the falling trip voltage from the resistor's value:

$$V_{FALLING-TRIP} = 0.5V\left(1+\frac{R1}{R2}\right)$$

M1 is different from the other high impedance input pins in that it has a 3µA internal pull up current. Typically the M1 pin is usually either connected to ground or left floating. When left floating, the internal 3µA pull up drives the M1 pin above its rising threshold (0.515V). Note that this 3µA pull up current can be used to pull up any of the other high impedance input pins. For example, many applications call for shorting the M1 and M2 pins so both are pulled above their rising thresholds.

Voltage Monitoring and Watchdog Function

The first voltage monitor input is PFI. This pin is a high impedance input to an accurate comparator with 15mV hysteresis. When the voltage at PFI is higher than its rising threshold (0.515V), the $\overline{PFO}$ pin is high impedance. Conversely, when the voltage level at PFI is lower than its falling threshold (0.5V), the $\overline{PFO}$ pin strongly pulls down to GND.

The second voltage monitor input is VM. This VM pin together with the WDE pin (as a watchdog monitor pin) affects the state of the $\overline{RST}$ output pin. The VM pin is also a high impedance input to an accurate comparator. However, the VM comparator has no hysteresis and hence the same rising and falling threshold (0.5V). When the voltage level at VM is less than 0.5V, the $\overline{RST}$ pin strongly pulls down to GND. When the voltage level at VM rises above 0.5V, the $\overline{RST}$ output pin is held low for a reset time out period (200ms) before turning high impedance.

After the $\overline{RST}$ pin becomes high impedance, if the WDE input pin is *not* left floating or *not* in a high-Z state, the watchdog timer is started. The watchdog timer is reset every time there is an edge (high to low or low to high transition) on the WDE pin. The watchdog timer can expire if no valid edge occurs on the WDE pin in a watch dog timeout period (1.6s) after the $\overline{RST}$ pin transitions from pulling low to being high impedance. It can also expire if no valid edge occurs on the WDE pin in a watchdog timeout period since the last valid edge on the WDE pin while the $\overline{RST}$ pin is high impedance.

When the watchdog timer is allowed to expire while the voltage at the VM pin is higher than 0.5V, the $\overline{RST}$ pin strongly pulls down to ground for a reset time out period (200ms) before again being high impedance for a watchdog timeout period (1.6s). This continues until there is again an edge at the WDE pin, the voltage at VM goes below 0.5V, or the watchdog function is disabled (by leaving the WDE pin floating or in a high-Z state).

Power Turn-On/ Turn-Off Sequence

Figure 10 shows a typical system power-on and power-off timing diagram. Note that in this timing diagram only the clean internal ON/OFF signal is shown. A transition at this internal ON/OFF signal can be caused by a valid debounced pushbutton at the $\overline{PB}$ pin or a digital ON/OFF command through the mode input pins (M1/M2).

In this timing sequence, the $\overline{KILL}$ pin has been set low since power is first applied to the LTC2952. As soon as the Internal ON/OFF signal transitions high (t1), the EN pin goes high impedance and an internal 500ms timer starts. During this 500ms, KILL On Blanking period, the input to the $\overline{KILL}$ pin is ignored and the EN pin remains in its high impedance state. This KILL On Blanking period is designed to give the system sufficient time to power up properly.

Once the µP/system powers on, it should set the $\overline{KILL}$ pin high (t2) indicating that proper power up sequence is completed. Failure to set $\overline{KILL}$ pin high at the end of the 500ms KILL On Blanking period (t3) results in an immediate system shut down (EN pin pulling down). However, in this typical sequence, with the $\overline{KILL}$ pin high at the end of the KILL On Blanking period, the system transitions to normal operation with power turned on.

When the Internal ON/OFF signal transitions low (t4), a shutdown sequence is immediately started. Note that during the shutdown sequence the $\overline{INT}$ pulls low. However, the transition from high to low at the $\overline{INT}$ pin can either occur at the beginning of the shutdown sequence if the transition low at the internal ON/OFF signal is as a result of a digital OFF command or earlier if the transition at the internal

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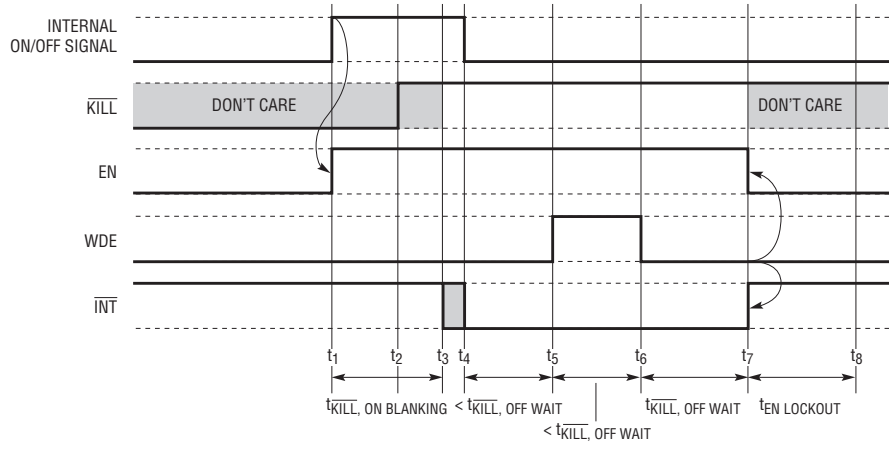

Figure 10. Typical power on and power off sequence

A 3.3V Input, 5V/2A Output Boost Converter

Figure 1 shows a typical LTC3872 application—a 3.3V input to 5V output boost regulator which can deliver up to 2A load current. Figure 2 shows the efficiency/power loss curve. In spite of the converter's small size, efficiency peaks at 90% and stays above 80% down to 20mA. In shutdown mode it draws only 8µA.

The LTC3872 uses the drain to source voltage of the external N-channel MOSFET to sense the inductor current. Eliminating a separate sense resistor can increase efficiency by 1%–2% at heavy loads. Absent a short circuit at the output, the maximum current that the converter can draw from V_{IN} is determined by the $R_{DS(ON)}$ of the MOSFET (a function of the gate drive voltage V_{IN}). This maximum current can be adjusted by using the three-state current limit programming pin IPRG.

A 5V Input, 48V/0.5A Output Boost Converter

Figure 3 shows the LTC3872's ability to deliver high output voltage. In this topology, the limitation on V_{OUT} is the 60V maximum rating of the SW pin. Where even higher output voltages are required, a sense resistor can be inserted between the source of the MOSFET and ground, with the SW pin tied to the high side of the sense resistor. The output is well-controlled against overshoot and undershoot during startup and load transients (Figure 4). At high duty cycle under heavy loads, the commutation cycle (here, 1/550kHz) is too brief to allow the average inductor current to equal the converter's required input current. In this case, the on-time of MOSFET M1 is extended, and inductor current ramps up to the level required to maintain output regulation (Figure 5).

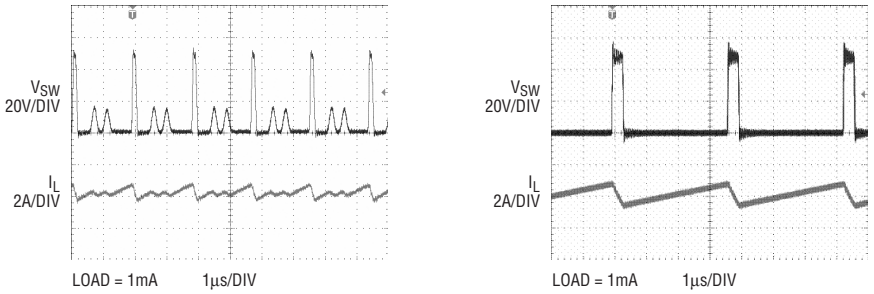

Figure 5. At light loads, the circuit of Figure 3 uses pulse skip mode. In this mode operation does not exceed the (80%) maximum duty cycle of the converter at 550kHz. At heavy loads, the maximum duty cycle is extended by allowing the switching frequency to fall.

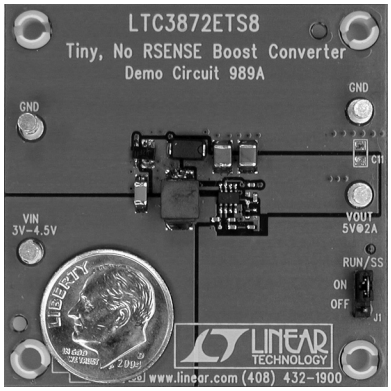

Figure 6. A typical LTC3872 application occupies just 2.25cm².

Conclusion

The LTC3872 is a tiny current-mode, non-synchronous boost controller that requires no sense resistor—a typical design occupies 2.25cm² (Figure 6). The small solution size and wide input voltage range make it an easy fit for a variety of applications.

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ON/OFF signal is caused by a valid pushbutton OFF.

From the start of the shutdown sequence, the system power turns off in 500ms, unless an edge (a high-to-low or low-to-high transition) at the WDE pin is detected within the 500ms period to extend the wait period for another 500ms. This KILL Wait time (500ms/cycle) is designed to allow the system to finish performing its house keeping tasks before shut down.

Once the µP finishes performing its power down operations, it can either let the KILL Wait time expire on its own or set the $\overline{KILL}$ pin low to immediately terminate the KILL Wait time. When the KILL Wait time expires, the LTC2952 sets EN low. This turns off the DC/DC converter connected to the EN pin. In the sequence shown in Figure 10, the KILL Wait time is reset twice with edges on the WDE pin (t5 and t6) before finally expiring (t7).

When the DC/DC converter is turned off (EN goes low), it can take a significant amount of time for its output level to decay to ground. In order to guarantee that the µP has always powered down properly before it is re-started, another 500ms (Enable Lock Out period) timer is started to allow for the DC/DC converter output power level to power down completely to ground. During this Enable Lock Out period, the EN pin remains in its low state regardless of any transition at the internal ON/OFF signal. At the end of the 500ms Enable Lock Out time (t8) the LTC2952 goes into its reset state, ready for the next turn on sequence. Note that at this reset state the EN pin remains strongly pulling down.

Conclusion

The LTC2952 is a versatile, full featured Power Path Management IC that provides robust pushbutton ON/OFF control with a simple and graceful communication interface to the system microprocessor. Its wide voltage range, gate drive capability and low power fit an extensive number of applications requiring efficient management of two or more power paths. To further complement the requirements of highly reliable systems, the LTC2952 also offers voltage and watchdog monitoring capabilities.

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