Application Report
SLAA252–May 2005

Interfacing the DAC7554 to the MSP430F449

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ABSTRACT

This application report describes how to interface the DAC7554 digital-to-analog converter to the MSP430F449 mixed signal microcontroller.

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1 Introduction

The DAC7554 is a quad-channel, low-power, 12-bit resolution, voltage output digital-to-analog converter (DAC), which features low glitch, 12-bit monotonic with double-buffered serial interface. The double-buffered register architecture is implemented to allow simultaneous updating of all DACs while writing new data to each input register. The communication port, which is interfaced with the MSP430F449 using SPI protocol, accepts 16 bits of serial input data.

Whereas the DAC7554 can be powered from a single supply source of +2.7 V minimum to +5.5 V maximum, this application report only focuses on a +5-V power supply applied to V_{DD}. Although the digital logic of the DAC7554 is specified with CMOS logic compatibility, it is still possible to reliably drive its logic input lines at +3 V minimum (no less) with the tradeoff of higher power consumption. Because the MSP430F449 microprocessor provides +3.3-V logic, the DAC7554 consumes more power (approximately 1 mA per logic input pin driven) for this specific application example.

The voltage source for the reference supply of the DAC7554 comes from the REF3140, which provides 4.096 V with an accuracy of 0.2% maximum and a drift of 15 ppm/°C.

2 Hardware Setup Configuration

This application report is written based on an experiment using the HPA449 platform for the MSP430F449 and the DAC7554 EVM revision A. Once the HPA449 and the DAC7554 EVM are configured properly, they can be connected together easily. Figure 1, Figure 2, and Figure 3 show the hardware configuration setup for both the HPA449 and the DAC7554 EVM boards.

The HPA449 comes configured with the correct jumper settings from factory (see Figure 1). The hardware setup configuration for the DAC7554 EVM (see Figure 2) depicts the simple diagram of the interface connection between the DAC7554 and the MSP430F449, as shown in Figure 3.

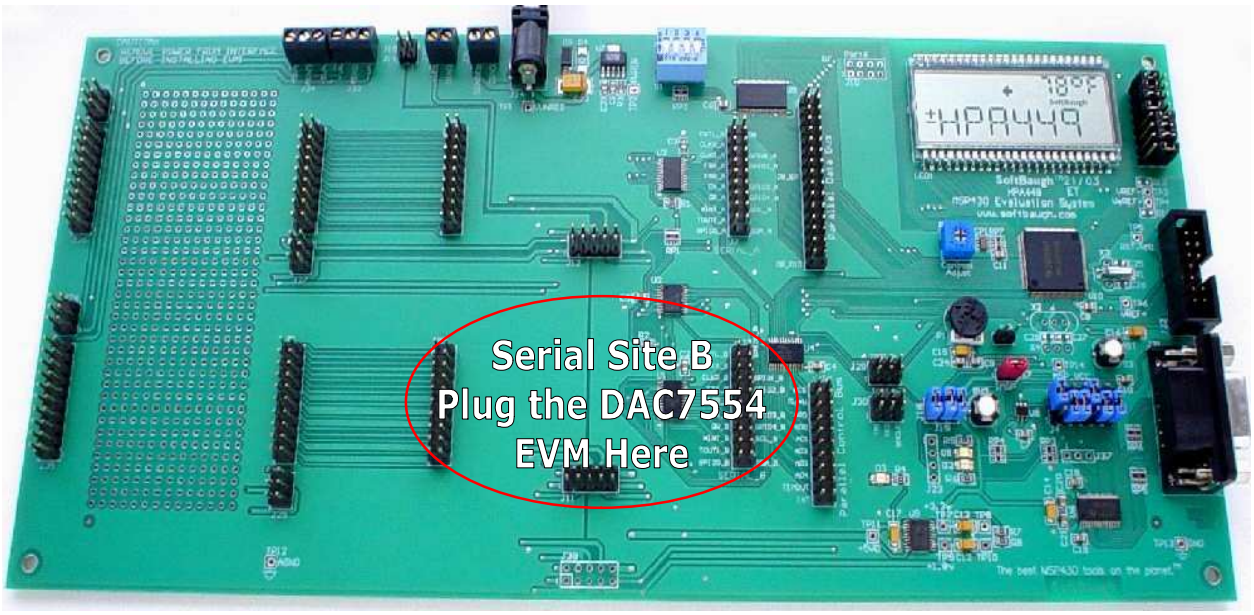

Figure 1. HPA449 Hardware Configuration

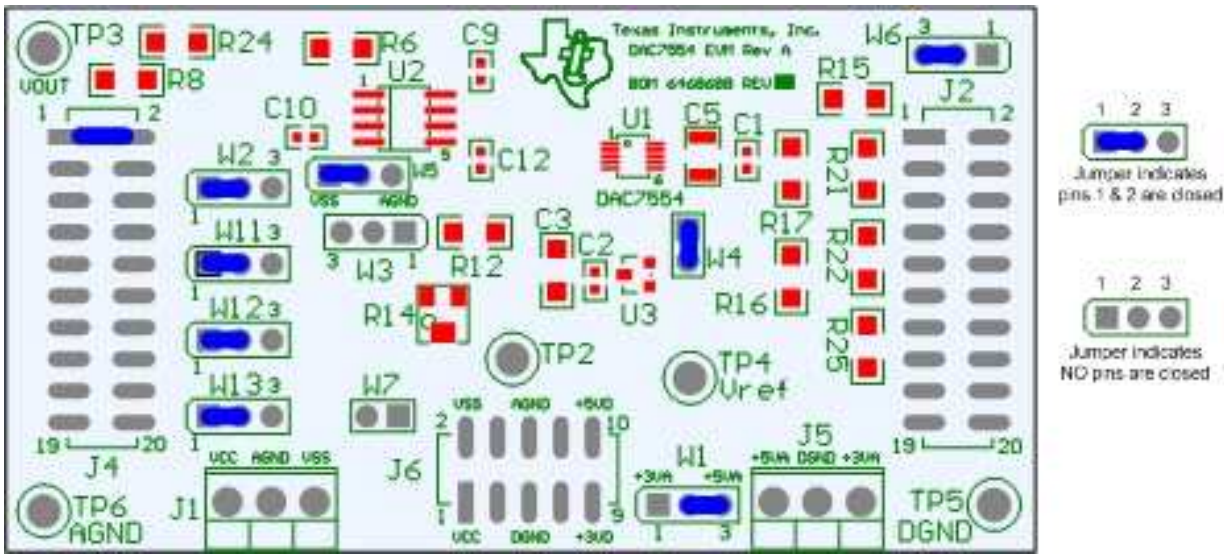

Figure 2. DAC7554 EVM Hardware Configuration

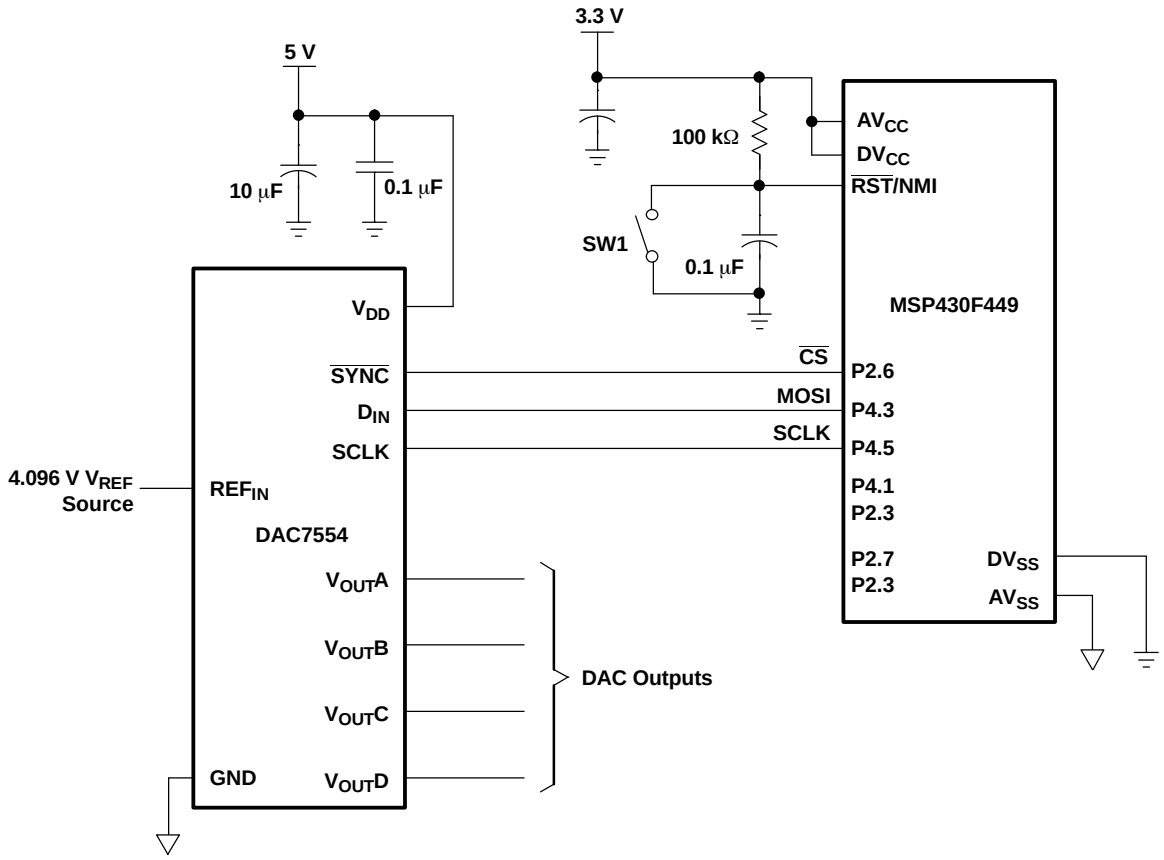

Figure 3. MSP430 and DAC7554 Circuit Diagram

3 Principle of Operation

The MSP430F449 microcontroller interfaces with the DAC7554 using the SPI serial data communication protocol via the MSP430 microcontroller's USART1 port. Only two pins are used out of the four-pin SPI mode of configuration. It is implemented this way because it is unnecessary to read any data from the DAC7554 or have the MSP430 microcontroller be slaved by another host peripheral for SPI purposes. Therefore, the STE and the MISO functions in SPI mode of the USART1 port are unused.

The $\overline{\text{SYNC}}$ function is a level-triggered signal that indicates the start of a serial data frame transfer through the SPI bus. This $\overline{\text{SYNC}}$ function is accomplished using a GPIO pin, P2.6, of the MSP430 microcontroller to enable the serial communication and data frame synchronization.

The DAC7554 receives a 16-bit digital input word serially. Because the SPI only provides eight data clocks per transmission, two write cycles are required within the $\overline{\text{SYNC}}$ low period to complete one write cycle to the DAC7554; this is shown in Figure 4. The first two bits (LD1 and LD0), starting from the MSB, contain the load bits that select the type of load to be performed. The load bits work with the SEL1 and SEL0 bits to select one of 16 different DAC load and update combinations. See Table 1 for the DAC7554 load and update combinations. The last 12 bits [MSB:LSB] compose the DAC7554 digital word with the most significant bit first.

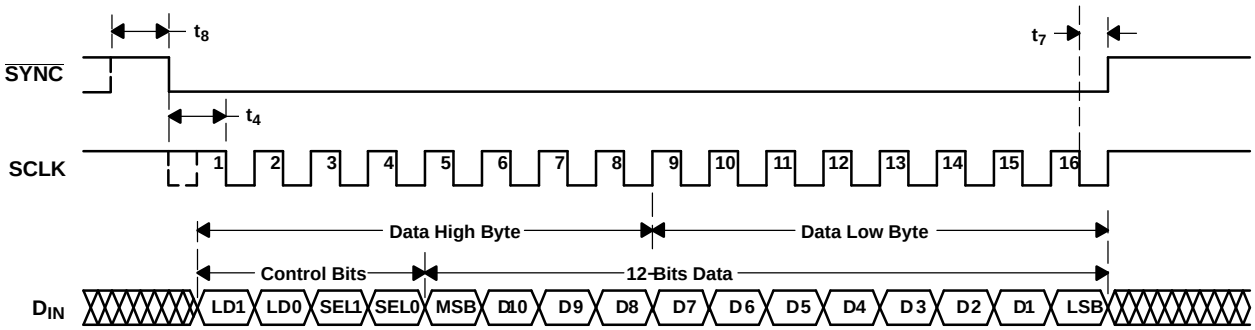

Figure 4. DAC7554 Serial Interface Timing

Table 1. DAC7554 Load and Update Combinations

CONTROL				DATA BITS	DAC(s)	FUNCTION
LD1	LD0	SEL1	SEL0	DB11–DB0		
0	0	0	0	data	A	Input register updated
0	0	0	1	data	B	Input register updated
0	0	1	0	data	C	Input register updated
0	0	1	1	data	D	Input register updated
0	1	0	0	data	A	DAC register updated, output updated
0	1	0	1	data	B	DAC register updated, output updated
0	1	1	0	data	C	DAC register updated, output updated
0	1	1	1	data	D	DAC register updated, output updated
1	0	0	0	data	A	Input register and DAC register updated, output updated
1	0	0	1	data	B	Input register and DAC register updated, output updated
1	0	1	0	data	C	Input register and DAC register updated, output updated
1	0	1	1	data	D	Input register and DAC register updated, output updated
1	1	0	0	data	A–D	Input register updated
1	1	0	1	data	A–D	DAC register updated, output updated
1	1	1	0	data	A–D	Input register and DAC register updated, output updated
1	1	1	1	data	—	Power-Down Mode – See Table 2 of the data sheet

The falling edge of SCLK clocks the data in, starting from the MSB until all 16 bits are transferred into the shift register. Any data and clock pulses after the 16th falling edge of SCLK are ignored and the transition of $\overline{\text{SYNC}}$ from low to high ends the data transfer. If the $\overline{\text{SYNC}}$ signal is taken high before the 16th falling edge of SCLK, the data transfer is aborted and the DAC input registers are not updated. As described previously, the control bits (LD1, LD0, SEL1, and SEL0) are decoded by the DAC7554 and determine the type of load and update using the contents of the shift register.

The DAC7554 features a double-buffered architecture to allow new data to be written to each of the DAC registers without disturbing the analog outputs. The first sets of registers are the DAC input registers. The second sets of registers are the DAC output registers.

4 Generating the Sine-Wave Output

The actual timing diagram of the serial peripheral interface (SPI) is shown in Figure 5. Channel 2 shows the SCLK running at approximately 4 MHz while channel 3 shows the SDI transmitting the 16 bits of the control and data word. The control bits (LD1, LD0, SEL1, and SEL0) are set to 0xE so that the data in the shift register is loaded in the input registers and DAC registers of all four DACs, as well as updating all the DAC outputs ($V_{OUT}A$, $V_{OUT}B$, $V_{OUT}C$, and $V_{OUT}D$). Channel 1 is the $\overline{\text{SYNC}}$ signal that enables the serial communication interface of the DAC7554 and signals the start of data frame transmission.

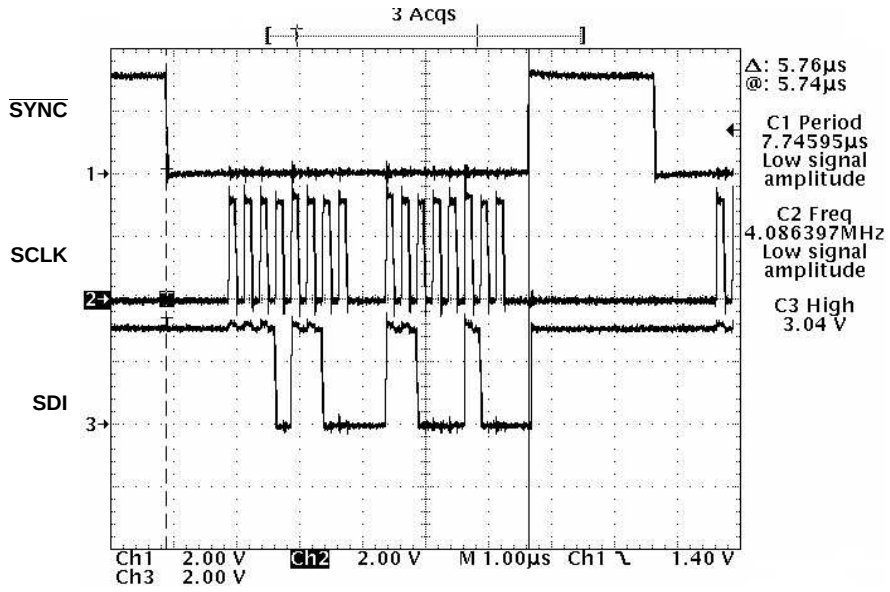

Figure 5. Actual Timing of the DAC7554 SPI

If the serial interface timing for the DAC7554 is met as shown in Figure 4 and Figure 5, the following sinusoidal waveform in Figure 6 should be observed. The DAC channel A output displays the sine wave with an amplitude of 8 V while the rest of the DAC output channels are 4 V. The signal amplitude of output A is 8 V because the DAC A channel output of the DAC7554 is connected to an external output amplifier with a gain of 2 as shown in Figure 7. Only one DAC output channel at a time can be connected to the external amplifier and evaluated using the DAC7554 EVM board.

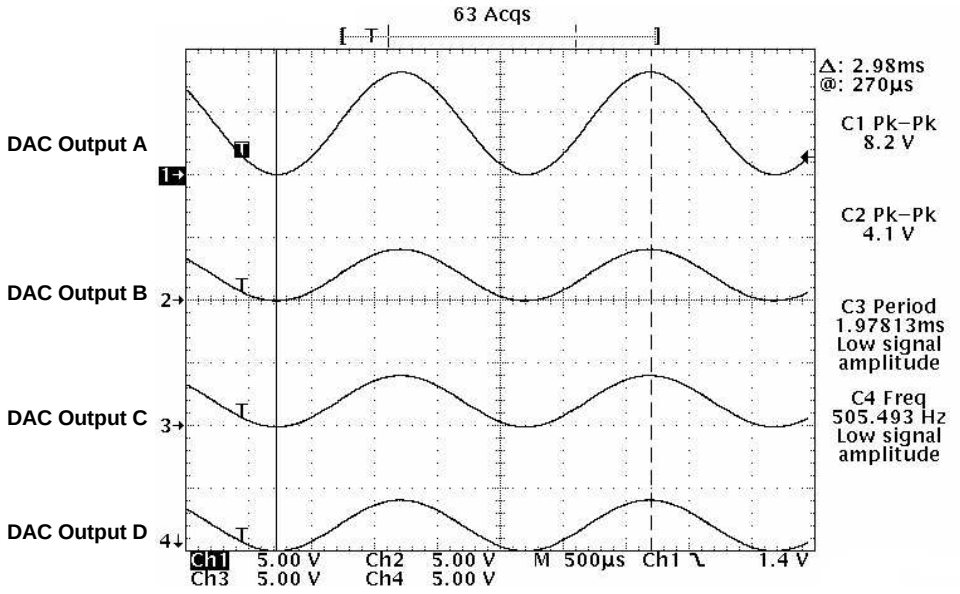

Figure 6. DAC Output Waveform Diagram

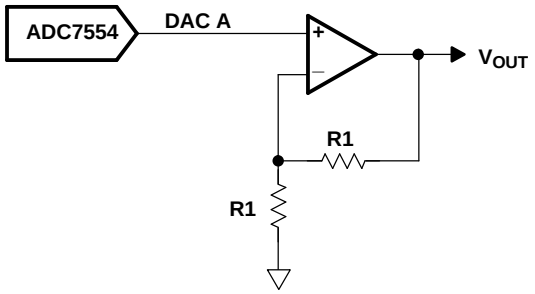

Figure 7. DAC A Output With a Gain of 2 (1 of 4 DACs)

5 Summary

This application report shows how easy it is to interface the DAC7554 to the MSP430F449 microcontroller using the SPI mode of serial communication. Using the software program provided in this application report, a simple routine to generate a sinusoidal waveform is achieved. Using the DAC7554 EVM along with the HPA449 evaluation system makes it even easier. For more detailed information regarding the DAC7554, see the data sheet SLAS399. For further support, contact the TI Data Acquisition Product group by sending an e-mail to dataconvapps@list.ti.com.

For questions or information regarding the HPA449 evaluation system, contact SoftBaugh, Inc. at e-mail address info@softbaugh.com or call directly at toll free number (800) 794-5756 or commercial number (770) 772-8111.

6 References

1. *DAC7554, 12-Bit, Quad, Ultralow Glitch, Voltage Output, Digital-to-Analog Converter* data sheet (SLAS399)
2. *DAC7554 EVM User's Guide* (SLAU154)
3. *MSP430x43x, MSP430x44x, Mixed Signal Microcontroller* data sheet (SLAS344)
4. *MSP430x4xx Family User's Guide* (SLAU056)
5. *MSP430F44X Evaluation System (HPA449) User's Guide* (SoftBaugh, Inc)

Appendix A MSP430F449 Software Code

A.1 Main Code

```
;*******************************************************************
; MSP430F449 Demo - SPI Communication with DAC7554 and MSP430F449
;
; Assembled with IAR Embedded Workshop for MSP430 Kickstart
;
; Author:      Jojo Parguian
;              HPA/DAP
; Company:  Texas Instruments, Inc.
;
; Used:
;        HPA449 V1.1
;        DAC7554 EVM Rev 1 & Rev A
;*******************************************************************
#include   "msp430x44x.h"         // Standard Equations
#include   "legal.asm"
#include   "readme.asm"
#define     CSb                 0x40/* P2.6 */
#define     SPI                 0x38
#define     DATASPI             R9

;-------------------------------------------------------------------------
; 12-bit Sine Lookup table with 256 steps
;-------------------------------------------------------------------------
          ORG   01000h
;-------------------------------------------------------------------------
Sin_tab   DW  2048,2098,2148,2199,2249,2299,2349,2398,2448,2497,2546,2594,2643,2690,2738,2785
          DW  2832,2878,2924,2969,3013,3057,3101,3144,3186,3227,3268,3308,3347,3386,3423,3460
          DW  3496,3531,3565,3599,3631,3663,3693,3722,3751,3778,3805,3830,3854,3877,3899,3920
          DW  3940,3959,3976,3993,4008,4022,4035,4046,4057,4066,4074,4081,4086,4090,4093,4094
          DW  4095,4094,4093,4090,4086,4081,4074,4066,4057,4046,4035,4022,4008,3993,3976,3959
          DW  3940,3920,3899,3877,3854,3830,3805,3778,3751,3722,3693,3663,3631,3599,3565,3531
          DW  3496,3460,3423,3386,3347,3308,3268,3227,3186,3144,3101,3057,3013,2969,2924,2878
          DW  2832,2785,2738,2690,2643,2594,2546,2497,2448,2398,2349,2299,2249,2199,2148,2098
          DW  2048,1998,1948,1897,1847,1797,1747,1698,1648,1599,1550,1502,1453,1406,1358,1311
          DW  1264,1218,1172,1127,1083,1039,995,952,910,869,828,788,749,710,673,636,600,565,531
          DW  497,465,433,403,374,345,318,291,266,242,219,197,176,156,137,120,103,88,74,61,50
          DW  39,30,22,15,10,6,2,1,0,1,2,6,10,15,22,30,39,50,61,74,88,103,120,137,156,176,197
          DW  219,242,266,291,318,345,374,403,433,465,497,531,565,600,636,673,710,749,788,828
          DW  869,910,952,995,1039,1083,1127,1172,1218,1264,1311,1358,1406,1453,1502,1550,1599
          DW  1648,1698,1747,1797,1847,1897,1948,1998,2048

;-------------------------------------------------------------------------
            ORG     0F000h
;-------------------------------------------------------------------------
;*******************************************************************
;Program Code
;*******************************************************************
           RSEG CODE
;*******************************************************************
RESET
       mov.w   #0A00h,SP          ; Initialize stack-pointer
       call    #Init_Sys          ; Initialize system
       clr.w   R6
Write_Data
       mov.w   #0FFh,R6           ; Initialize table counter
       mov.w   #0,R5              ; Initialize table pointer
       mov.w   #0E000h,R10        ; For padding the MSB - Broadcast
       bic.b   #0FFh,&P1OUT
Again
       mov.w   Sin_tab(R5),DATASPI
```

```
        bis.w   R10,DATASPI         ; Set the 4 MSB to b1110
        swpb    DATASPI             ; MSB first
        bic.b   #CSb, &P2OUT        ; Enable serial port and start write
        mov.b   DATASPI,&U1TXBUF
WaitXMT1
        bit.b   #UTXIFG1, &IFG2     ; TXBUF ready?
        jnc     WaitXMT1
        swpb    DATASPI             ; LSB next
        mov.b   DATASPI,&U1TXBUF
WaitXMT2
        bit.b   #UTXIFG1, &IFG2     ; TXBUF ready?
        jnc     WaitXMT2
        mov.w   #01h, R14
Delay0
        dec.w   R14                 ;
        jnz     Delay0
        bis.b   #CSb, &P2OUT        ; End SPI transfer
        incd.w  R5                  ; Increment table pointer
        sub.w   #1,R6               ; Decrement table counter
        and.w   #0FFh,R6            ; Check if bottom of table counter
        jnz     Again               ; Get another sample
        jmp     Write_Data          ; Repeat cycle
;-------------------------------------------------------------------
Init_Sys;  Modules and Controls Registers set-up subroutine
;-------------------------------------------------------------------
StopWDT
        mov.w   #WDTPW+WDTHOLD,&WDTCTL          ;Stop Watchdog Timer
SetupFLL2
        bis.b   #FN_4,&SCFI0                    ; x2 DCO, 8MHz nominal DCO
        bis.b   #DCOPLUS+XCAP14PF,&FLL_CTL0     ; DCO+, configure load caps
        mov.b   #121,&SCFQCTL                   ;(121+1) x 2 x 32768 = 7.99 Mhz
SetupPorts
; Port 2
        bis.b #CSb, &P2DIR
        bis.b #CSb, &P2OUT
; Port 4
        bis.b #SPI,&P4SEL                       ;P4.3,4,5 SPI option select
SetupSPI0
        bis.b #USPIE0,&ME1                      ; Enable SPI TX/RX
        mov.b #CHAR+SYNC+MM,&U0CTL              ; 8-bit SPI Master
        bis.b #SSEL0+SSEL1+STC,&U0TCTL          ; 3-pin SPI0 mode, SMCLK
        mov.b #02h,&U0BR0
        mov.b #00h,&U0BR1
        mov.b #00h,&U0MCTL
        bis.b #UTXIE0, &P1IE
SetupSPI1
        bis.b #USPIE1,&ME2                      ; Enable SPI TX/RX
        mov.b #CHAR+SYNC+MM+SWRST,&U1CTL        ; 8-bit SPI Master
        bis.b #SSEL0+SSEL1+STC,&U1TCTL          ; 3-pin SPI1 mode, SMCLK
        mov.b #002h,&U1BR0
        mov.b #000h,&U1BR1
        mov.b #000h,&U1MCTL
        bis.b #USPIE1,&ME2
        bic.b #SWRST, &U1CTL
        ret
;-------------------------------------------------------------------------------
          COMMON  INTVEC            ; MSP430x11x1/MSP430F14x Interrupt vectors
;-------------------------------------------------------------------------------
 ORG    RESET_VECTOR
RESET_VEC
        DW      RESET                           ; POR, ext. Reset, Watchdog
        END
```

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