

Using the TPS59650EVM-753 Intel™ IMVP-7 3-Phase CPU/2-Phase GPU SVID Power System

The TPS59650EVM-753 evaluation module (EVM) is a complete solution for Intel™ IMVP7 Serial VID(SVID) Power System from a 9V-20V input bus. This EVM uses the TPS59650 for IMVP7 - 3-Phase CPU and 2-Phase GPU Vcore controller, the TPS51219 for 1.05VCCIO, TPS51916 for DDR3L/DDR4 Memory rail (1.2VDDQ, 0.6VTT and 0.6VTTREF) and also uses the (CSD87350Q5D) a 5mm x 6mm TI's power block MOSFETs that uses Powerstack™ technology with high-side and low-side MOSFETs for high power density and superior thermal performance.

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1 Description

The TPS59650EVM-753 is designed to use a 9V-20V Input bus to produce 6 regulated outputs for IMVP7 SVID CPU/GPU Power System. The TPS59650EVM-753 is specially designed to demonstrate the TPS59650 full IMVP7 mobile feature while providing GUI communication programming and a number of test points to evaluate the static and dynamic performance of TPS59650.

1.1 Typical Applications

- IMVP7 Vcore Applications for Adapter, Battery, NVDC or 3V/5V/12V rails

1.2 Features

The TPS59650EVM-753 features:

- Complete solution for 9V-20V Input Intel IMVP7 SVID Power System
- GUI communication to demonstrate full IMVP7 Mobile feature
- 3-Phase CPU Vcore can support up to 94A output current
- 2-Phase GPU Vcore can support up to 46A output current
- 8 Selectable Switching frequency for CPU and GPU power
- 8 Levels selectable current limit for CPU and GPU power
- Switches or Jumpers for each output enable
- On Board Dynamic Load for CPU, GPU Vcore and VCCIO output
- High efficiency and high density by using TI power block MOSFET
- Convenient test points for probing critical waveforms
- Eight Layer PCB with 1oz copper

2 TPS59650EVM-753 Power System Block Diagram

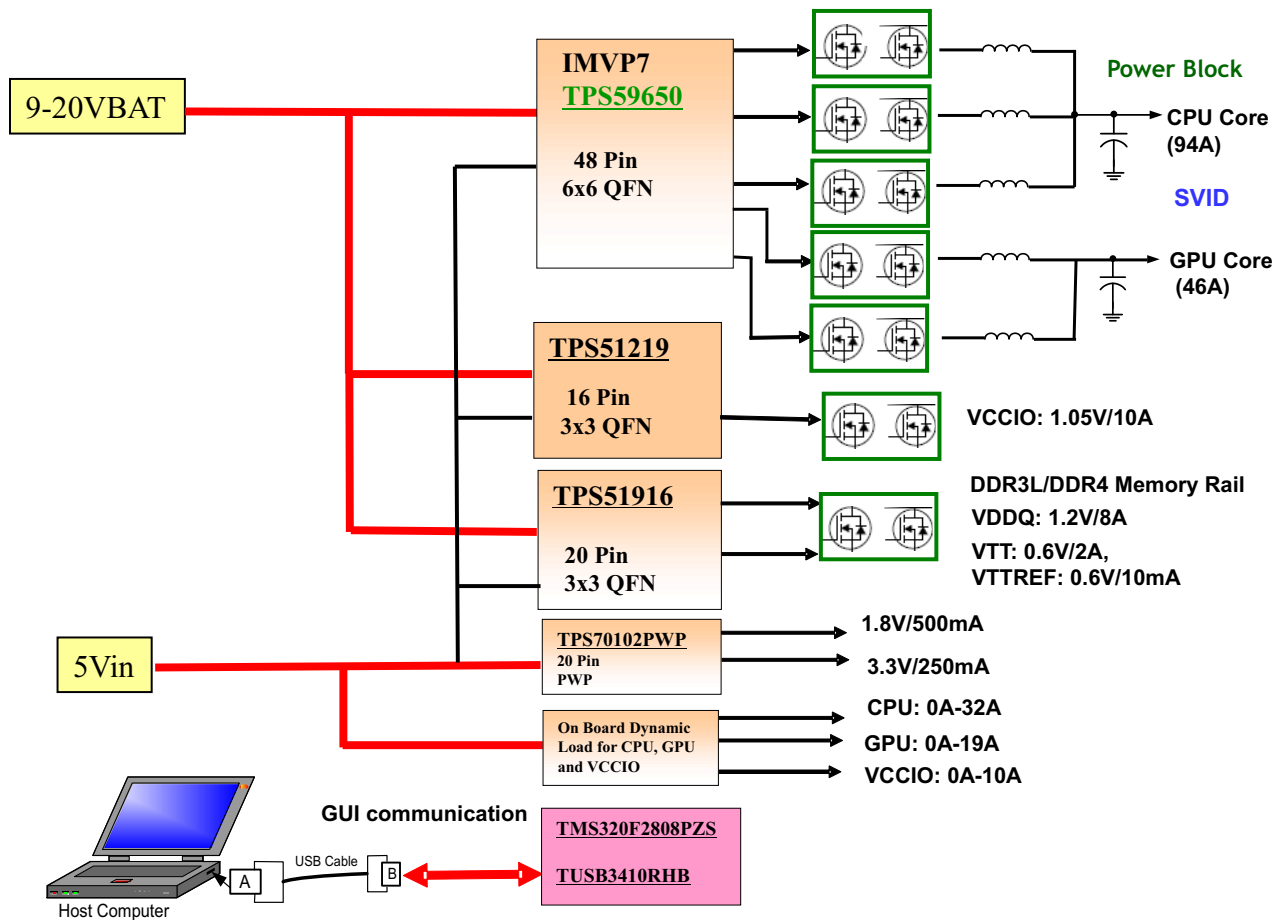


Figure 1. TPS59650EVM-753 Power System Block Diagram

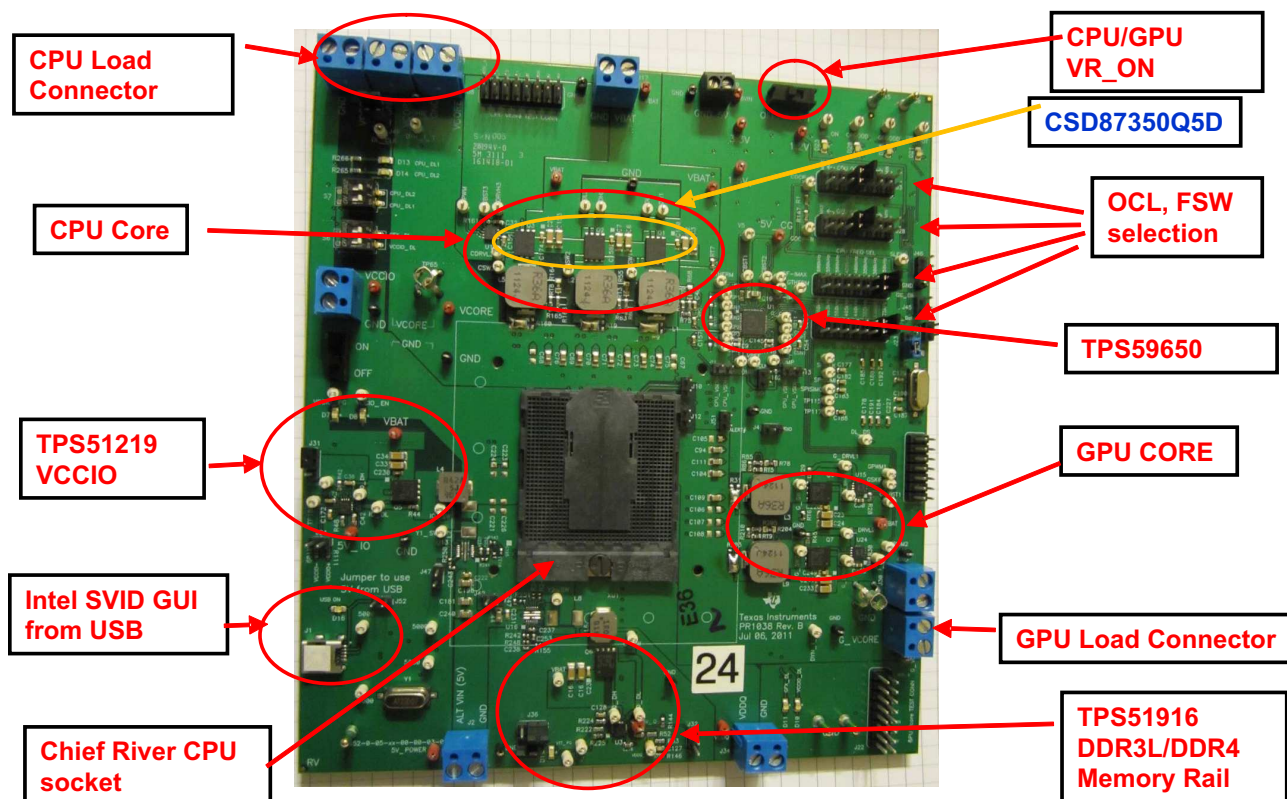


Figure 2. TPS59650EVM-753 EVM Illustration

3 Electrical Performance Specifications

Table 1. TPS59650EVM-753 Electrical Performance Specifications⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
12VBAT input voltage range	VBAT	9	12	20	V
Maximum input current	VBAT = 12V, all full load (3-Phase CPU/2-Phase GPU)		15.5		A
No load input current	VBAT=12V, all no load(3-Phase CPU/2 Phase GPU)		0.14		A
5VIN input voltage range	5Vin	4.5	5	5.5	V
Maximum input current	VBAT =12 V, all full load		0.3		A
No load input current	VBAT=12V, all no load		0.1		A
OUTPUT CHARACTERISTICS					
CPU(TPS59650)					
Output voltage Vcore	SVID: Address:00 CPU, Payload: 1.05V		1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation(Droop) Load Line		-1.9		mΩ
Output voltage ripple	VBAT=12V, 1.05V/90A(3-Phase) at 300kHz		25		mVpp
Output load current	CPU 3-Phase operation	0		94	A
Output over current	Selectable per phase		37		A
Switching frequency	Selectable	250	300	600	kHz
Full load efficiency	VBAT=12V, 1.05V/95A at 300kHz		80.05%		
GPU(TPS59650)					
Output voltage Vcore	SVID: Address:01 GPU, Payload: 1.23V		1.23		V

⁽¹⁾ Jumpers set to default locations, see section 6 of this user's guide

Table 1. TPS59650EVM-753 Electrical Performance Specifications⁽¹⁾ (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage regulation	Line regulation		0.1%		
	Load regulation(Droop) Load Line		–3.9		mΩ
Output voltage ripple	VBAT=12V, 1.23V/50A 2 Phase at 385kHz		30		mVpp
Output load current		0		50	A
Output over current	Selectable per phase		37		A
Switching frequency	Selectable	275	385	660	kHz
Full load efficiency	VBAT=12V, 1.23V/50A 2 Phase at 385kHz		86.58%		
1.05V VCCIO (TPS51219)					
Output voltage			1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VBAT=12V, 1.05V/10A		30		mVpp
Output load current		0		10	A
Output over current			16		A
Switching frequency	Selectable		500		kHz
Full load efficiency	VBAT=12V, 1.05V/10A		89.87%		
DDR3L/DDR4 Memory Rail (TPS51916)					
Output voltage			1.2		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VBAT=12V, 1.2V/8A		30		mVpp
Output load current		0		8	A
Output over current			10		A
Switching frequency	Selectable		500		kHz
Full load efficiency	VBAT=12V, 1.2V/8A		89.07%		
Operating temperature			25		°C

4 Test Setup

4.1 Test Equipment

4.1.1 PC Computer (Host Computer)

Microsoft Windows XP or newer with available USB port

4.1.2 USB Cable

The USB Cable: Standard USB_A to USB_B 5 Pin Mini-B cable. See [Figure 3](#) .


Figure 3. USB Cable

4.1.3 TPS59650 USB driver and SVID GUI Installation

1. Copy the both files: setup.exe and setup.msi to the host computer.
2. Run this setup.exe.
3. Following installation Instructions, this will install the driver and the Texas Instruments SVID GUI.
4. It will add the below icon



4.1.4 DC Source

12VBAT DC Source: The 12VBAT DC source should be a 0-20V variable DC source capable of supplying 20Adc current. Connect 12VBAT to J21 as shown in [Figure 4](#).

5Vin DC Source: The 5Vin DC source should be a 0-5V variable DC source capable of supplying 1Adc current. Connect 5Vin to J22 as shown in [Figure 4](#).

4.1.5 Meters

- **V1:** 5Vin at TP81(5Vin) and TP83(GND)
- **V2:** 12VBAT at TP82(VBAT) and TP24(GND)
- **V3:** CPU Vcore sense voltage at J7; GPU Vcore sense voltage at J9; VDDQ sense voltage at J20, VCCIO sense voltage at J16
- **A1:** 12VBAT input current

4.1.6 Load

The output load should be an electronic constant current load capable of 0-90Adc.

4.1.7 Oscilloscope

A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for 1MΩ impedance, 20MHz Bandwidth, AC coupling, 2us/division horizontal resolution, 50mV/division vertical resolution. Test point TP30 and TP46 can be used to measure the output ripple voltage for CPU and GPU. Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

4.2 Recommended Wire Gauge

1. **V5in to J22(5V input):**
The recommended wire size is 1x AWG #18 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
2. **12VBAT to J21(12V input):**
The recommended wire size is 1x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
3. **J1, J2, J3(CPU) to LOAD or J4, J5 (GPU) to LOAD or J19 (VDDQ) to LOAD or J15(VCCIO) to LOAD:**
The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return)

4.3 Recommended Test Setup

[Figure 4](#) is the recommended test set up to evaluate the TPS59650EVM-753. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before handling the EVM.

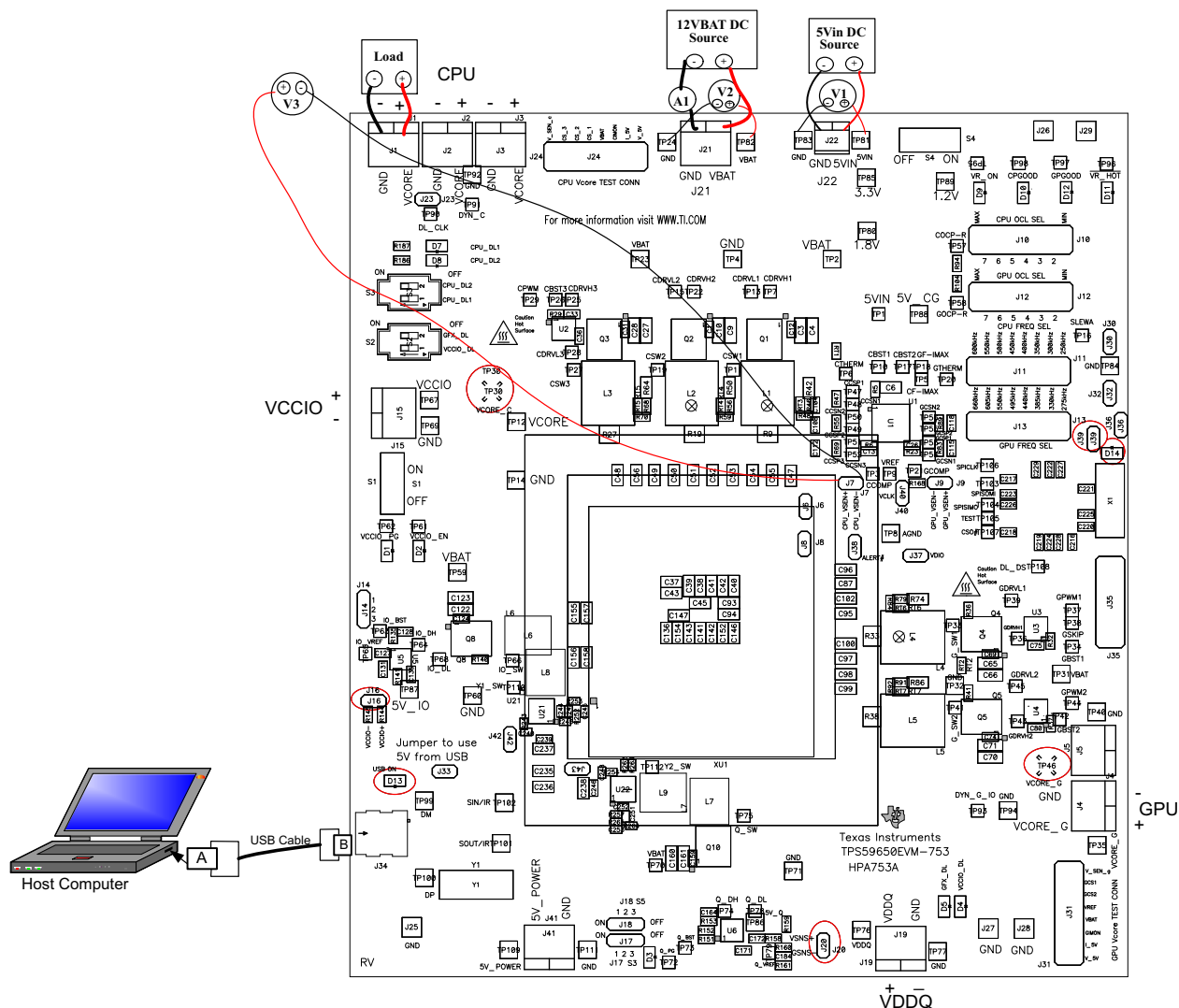


Figure 4. TPS59650EVM-753 Recommended Test Set Up

4.4 USB Cable Connections

A standard USB_A and 5 pin Mini_B USB cable needed to connect between host computer and J34 USB port (left bottom side). A GREEN LED(D13) will light up near the USB port on the EVM. This just means USB cable is connected.

4.5 Input Connections

1. Prior to connecting the 5Vin DC source, it is advisable to limit the source current from 5Vin to 1A maximum. Make sure 5Vin is initially set to 0V and connected as shown in [Figure 4](#).
2. Prior to connecting the 12VBAT DC source, it is advisable to limit the source current from 12VBAT to 10A maximum. Make sure 12VBAT is initially set to 0V and connected as shown in [Figure 4](#).
3. Connect voltmeters V1 at TP81 (5Vin) and TP83 (GND) to measure 5Vin voltage, V2 at TP82 (VBAT) and TP24 (GND) to measure 12VBAT voltage as shown in [Figure 4](#).
4. Connect a current meter A1 between 12VBAT DC source and J21 to measure the 12VBAT input current.

4.6 Output Connections

1. Connect Load to J1, J2, J3 and set Load to constant resistance mode to sink 0Adc before 5Vin and 12VBAT are applied. This is for CPU operation.
2. Connect a voltmeter V3 at J7 to measure CPU Vcore sense voltage.

5 Configuration

All Jumper selections should be made prior to applying power to the EVM. User can configure this EVM per following configurations.

5.1 CPU and GPU Configuration

5.1.1 CPU/GPU Current Limit Trip Selection (J10 for CPU and J12 for GPU)

The current limit trip can be set by J10(COCP) and J12(GOCP).

Default setting: Level 5 for both CPU and GPU.

Table 2. Current Limit Trip Selection

Jumper set to	Connected Resistor	COCP/GOCP Limit (Typ.)
Left (1-2 pin shorted)	150k	Max
2 nd (3-4 pin shorted)	100k	Level 7
3 rd (5-6 pin shorted)	75k	Level 6
4th(7-8 pin shorted)	56.2k	Level 5
5 th (9-10 pin shorted)	39.2k	Level 4
6 th (11-12 pin shorted)	30.1k	Level 3
7 th (13-14 pin shorted)	24.3k	Level 2
Right(15-16 pin shorted)	20.0k	Min

5.1.2 CPU Frequency Selection (J11)

The operating frequency can be set by J11

Default setting: 300 kHz for CPU

Table 3. CPU Frequency Selection

Jumper set to	Connected Resistor	CPU
Left (1-2 pin shorted)	150k	600 kHz
2 nd (3-4 pin shorted)	100k	550 kHz
3 rd (5-6 pin shorted)	75k	500 kHz
4 th (7-8 pin shorted)	56.2k	450 kHz
5 th (9-10 pin shorted)	39.2k	400 kHz
6 th (11-12 pin shorted)	30.1k	350 kHz
7th(13-14 pin shorted)	24.3k	300 kHz
Right(15-16 pin shorted)	20.0k	250 kHz

5.1.3 GPU Frequency Selection (J13)

The operating frequency can be set by J13

Default setting: 385 kHz for GPU.

Table 4. GPU Frequency Selection

Jumper set to	Connected Resistor	GPU
Left (1-2 pin shorted)	150k	660 kHz
2 nd (3-4 pin shorted)	100k	605 kHz
3 rd (5-6 pin shorted)	75k	550 kHz
4 th (7-8 pin shorted)	56.2k	495 kHz
5 th (9-10 pin shorted)	39.2k	440 kHz
6th(11-12 pin shorted)	30.1k	385 kHz
7 th (13-14 pin shorted)	24.3k	330 kHz
Right(15-16 pin shorted)	20.0k	275 kHz

5.1.4 F2808 DSP Program Mode Selection (J39)

The F2808 DSP Program Mode(GUI) Selection can be set by J39.

Default setting: No Jumper shorts on J39 for normal operation

Table 5. F2808 DSP Program Mode Selection

Jumper set to	Program Mode Selection
No Jumper on J39	Normal Operation
Jumper on J39	Flash the DSP program to the EVM

5.1.5 5Vin Bias Voltage Option (J33)

The 5Vin Bias Voltage can be used from USB or Externally

Default setting: No Jumper shorts on J33

Table 6. 5Vin Bias Voltage Option (J33)

Jumper set to	Selection
No Jumper	5Vin Bias from J22 external
Jumper on J39	5Vin Bias from USB, 5Vin from J22 should not be connected

5.1.6 On Board Dynamic Load Selection (S3 for CPU, S2(upper) for GPU, S2(lower) for VCCIO)

The on board dynamic load can be set by S2 and S3.

Default setting: Push S2 and S3 to “OFF” position to disable the on board dynamic load

Table 7. On Board Dynamic Load Selection

Switch set to	Dynamic Load Selection
Push S3 to “ON” position	Enable 32A on board dynamic load at CPU
Push S3 to “OFF” position	Disable 32A on board dynamic load at CPU
Push S2(upper) to “ON” position	Enable 19A on board dynamic load at GPU
Push S2(upper) to “OFF” position	Disable 19A on board dynamic load at GPU
Push S2(lower) to “ON” position	Enable 10A on board dynamic load at VCCIO
Push S2(lower) to “OFF” position	Disable 10A on board dynamic load at VCCIO

5.1.7 IMVP-7 VR_ON Enable Selection (S4)

The IMVP-7 CPU/GPU can be enabled and disabled by S4

Default setting: Push S4 to "OFF" position to disable both CPU and GPU

Table 8. VR_ON Enable Selection

Switch set to	VR_ON Selection
Push S4 to "ON" position	Enable IMVP-7 CPU/GPU Vcore
Push S4 to "OFF" position	Disable IMVP-7 CPU/GPU Vcore

5.2 1.2VDDQ, 0.6V VTT and 0.6V VTTREF Configuration

5.2.1 VDDQ S3, S5 Enable Selection

The controller can be enabled and disabled by J18 and J17.

**Default setting: Jumper shorts on Pin2 and Pin3 of J18,
Jumper shorts on Pin2 and Pin3 of J17**

Table 9. VDDQ S3, S5 Enable Selection

State	J17 (S3) set to	J18(S5) set to	VDDQ	VTTREF	VTT
S0	ON position	ON position	ON	ON	ON
S3	OFF position	ON position	ON	ON	OFF(High-Z)
S4/S5	OFF position	OFF position	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

5.3 1.05V VCCIO Configuration

5.3.1 1.05V Enable Selection (S1)

1.05V Enable can be set by S1

Default setting: Push S1 to "OFF" position

Table 10. 1.05V Enable Selection

Jumper set to	Selection
Push S1 to "ON" position	1.05V Enabled
Push S1 to "OFF" position	1.05V Disabled

5.3.2 VCCIO Output Voltage Selection (J14)

The VCCIO Output Voltage can be selected by J14

Default setting: Jumper shorts Pin1 and Pin2 of J14

Table 11. VCCIO Output Voltage Selection

Jumper set to	Selection
Jumper shorts on Pin1 and Pin2	VCCIO: 1.05V
Jumper shorts on Pin2 and Pin3	VCCIO: 1.00V

5.3.3 On Board Dynamic Load Enable Pin (J23)

The on board dynamic load can be enabled or disabled by J23

Default setting: Jumper shorts on J23

Table 12. On Board Dynamic Load Enable/Disable selection

Jumper set to	Selection
Jumper shorts	Enable on board dynamic load
No Jumper short	Disable on board dynamic load

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

6.1.1 CPU

1. Set up EVM as described in [Section 4.3](#) through [Section 4.6](#) and [Figure 4](#).
2. Ensure J39 no Jumper shorts on
3. Ensure all other Jumpers configuration setting by [Section 5](#) before 5Vin and 12VBAT are applied.
4. Ensure Load is set to constant resistance mode and to sink 0Adc
5. Ensure S1 and S4 are in "OFF" position
6. Add scope probe on the TP30 for CPU Vcore ripple measurement
7. Ensure USB Cable is connected between host computer and USB port(J34) on the EVM
8. Increase 5Vin from 0V to 5V. Using V1 to measure 5Vin input voltage.
9. Increase 12VBAT from 0V to 12V. Using V2 to measure 12VBAT input voltage.



10. Double-Click the icon to launch the GUI program. The GUI window shown in [Figure 5](#).
11. Push S4 to "ON" position to enable the VR_ON of TPS59650. VR_ON LED will light up.
12. Now the user is ready to send SVID commands. The GUI at start-up defaults:
Address: 00 CPU, Command: SetVIDslow, Payload: 1.05V (The user can select the SVID command by using the pull-down menu")
13. Click "send Command" and CPU CPGOOD LED will light up, See the GUI window as [Figure 5](#).
14. Measure V3: CPU Vcore at J7 and A1: 12VBAT input current
15. Vary CPU LOAD from 0Adc to 94Adc, CPU Vcore must remain in load line
16. Vary 12VBAT from 9V to 20V CPU Vcore must remain in line regulation
17. Push S4 to "OFF" position to disable CPU Vcore controller.
18. Decrease LOAD to 0A and disconnect the LOAD from terminal J1, J2, J3
19. Disconnect V3 from J7.
20. Disconnect scope probe from TP30

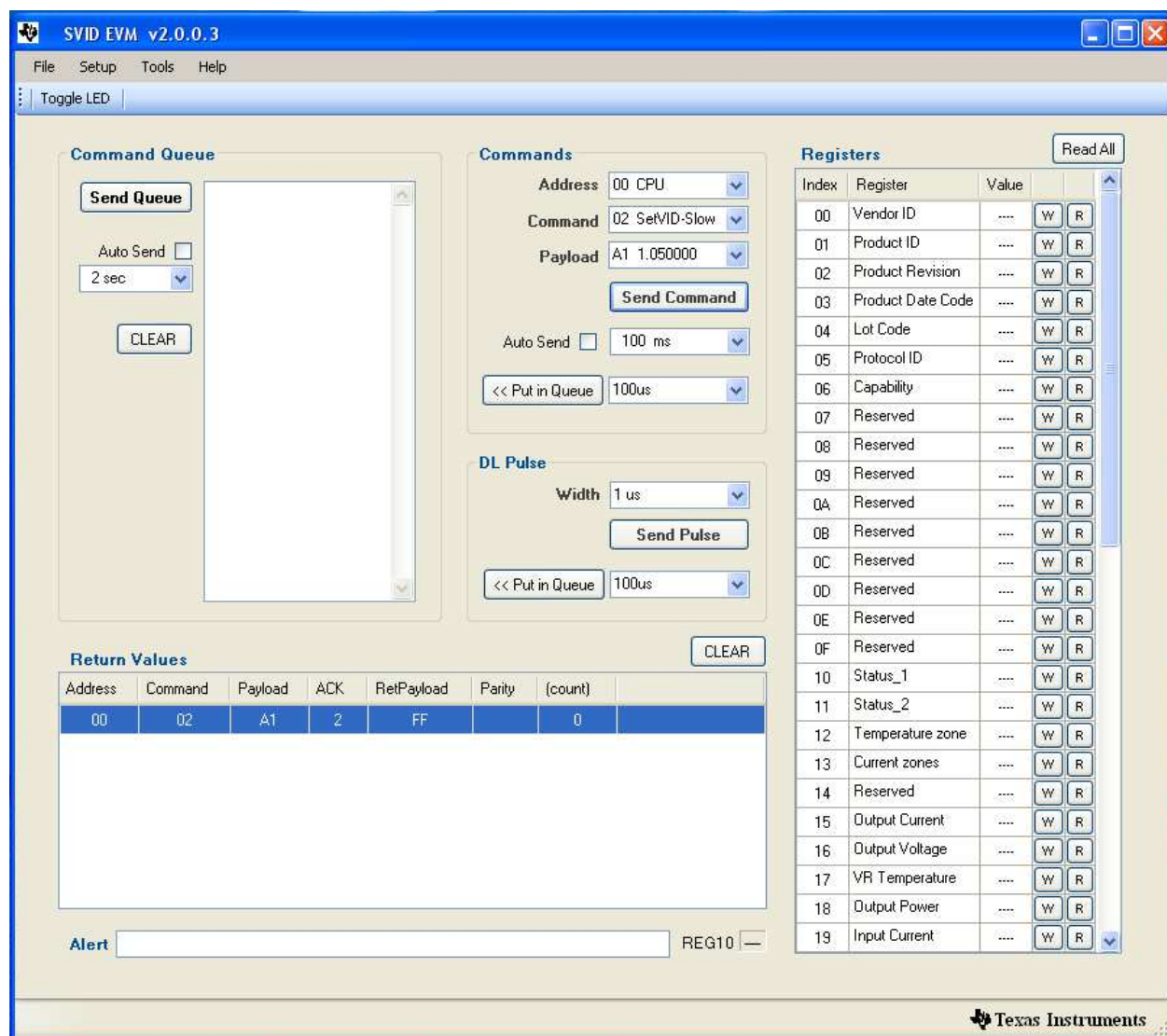


Figure 5. TPS59650EVM-753 CPU GUI set up Window

6.1.2 GPU

1. Connect the LOAD to GPU terminal J4, J5 and V3 at J9. Ensure correct polarity.
2. Add scope probe on the TP46 for GPU Vcore_G ripple measurement
3. Push S4 to "ON" position to enable the VR_ON of TPS59650. The VR_ON LED will light up.
4. Now you are ready to send SVID commands for GPU. Using pull-down menu:
Address: **01 GPU**, Command: SetVIDslow, Payload: **1.23V**
5. Click "send Command" and GPU GPOOD LED will light up, See the GUI window as Figure 6.

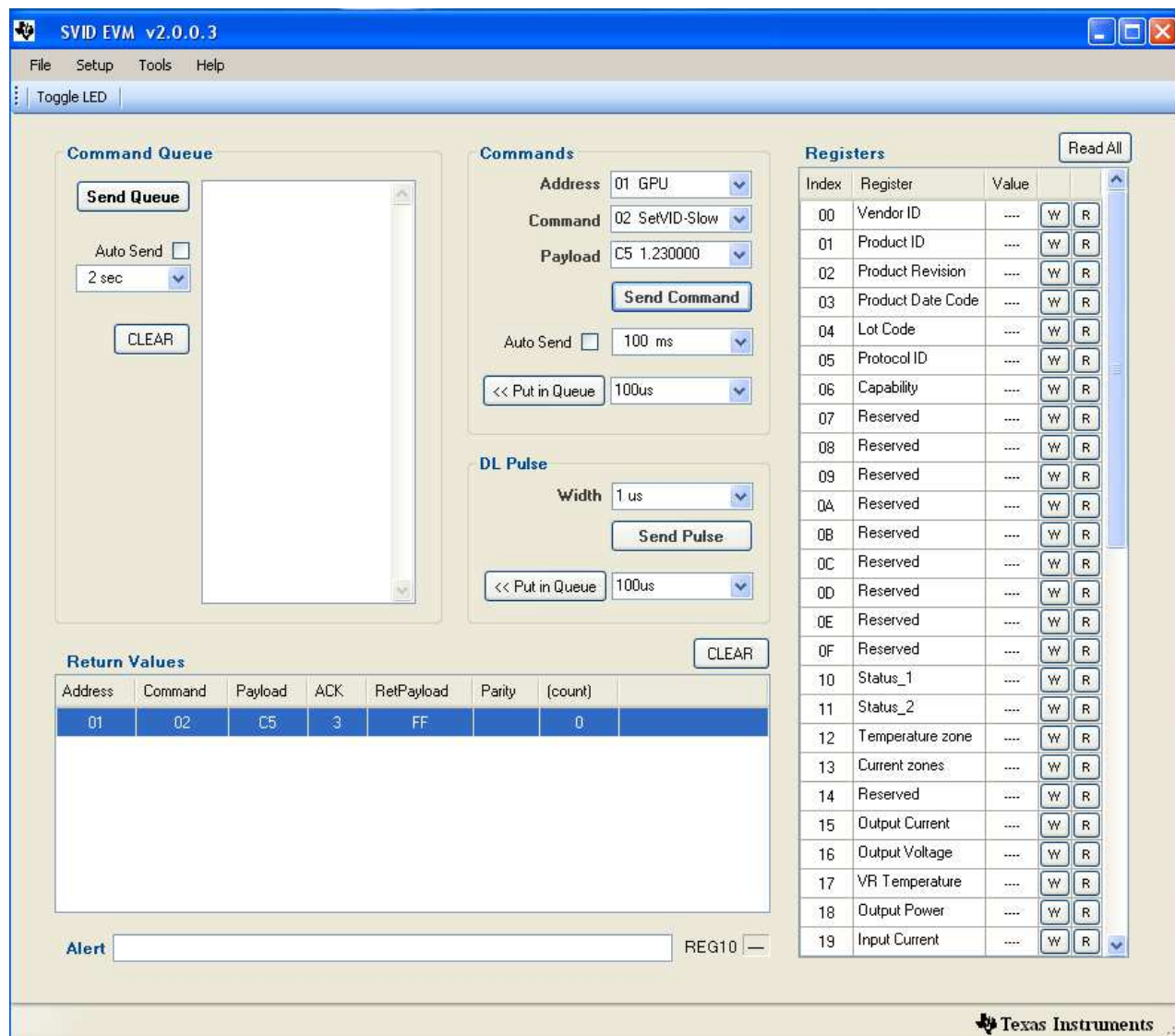


Figure 6. TPS59650EVM-753 GPU GUI set up Window

6. Measure V3: GPU Vcore_G at J9 and A1: 12VBAT input current
7. Vary GPU LOAD from 0Adc to 50Adc, GPU Vcore must remain in load line
8. Vary 12VBAT from 9V to 20V GPU Vcore must remain in line regulation
9. Push S4 to "OFF" position to disable GPU Vcore controller.
10. Decrease LOAD to 0A and disconnect the LOAD from terminal J11
11. Disconnect V3 from J9.
12. Disconnect scope probe from TP46
13. Exit SVID GUI window: click File → click Exit
14. Disconnect the USB cable between host Computer and EVM

6.1.3 VDDQ

1. Connect the LOAD to VDDQ terminal J19 and V3 at J20. Ensure correct polarity.
2. Remove Jumper from J17, J18 from pin2 and pin3 and put this Jumper on pin1 and pin 2 of J18, J17 to enable S5 of VDDQ controller. VDDQ PGOOD LED will light up.
3. Measure V3: VDDQ at J20 and A1: 12Vin input current
4. Vary VDDQ LOAD from 0Adc to 8Adc, VDDQ must remain in the load regulation
5. Vary 12VBAT from 9V to 20V, VDDQ must remain in the line regulation
6. Remove Jumper of J17, J18 and shorts back on pin2 and pin3 of J17, J18 to disable VDDQ controller.
7. Decrease LOAD to 0A and disconnect the LOAD from terminal J19
8. Disconnect V3 from J20.

6.1.4 VCCIO

1. Connect the LOAD to VCCIO terminal J15 and V3 at J16. Ensure correct polarity.
2. Push S1 to "ON" position to enable the VCCIO controller. VCCIO EN and PGOOD LED will light up.
3. Measure V3: VCCIO at J16 and A1: 12Vin input current
4. Vary VDDQ LOAD from 0Adc to 10Adc, VCCIO must remain in the load regulation
5. Vary 12VBAT from 9V to 20V, VCCIO must remain in the line regulation
6. Push S1 to "OFF" position to disable VCCIO controller.
7. Decrease LOAD to 0A and disconnect the LOAD from terminal J15
8. Disconnect V3 from J16.

6.2 Equipment Shutdown

1. Shut down Load
2. Shut down 12VBAT and 5Vin
3. Shut down oscilloscope
4. Shut down host computer

7 Performance Data and Typical Characteristic Curves

Figure 7 through Figure 91 present typical performance curves for TPS59650EVM-753. Jumpers set to default locations, see section 6 of this user's guide.

7.1 CPU 3-Phase Operation

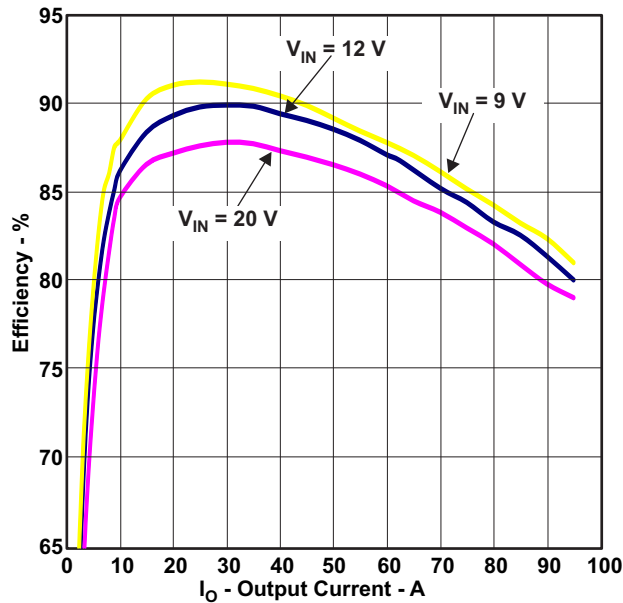


Figure 7. CPU3 Efficiency

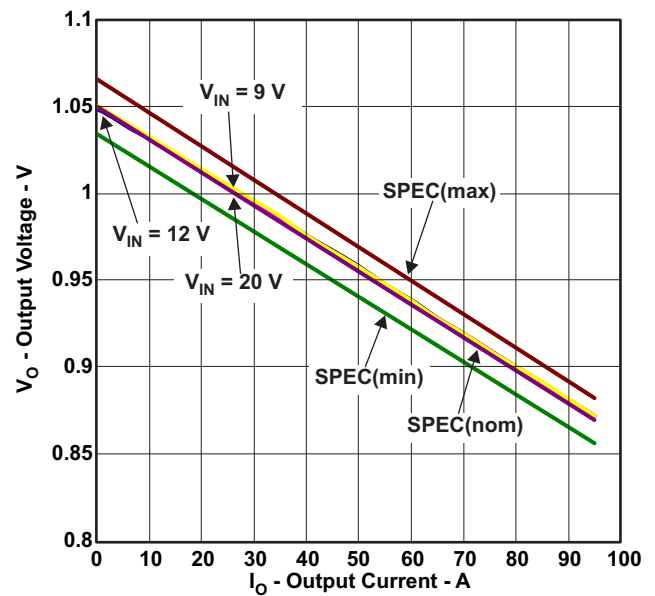


Figure 8. CPU3 Load regulation

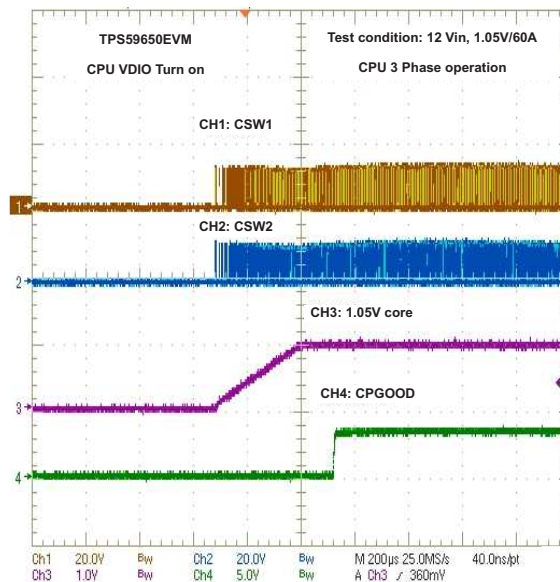


Figure 9. CPU3 Enable Turn on

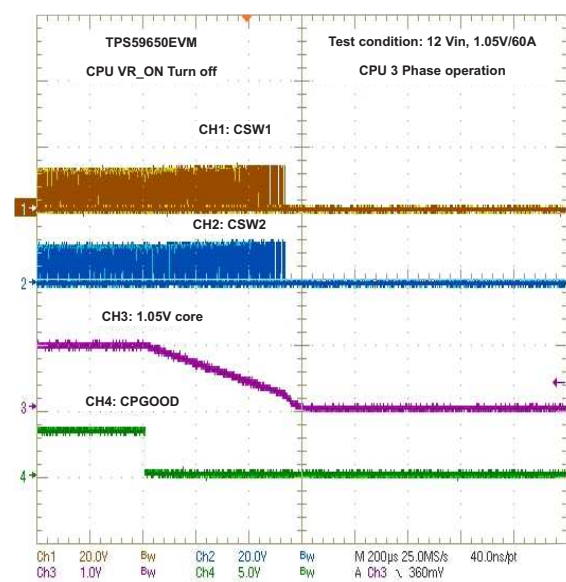


Figure 10. CPU3 Enable Turn off

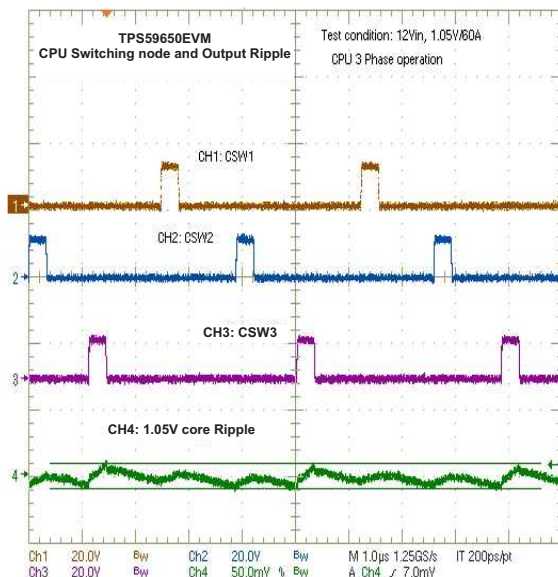


Figure 11. CPU3 Switching Node(Ripple)

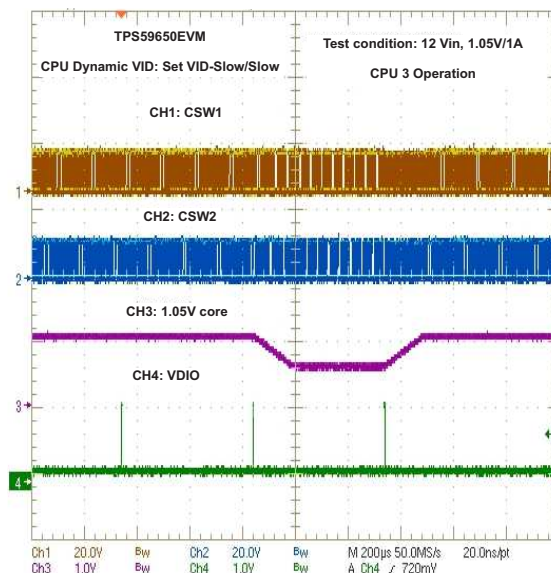


Figure 12. CPU3 Dynamic VID: SetVID-Slow/Slow

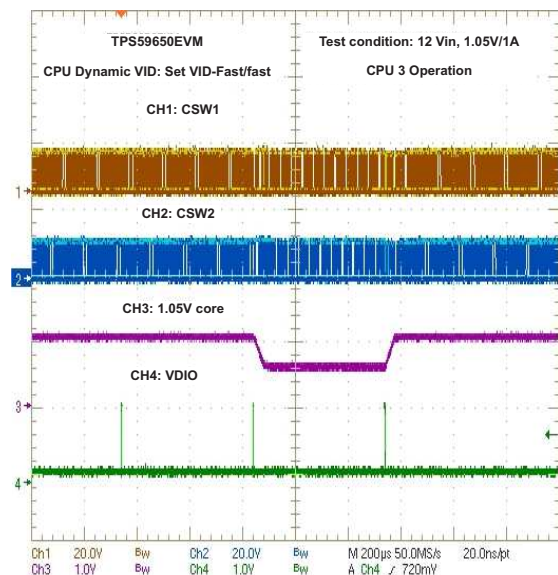


Figure 13. CPU3 Dynamic VID:SetVID-Fast/Fast

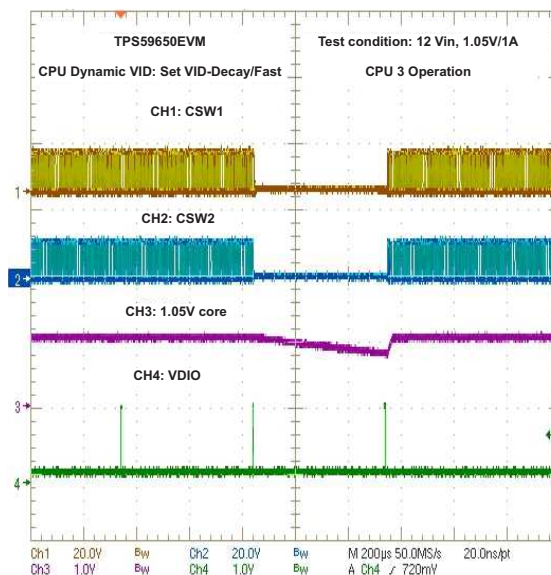


Figure 14. CPU3 Dynamic VID:SetVID-Decay/Fast

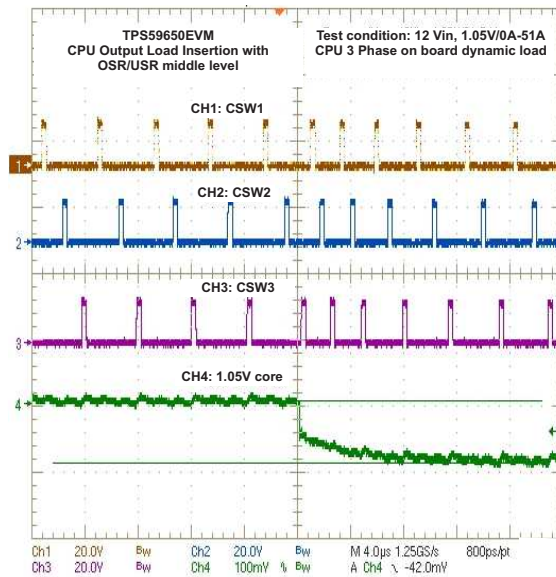


Figure 15. CPU3 Output Load Insertion with OSR/USR middle level

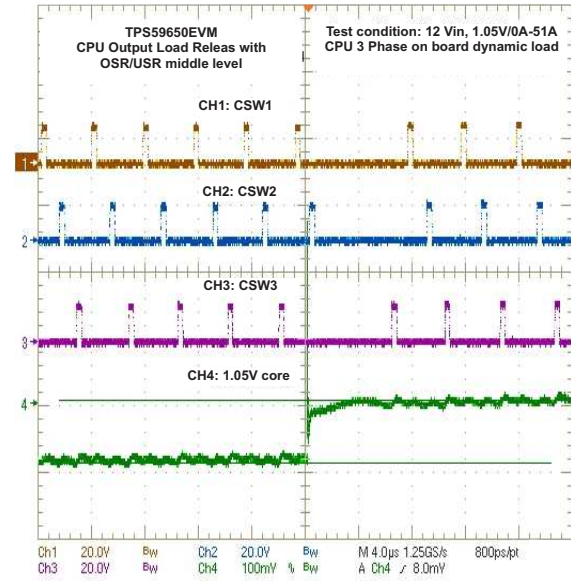


Figure 16. CPU3 Output Load Release with OSR/USR middle level

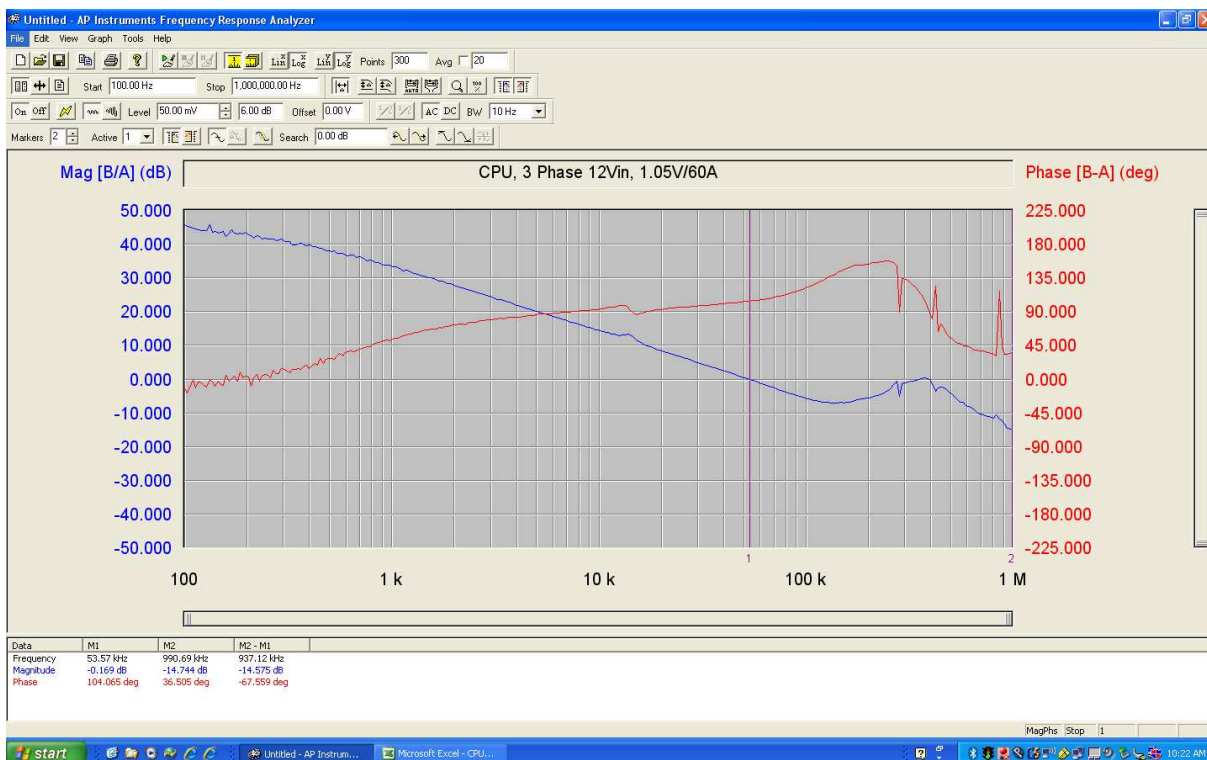


Figure 17. CPU3 Bode Plot at 12Vin, 1.05V/60A

Test condition: CPU3 12Vin, 1.05V/60A no airflow

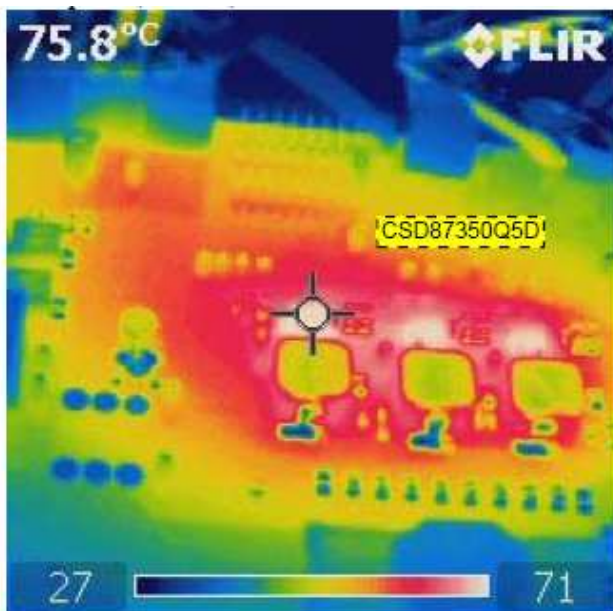


Figure 18. CPU3 MOSFET

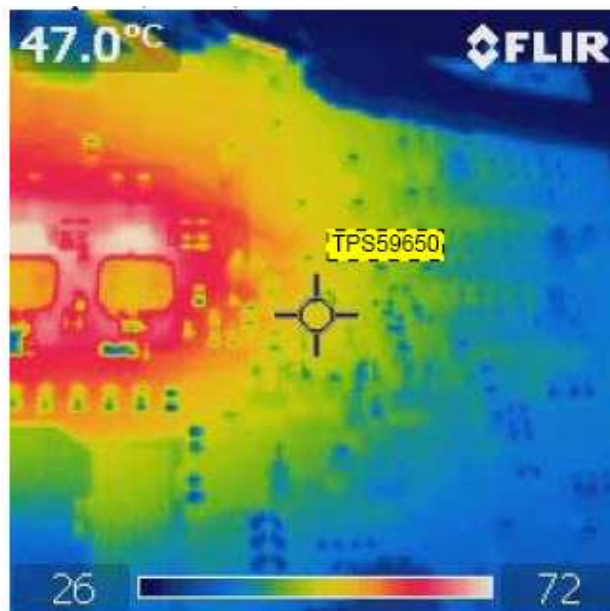


Figure 19. CPU3 IC

7.2 CPU 2-Phase Operation

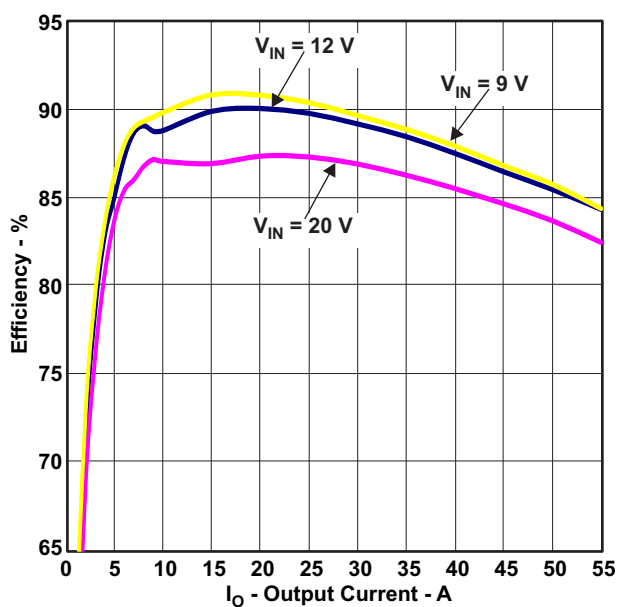


Figure 20. CPU2 Efficiency

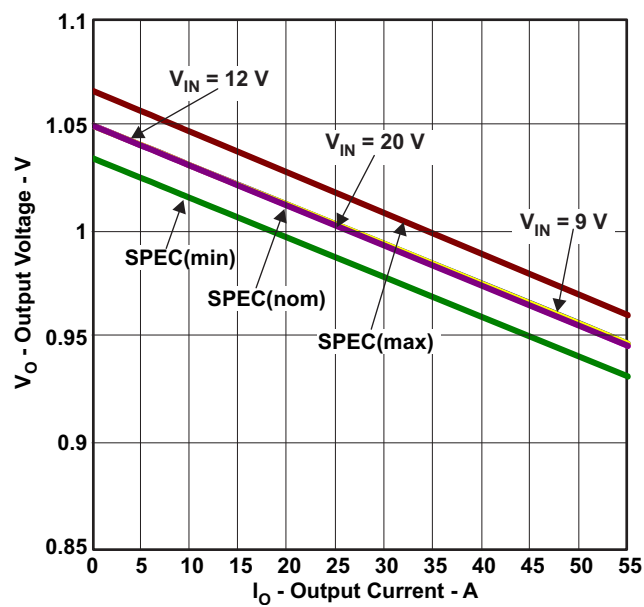


Figure 21. CPU2 Load regulation

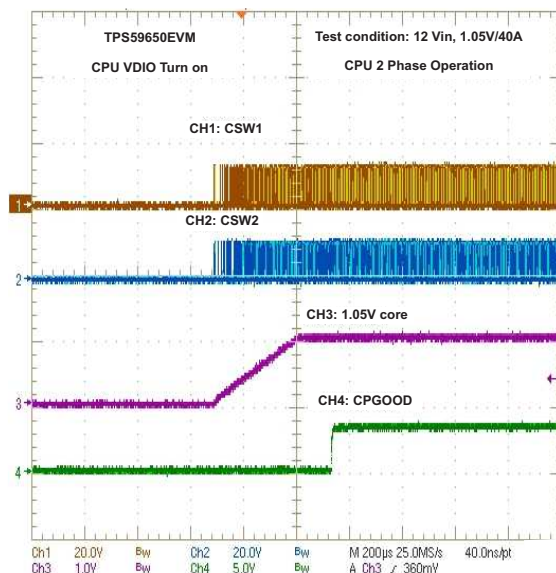


Figure 22. CPU2 Enable Turn on

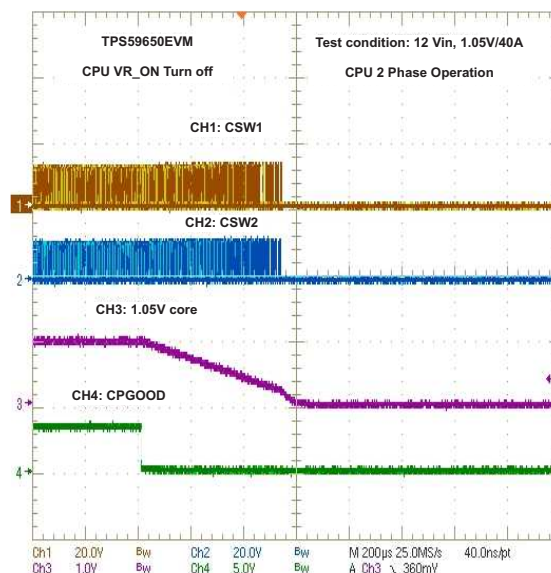


Figure 23. CPU2 Enable Turn off

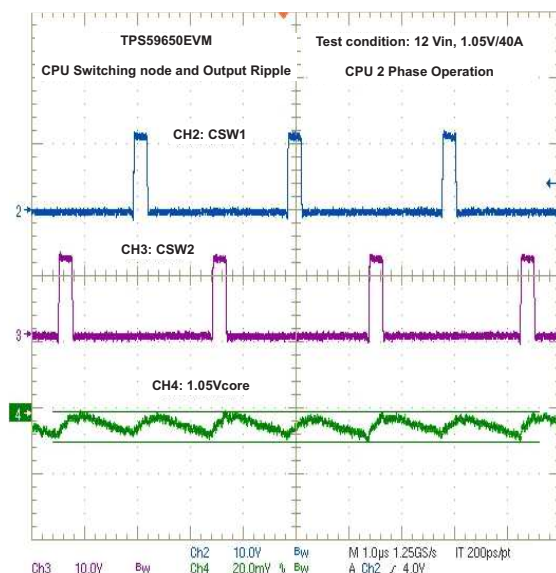


Figure 24. CPU2 Switching Node(Ripple)

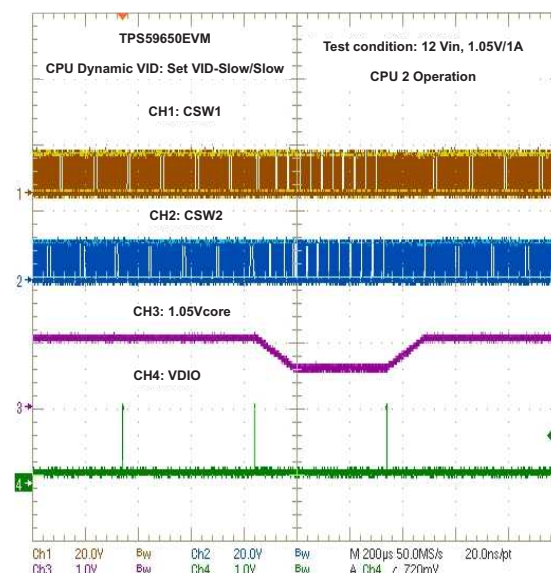


Figure 25. CPU2 Dynamic VID: SetVID-Slow/Slow

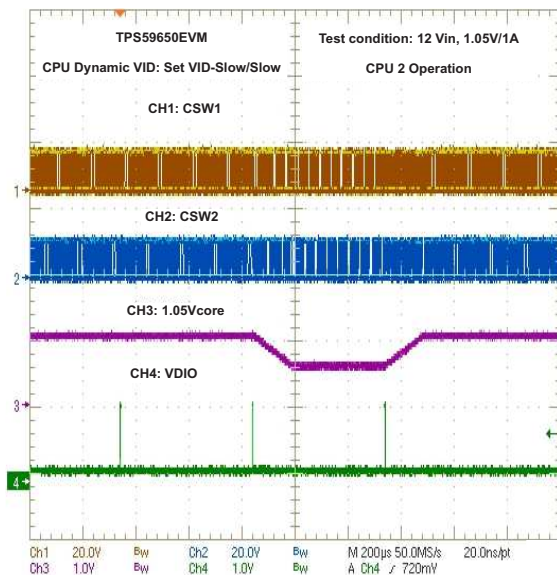


Figure 26. CPU2 Dynamic VID: SetVID-Slow/Slow

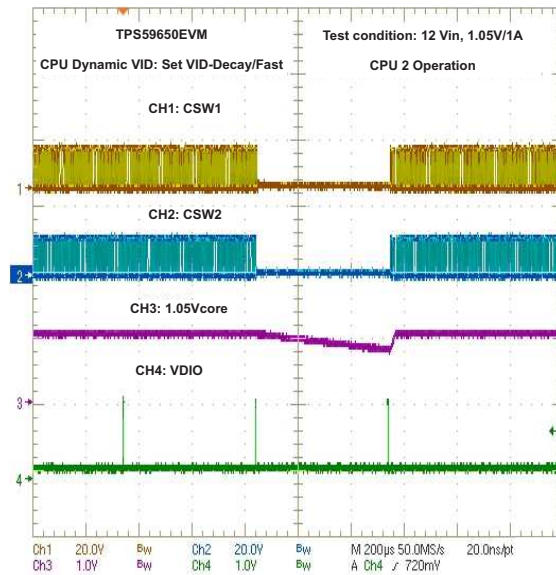


Figure 27. CPU2 Dynamic VID: SetVID-Decay/Fast

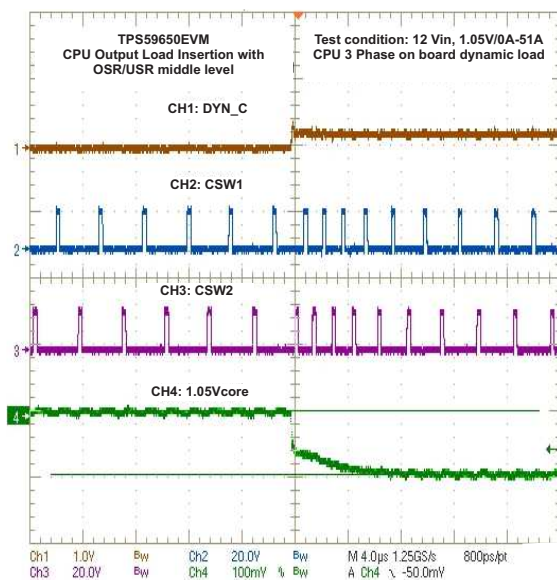


Figure 28. CPU2 Output Load Insertion with OSR/USR middle level

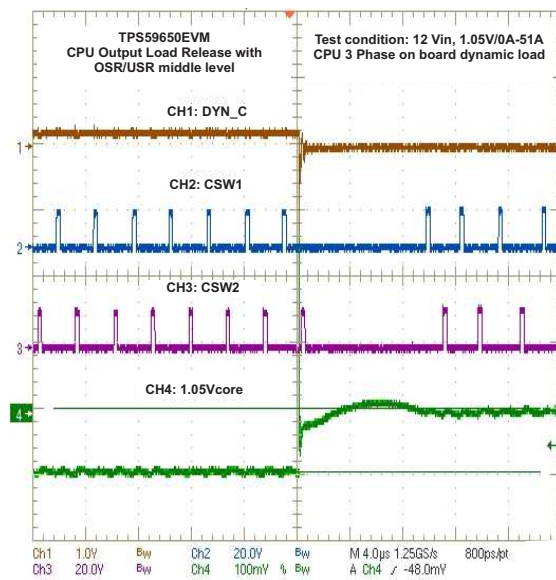


Figure 29. CPU2 Output Load Release with OSR/USR middle level

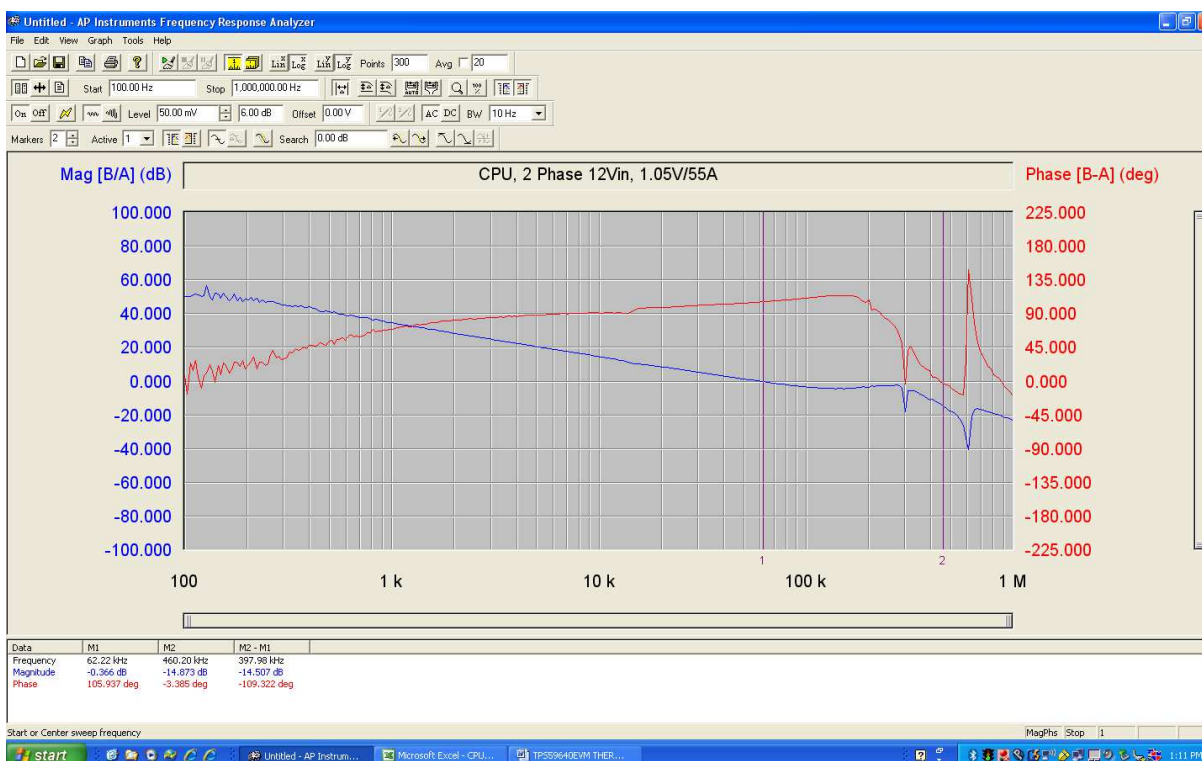


Figure 30. CPU2 Bode Plot at 12Vin, 1.05V/55A

Test condition: CPU2 12Vin, 1.05V/55A no airflow

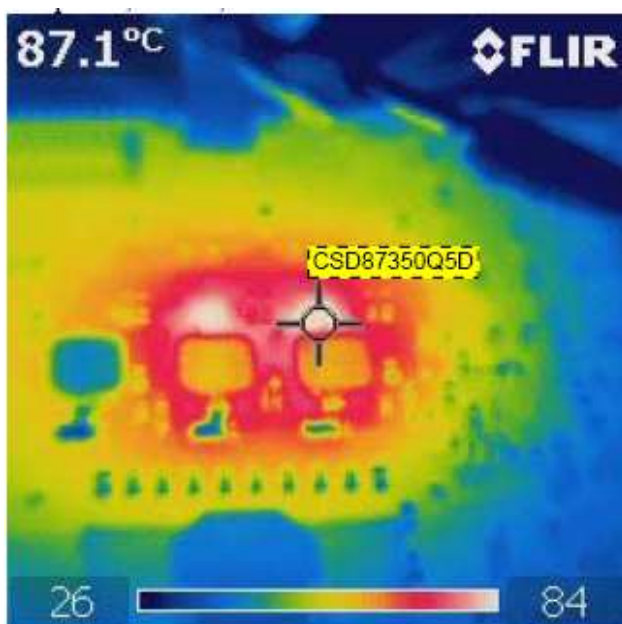


Figure 31. CPU2 MOSFET

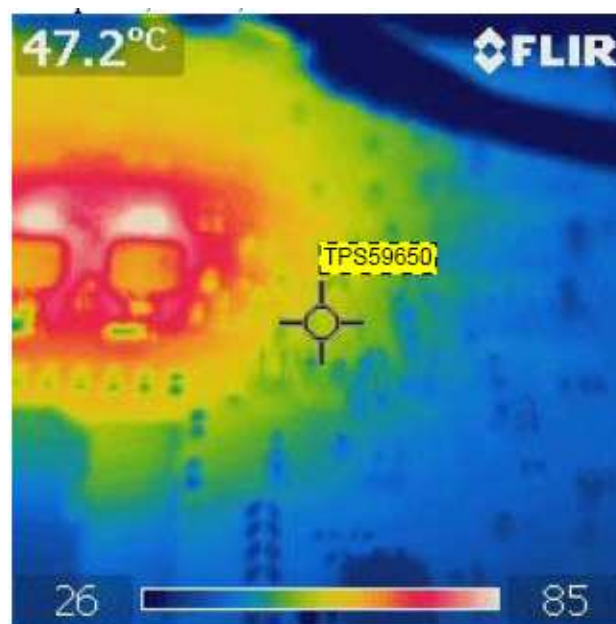


Figure 32. CPU2 IC

7.3 CPU1-Phase Operation

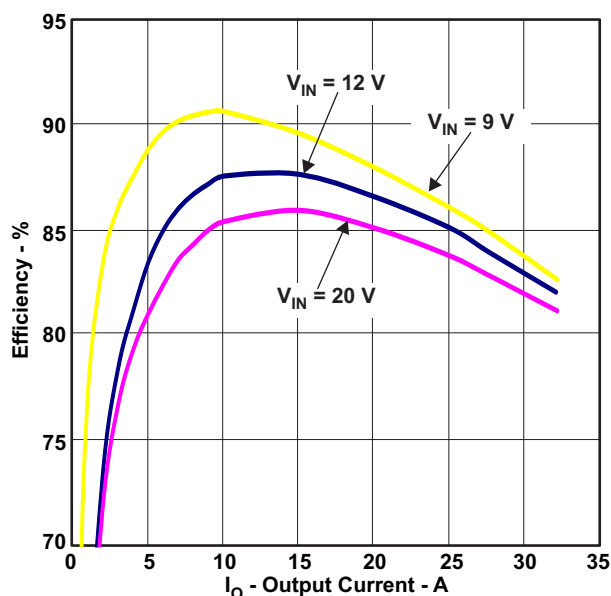


Figure 33. CPU1 Efficiency

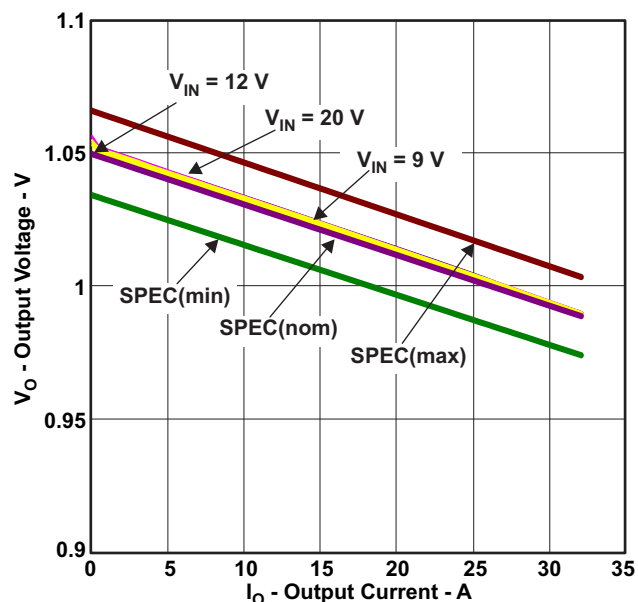


Figure 34. CPU1 Load regulation

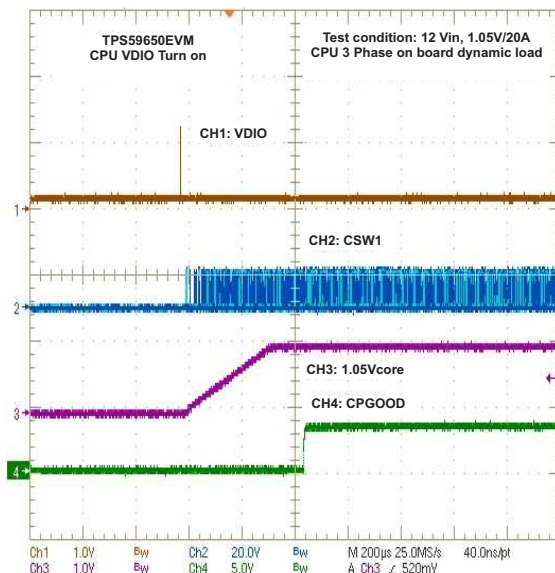


Figure 35. CPU1 Enable Turn on

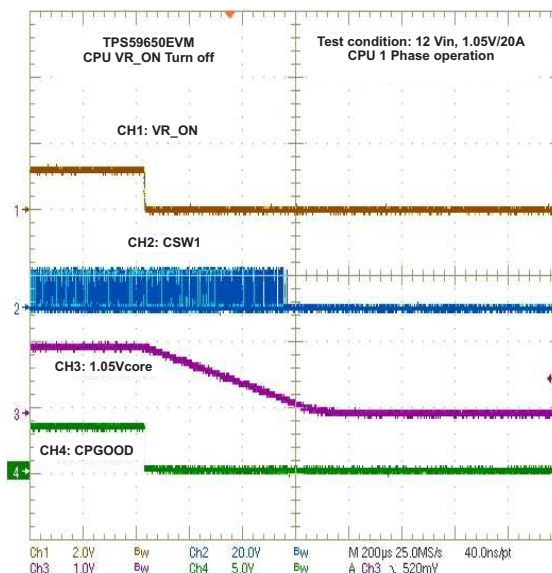


Figure 36. CPU1 Enable Turn off

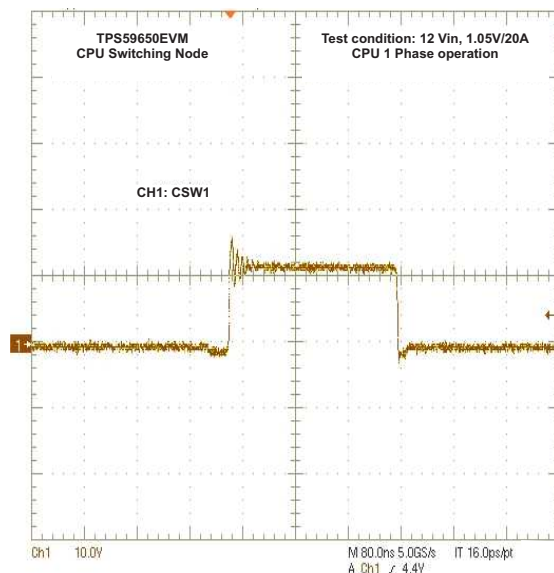


Figure 37. CPU1 Switching Node

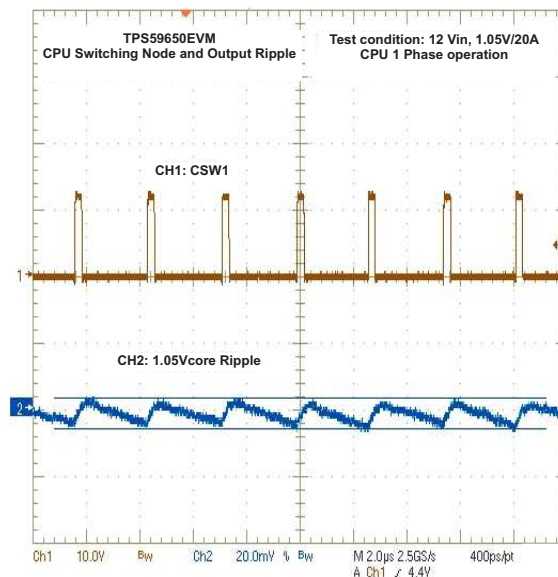


Figure 38. CPU1 Switching node and Ripple

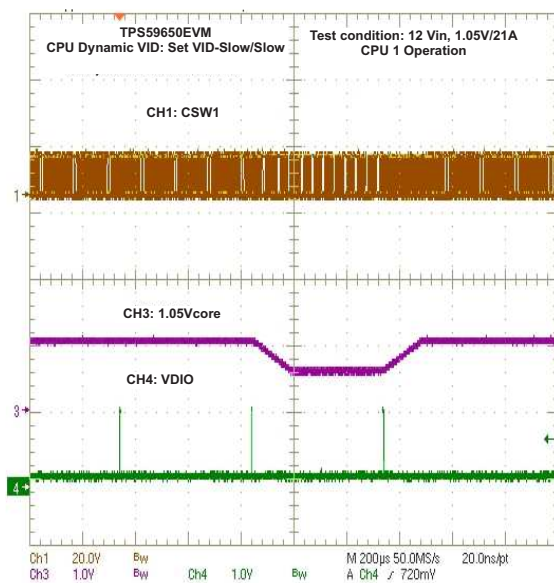


Figure 39. CPU1 Dynamic VID: SetVID-Slow/Slow

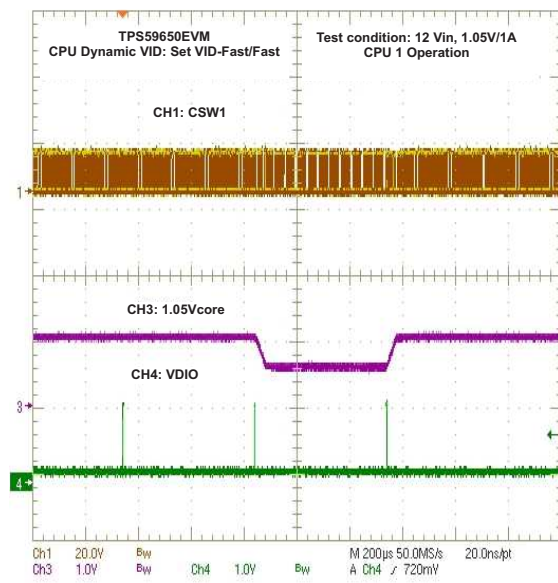


Figure 40. CPU1 Dynamic VID: SetVID-Fast/Fast

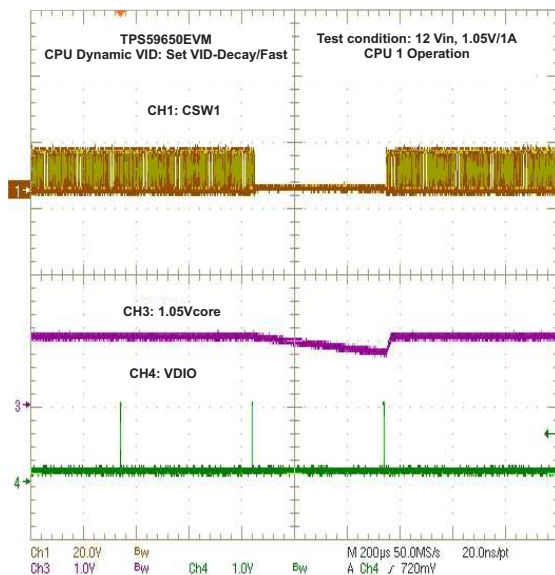


Figure 41. CPU1 Dynamic VID: SetVID-Decay/Fast

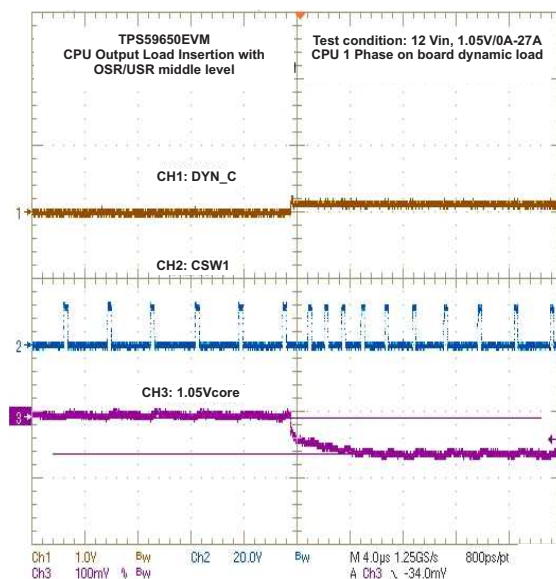


Figure 42. CPU1 Output Load Insertion with OSR/USR middle level

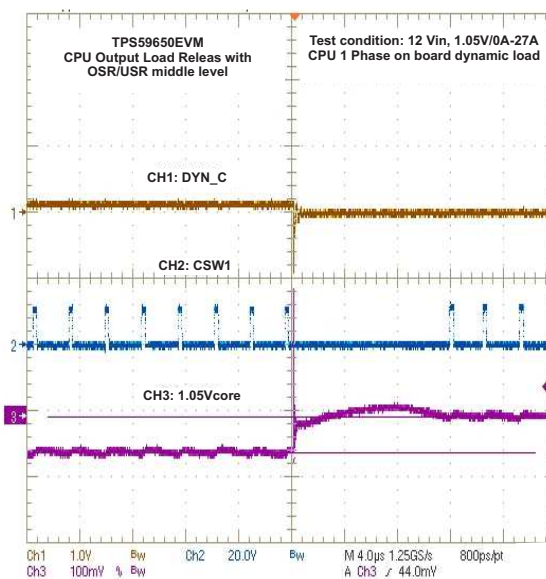


Figure 43. CPU1 Output Load Release with OSR/USR middle level

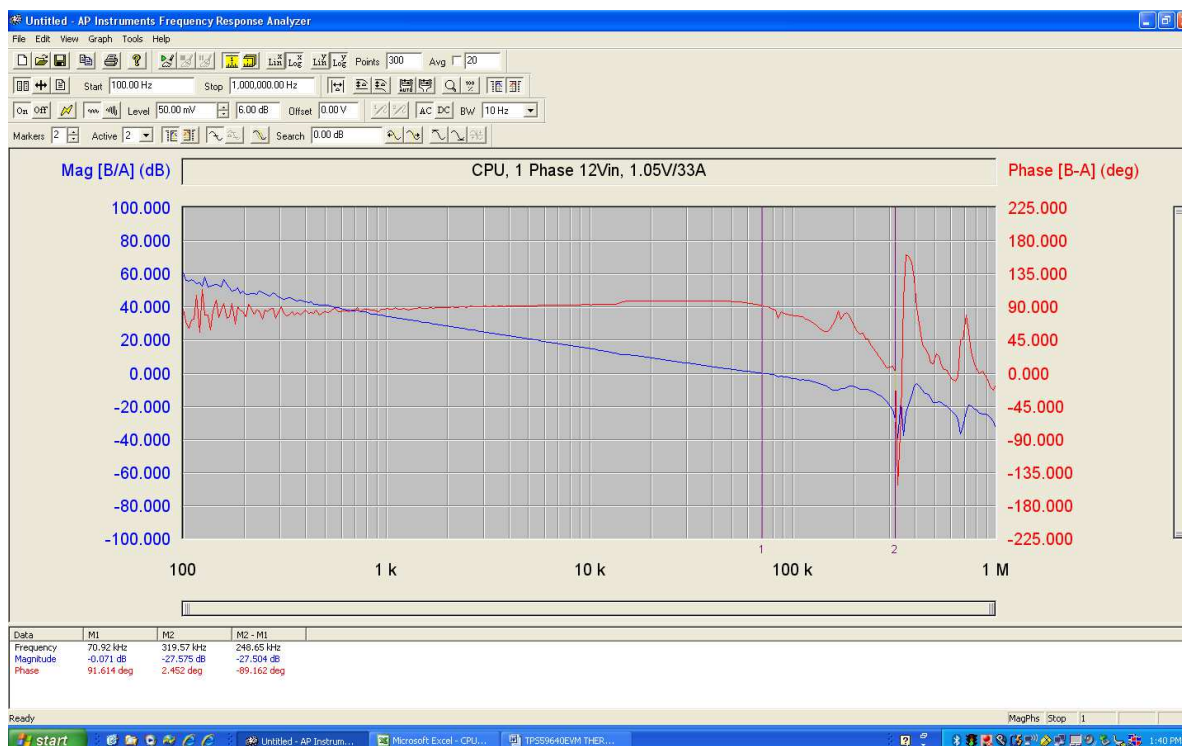


Figure 44. CPU1 Bode Plot at 12Vin, 1.05V/33A

Test condition: CPU1 12Vin, 1.05V/33A no airflow

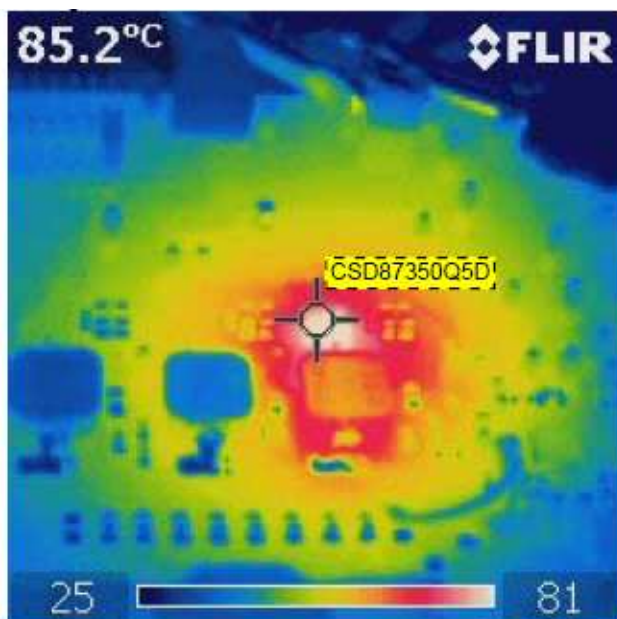


Figure 45. CPU1 MOSFET

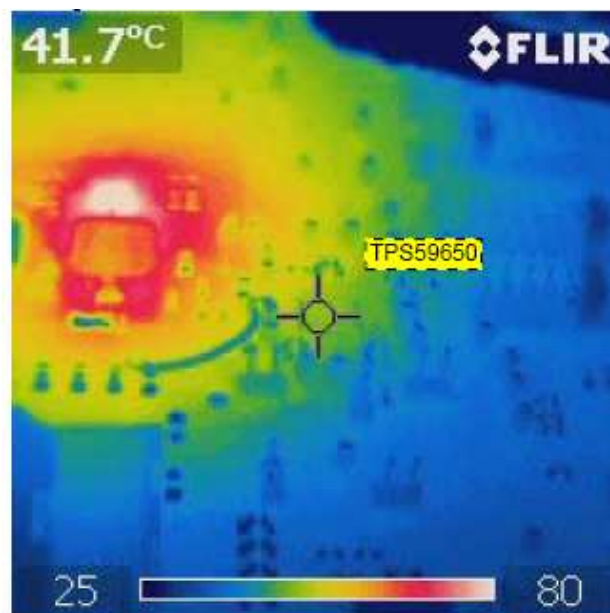


Figure 46. CPU1 IC

7.4 GPU 2 Phase Operation

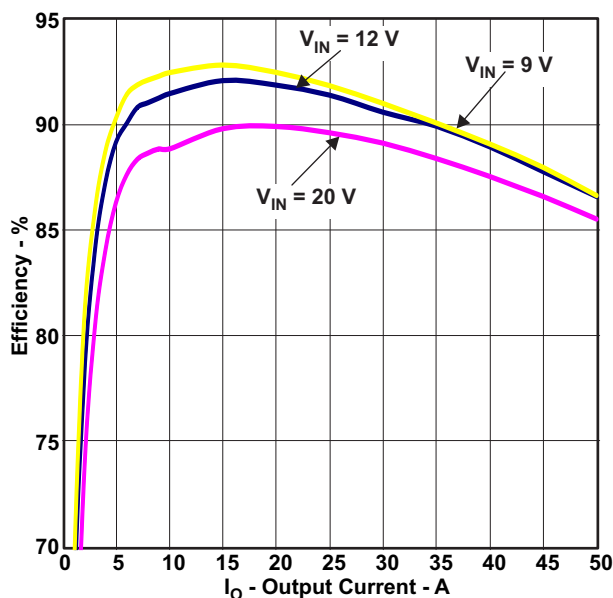


Figure 47. GPU2 Efficiency

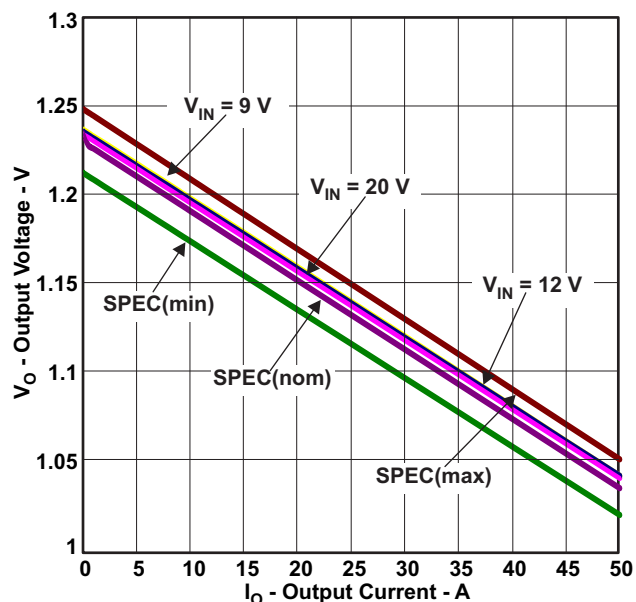


Figure 48. GPU2 Load regulation

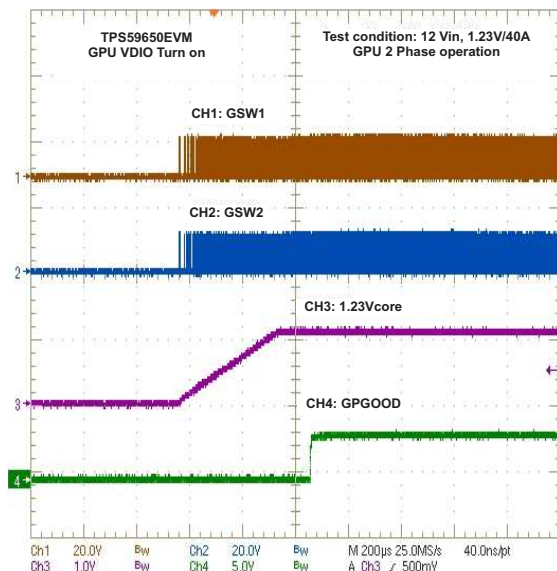


Figure 49. GPU2 Enable Turn on

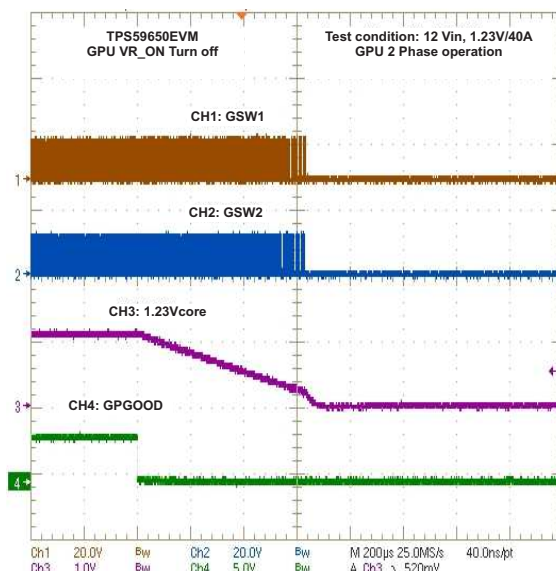


Figure 50. GPU2 Enable Turn off

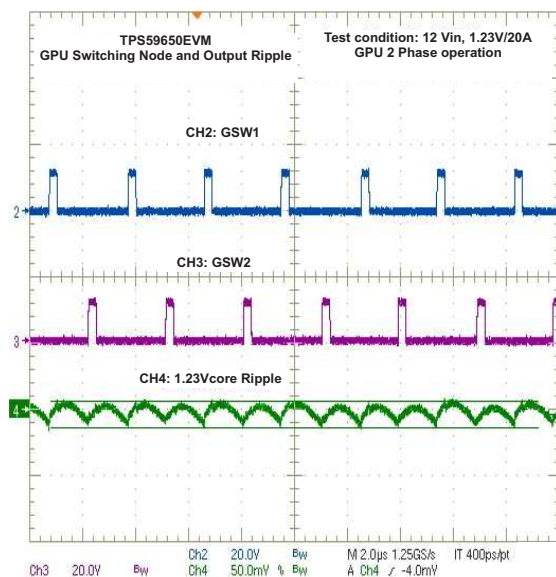


Figure 51. GPU2 Switching Node and Ripple

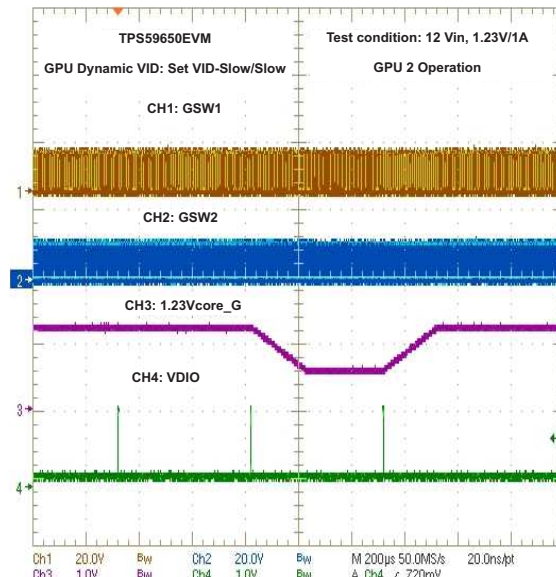


Figure 52. GPU2 Dynamic VID: Set VID-Slow/Slow

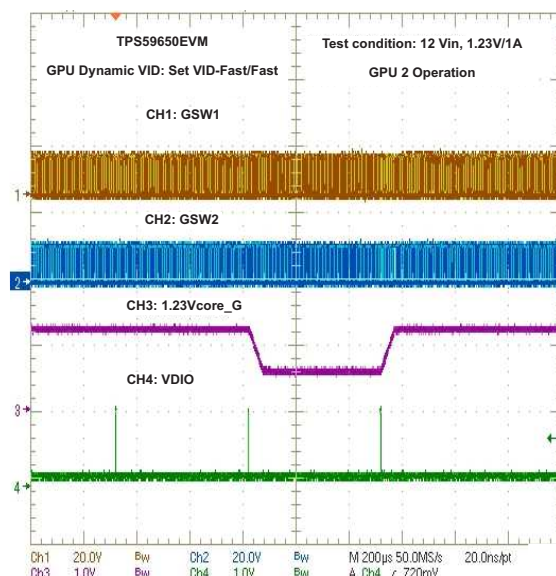


Figure 53. GPU2 Dynamic VID: Set VID-Fast/Fast

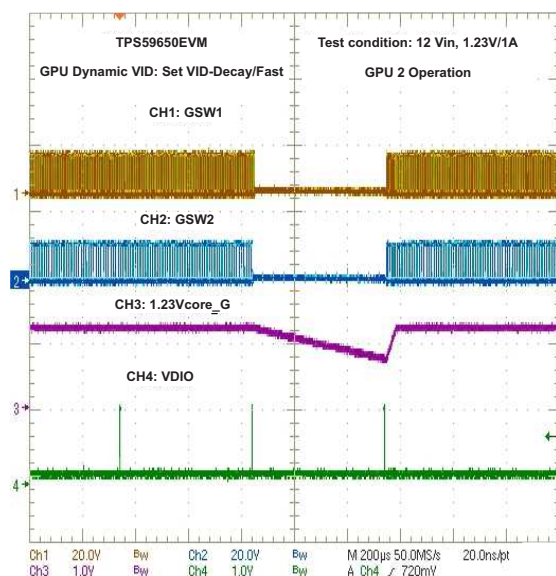


Figure 54. GPU2 Dynamic VID: Set VID-Decay/Fast

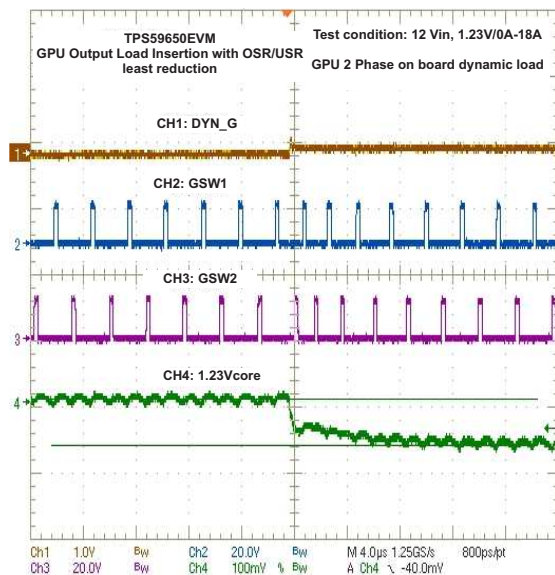


Figure 55. GPU2 Output Load Insertion with OSR/USR OFF

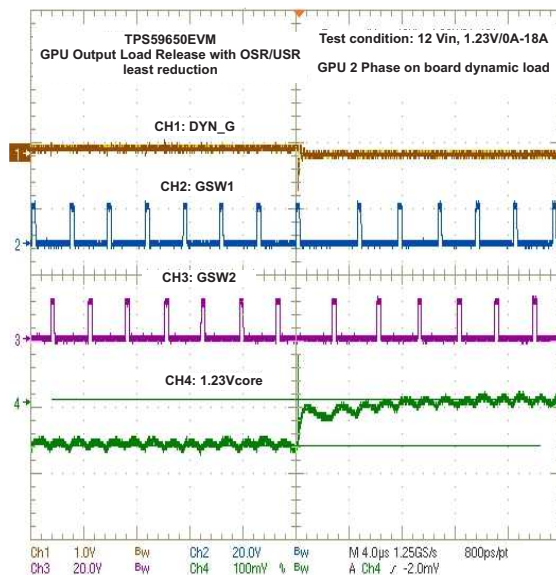


Figure 56. GPU2 Output Load Release with OSR/USR OFF

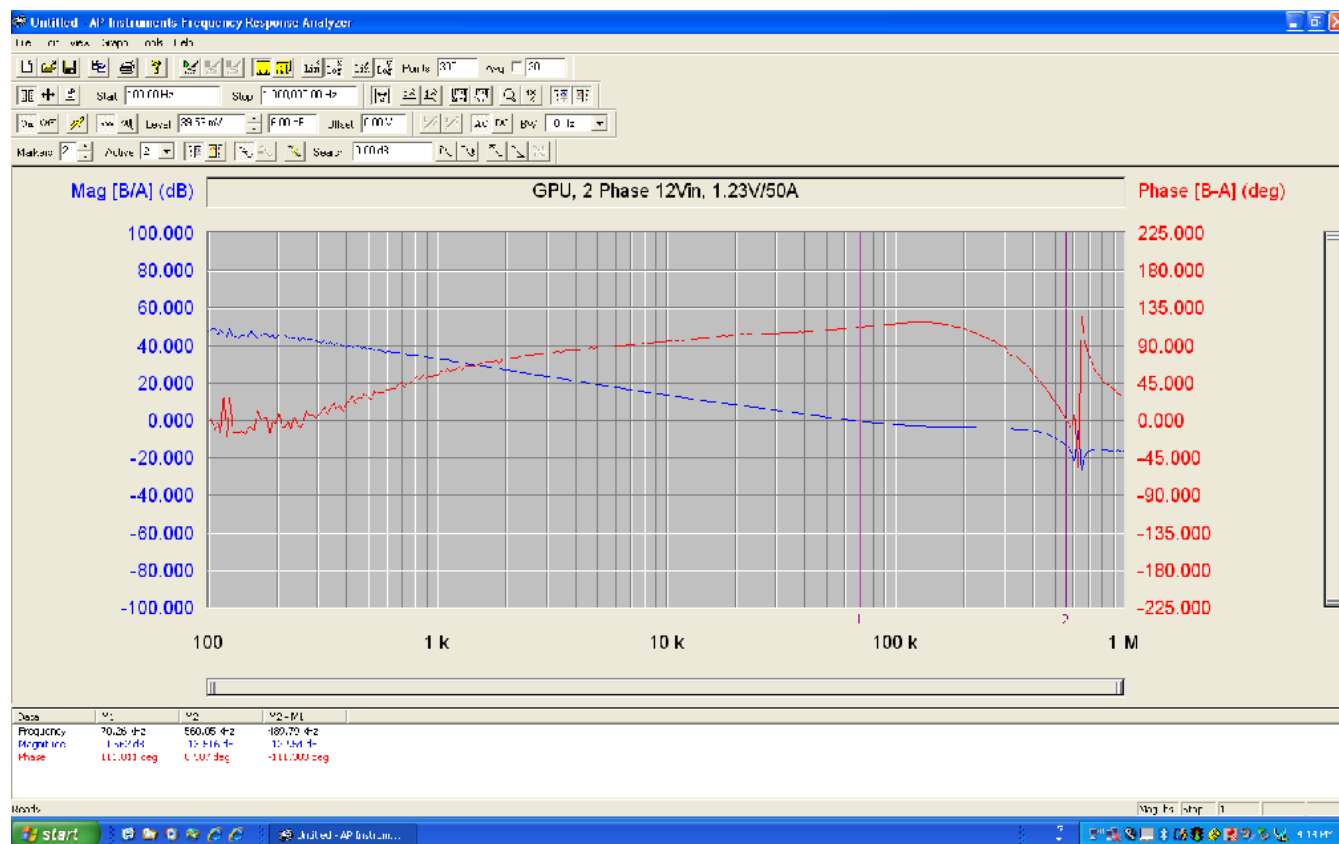


Figure 57. GPU2 Bode Plot at 12Vin, 1.23V/50A

Test condition: GPU2 12Vin, 1.23V/50A no airflow

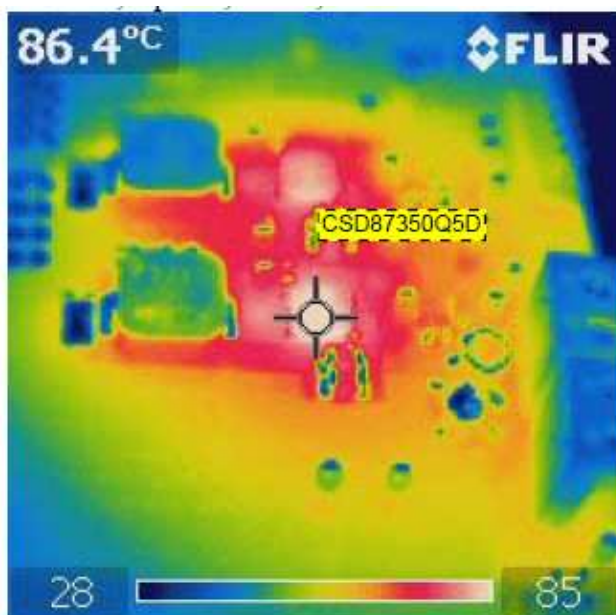


Figure 58. GPU2 MOSFET

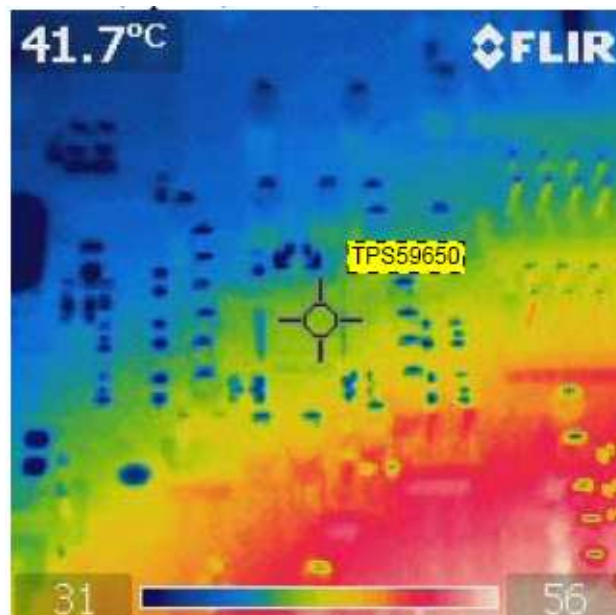


Figure 59. GPU2 IC

7.5 GPU 1 Phase Operation

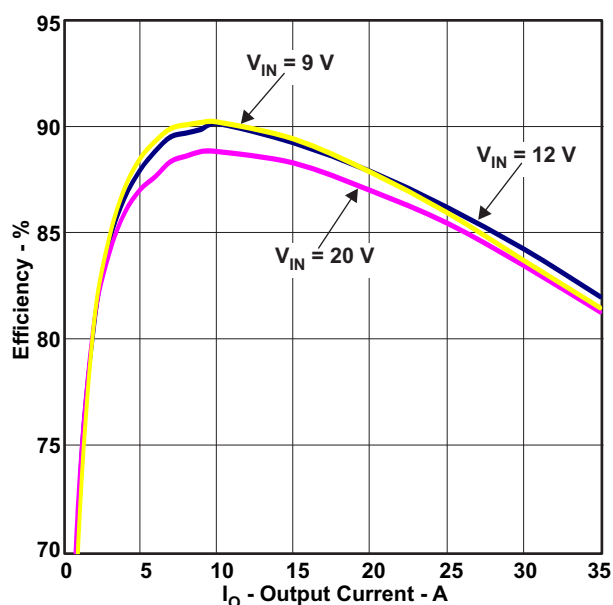


Figure 60. GPU1 Efficiency

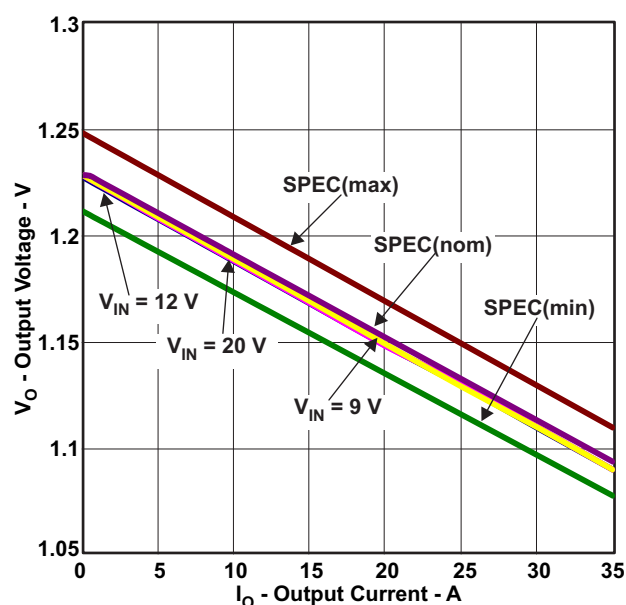


Figure 61. GPU1 Load regulation

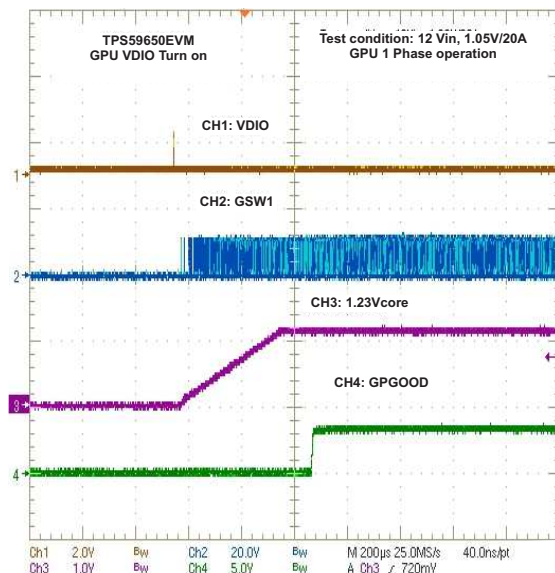


Figure 62. GPU1 Enable Turn on

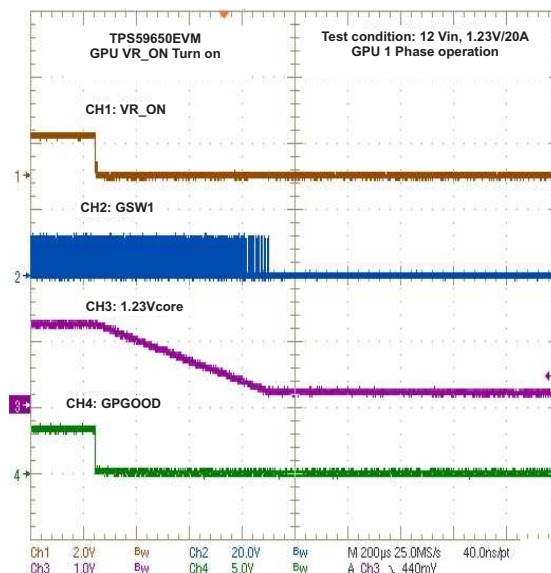


Figure 63. GPU1 Enable Turn off

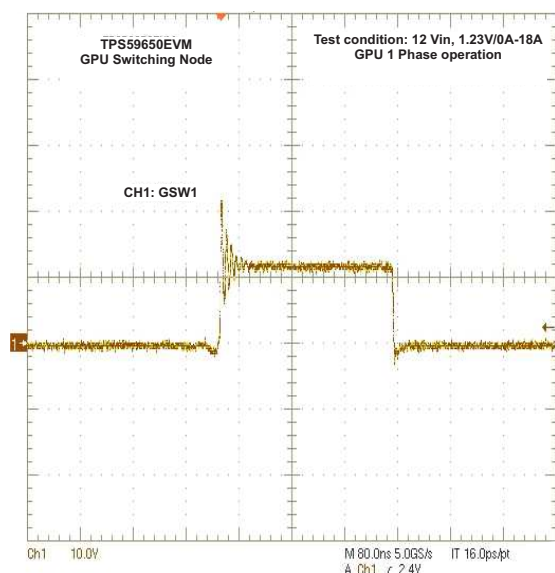


Figure 64. GPU1 Switching Node

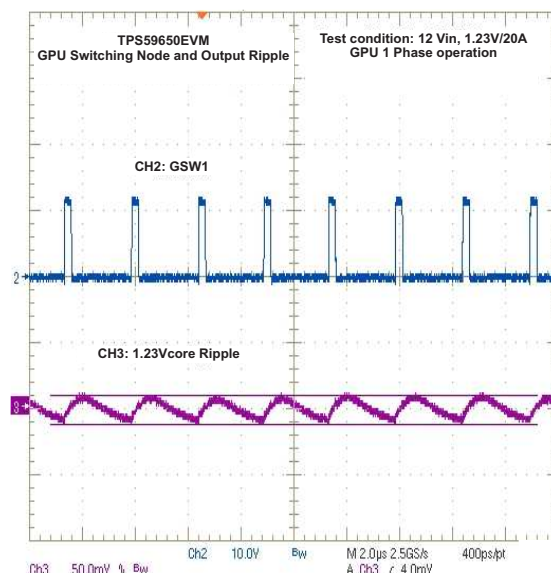


Figure 65. GPU1 Switching Node and Ripple

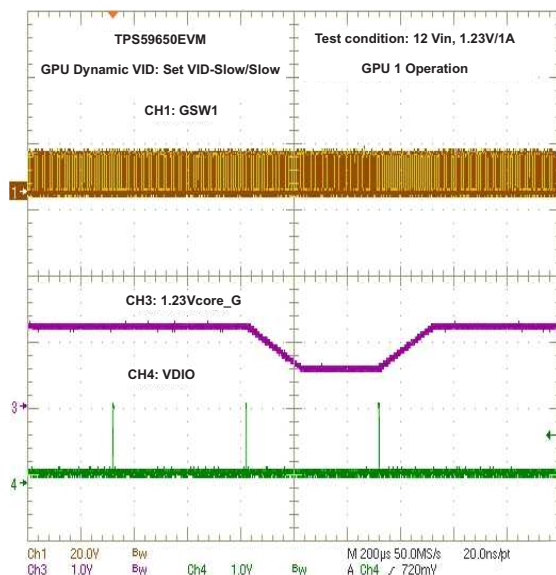


Figure 66. GPU1 Dynamic VID: SetVID-Slow/Slow

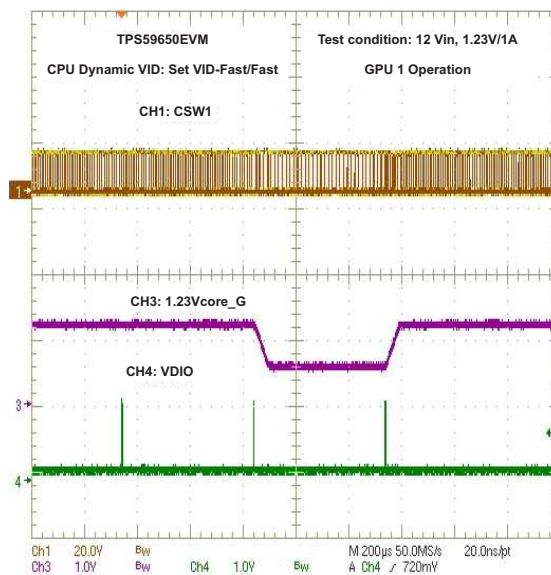


Figure 67. GPU1 Dynamic VID: SetVID-Fast/Fast

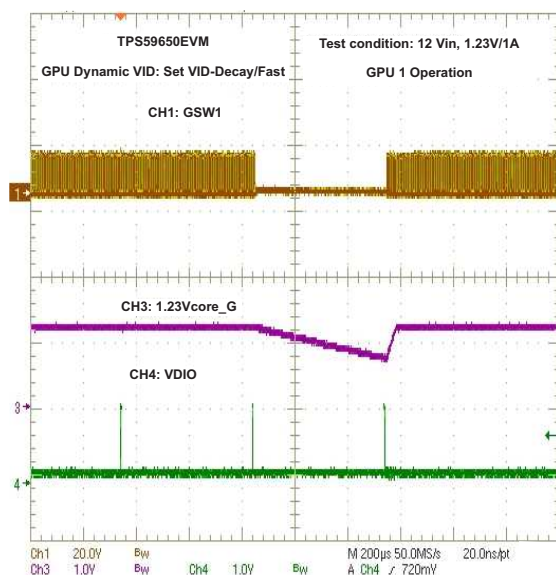


Figure 68. GPU1 Dynamic VID: SetVID-Decay/Fast

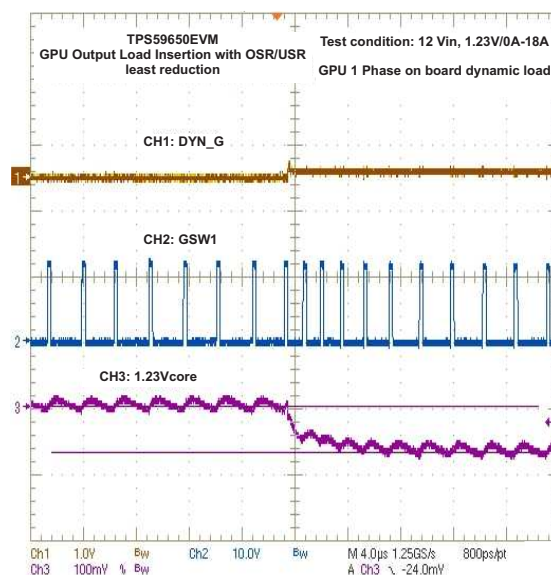


Figure 69. GPU1 Output Load Insertion with OSR/USR OFF

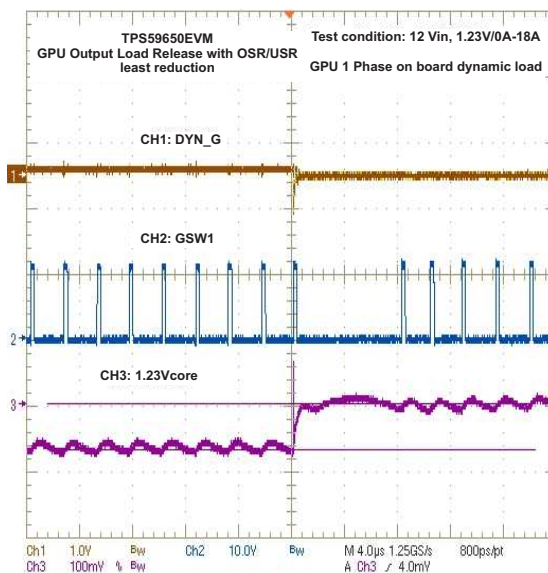


Figure 70. GPU1 Output Load Release with OSR/USR OFF



Figure 71. GPU1 Bode Plot at 12Vin, 1.23V/33A

Test condition: GPU1 12Vin, 1.23V/33A no airflow

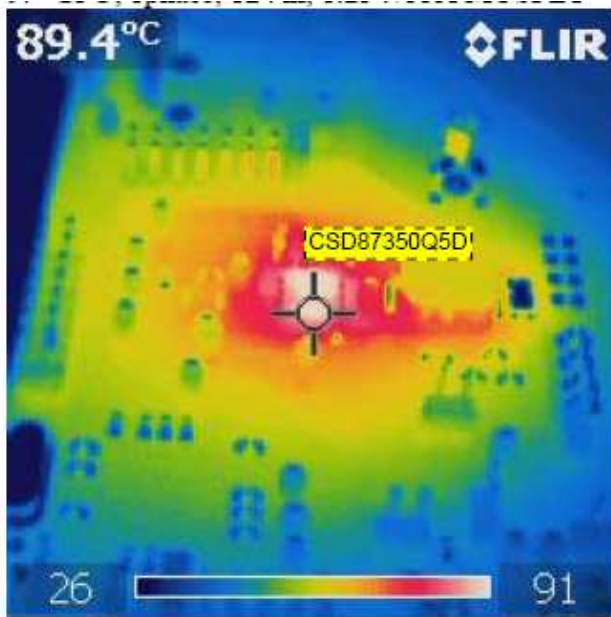


Figure 72. GPU1 MOSFET

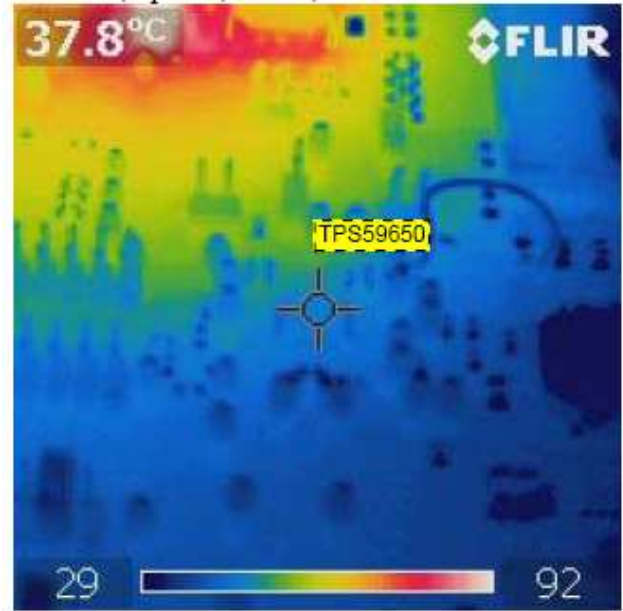


Figure 73. GPU1 IC

7.6 1.05V VCCIO

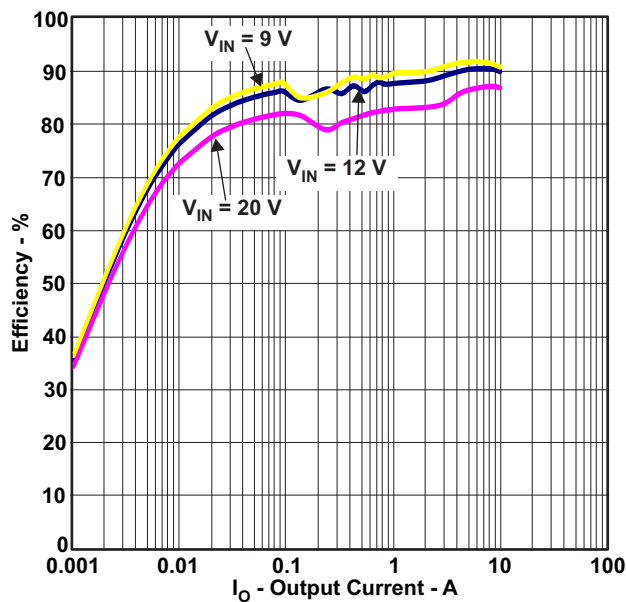


Figure 74. 1.05V Efficiency

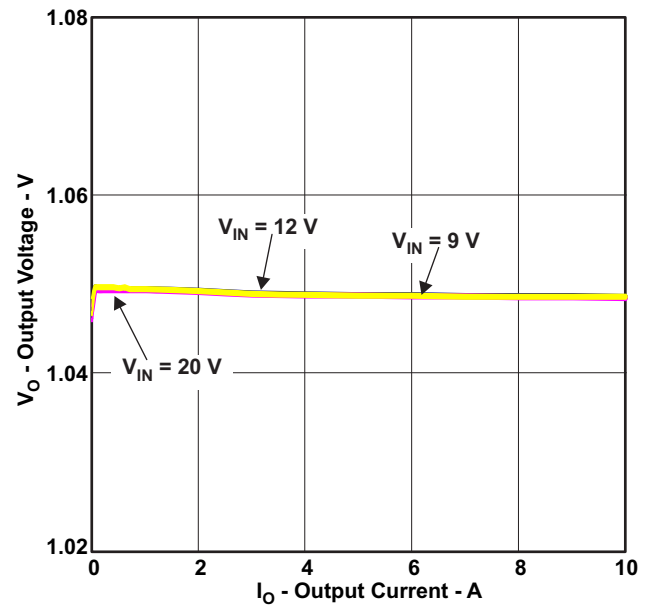


Figure 75. 1.05V Load regulation

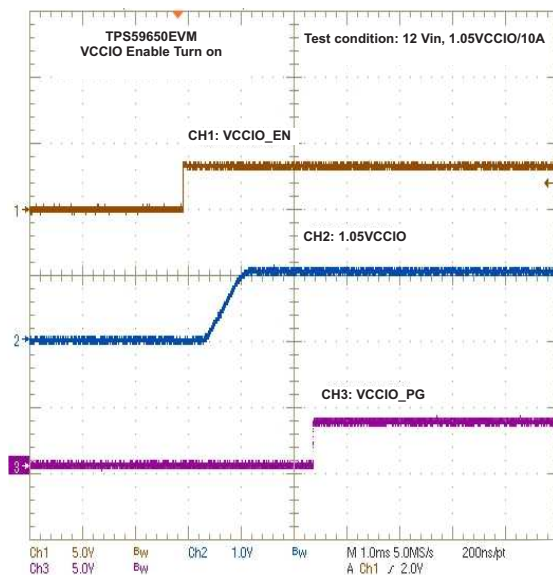


Figure 76. 1.05V Enable Turn on

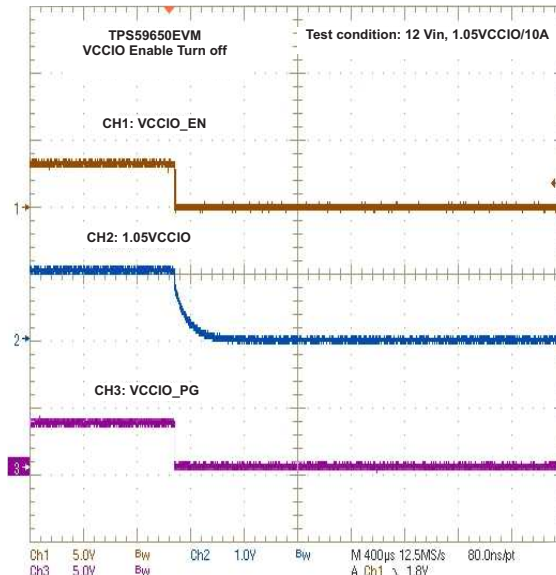


Figure 77. 1.05V Enable Turn off

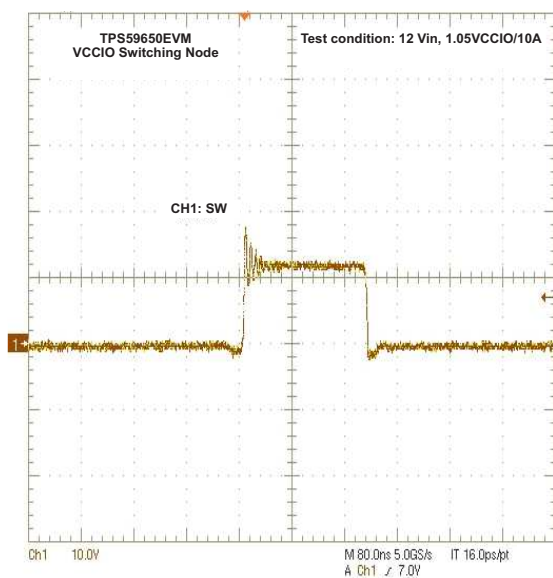


Figure 78. 1.05V Switching Node

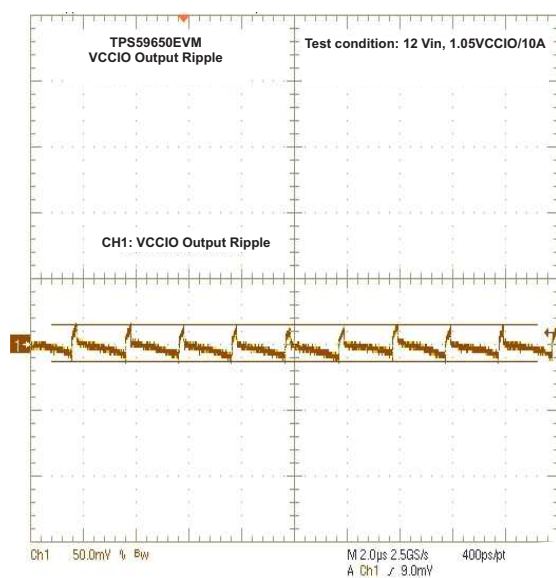


Figure 79. 1.05V Ripple

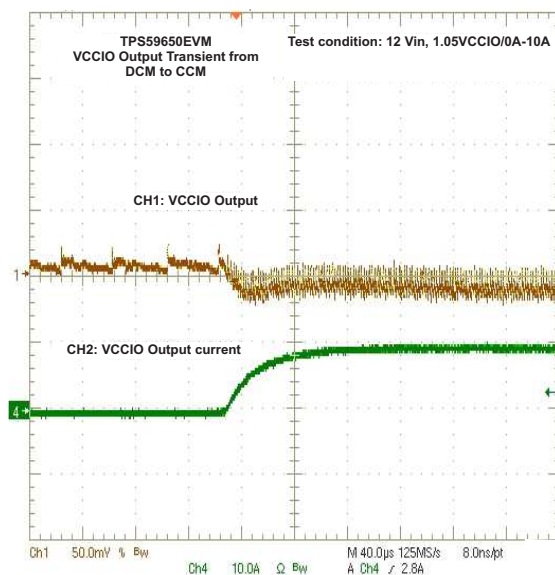


Figure 80. 1.05V Transient DCM TO CCM
Test condition: 12Vin, 1.05V/10A no airflow

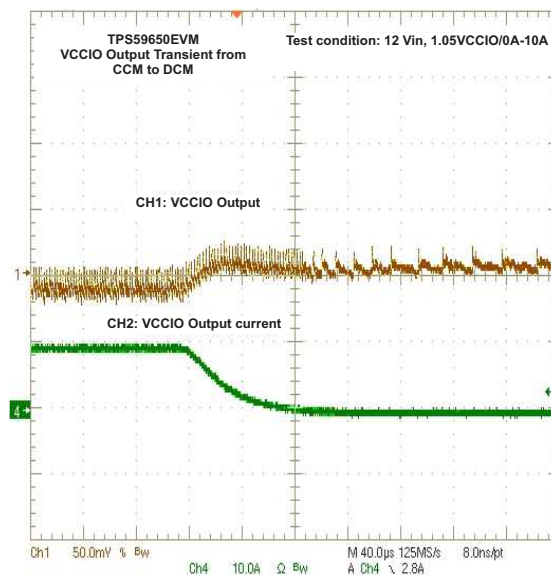


Figure 81. 1.05V Transient CCM to DCM

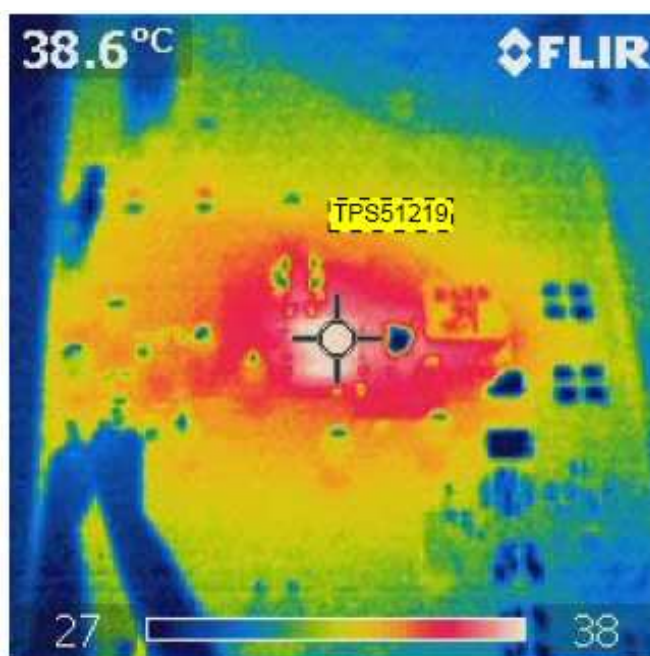


Figure 82. TPS51219 Thermal

7.7 1.2V VDDQ

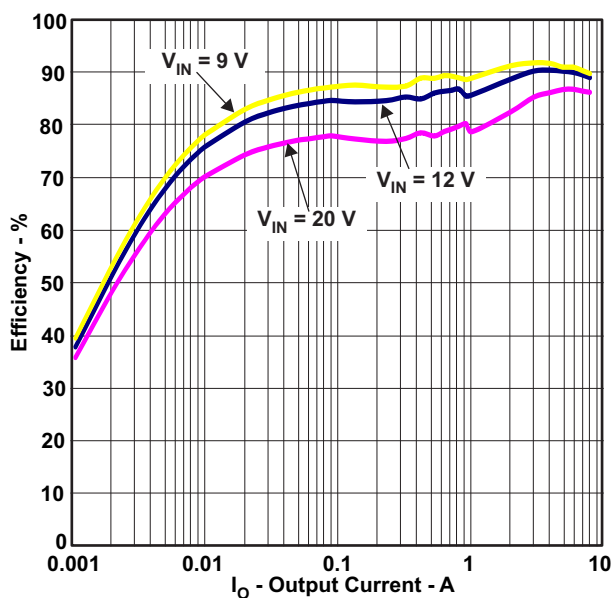


Figure 83. 1.2V Efficiency

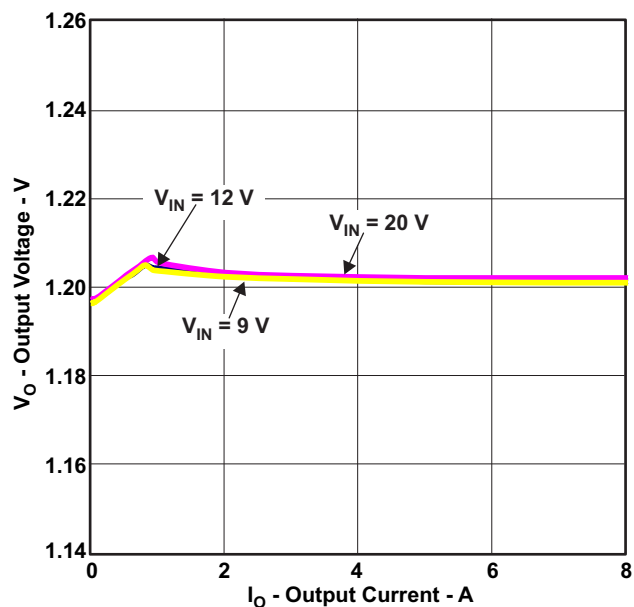


Figure 84. 1.2V Load regulation

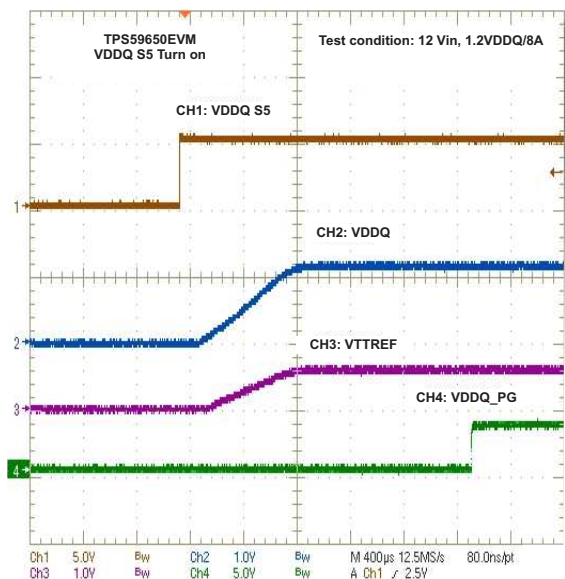


Figure 85. 1.2V Enable Turn on

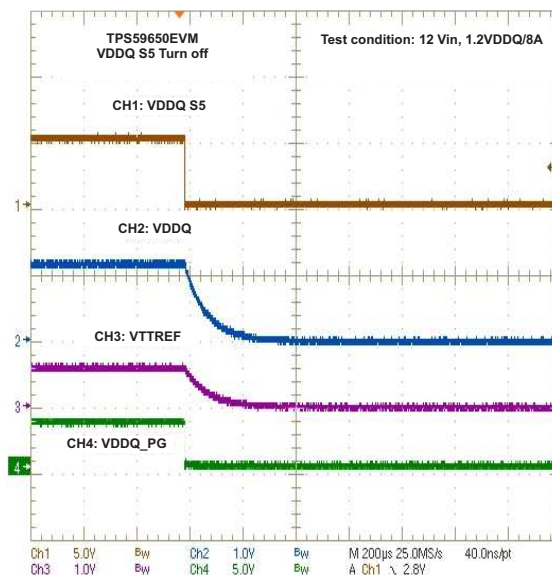


Figure 86. 1.2V Enable Turn off

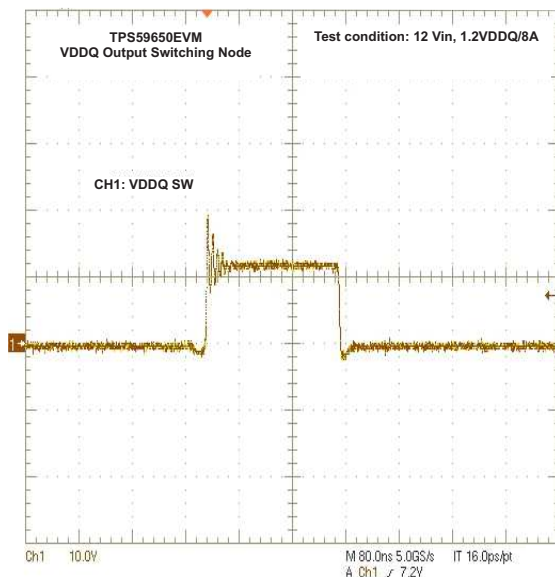


Figure 87. 1.2V Switching Node

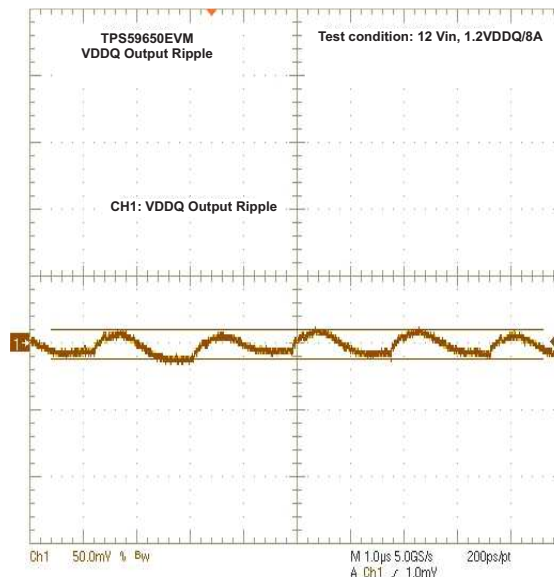


Figure 88. 1.2V Ripple

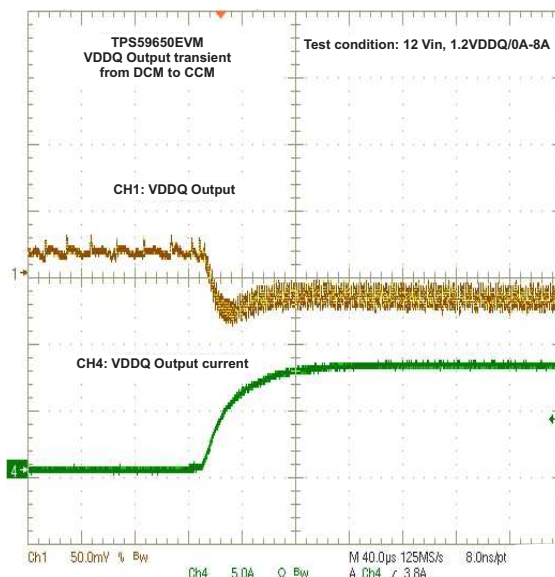


Figure 89. 1.2V Transient DCM TO CCM

Test condition: 12Vin, 1.2V/7.5A no airflow

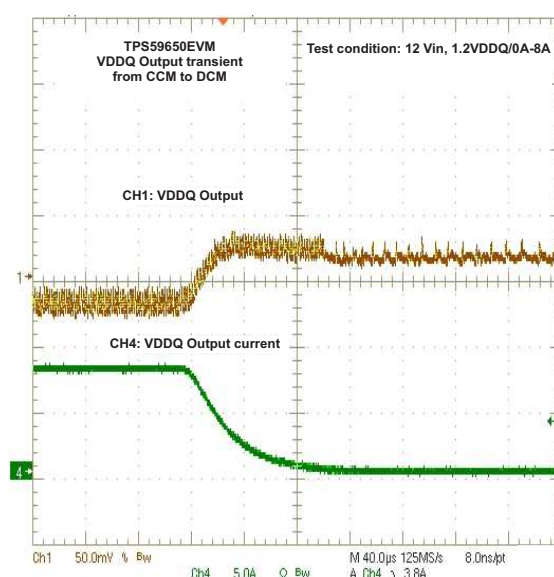


Figure 90. 1.2V Transient CCM to DCM

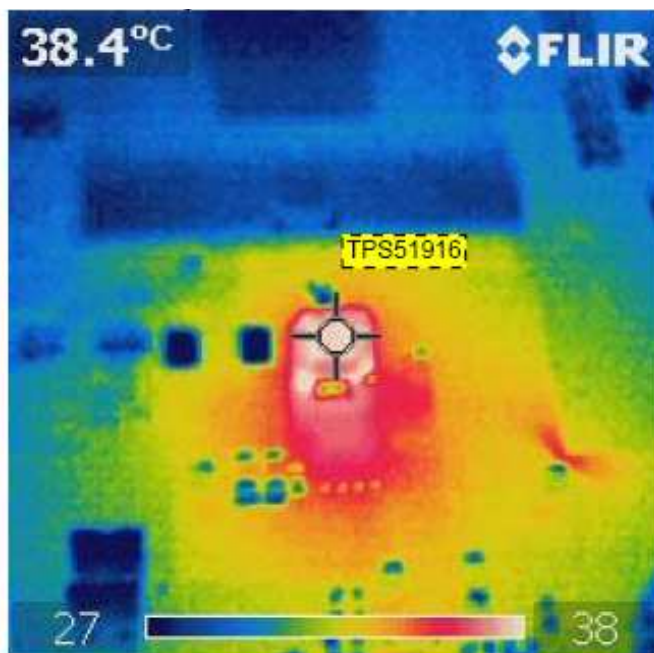


Figure 91. TPS51916 Thermal

The following figures ([Figure 92](#) through [Figure 101](#)) show the design of the TPS59650EVM-753 printed circuit board. The EVM has been designed using 8 Layers circuit board with 1oz copper on outside layers.



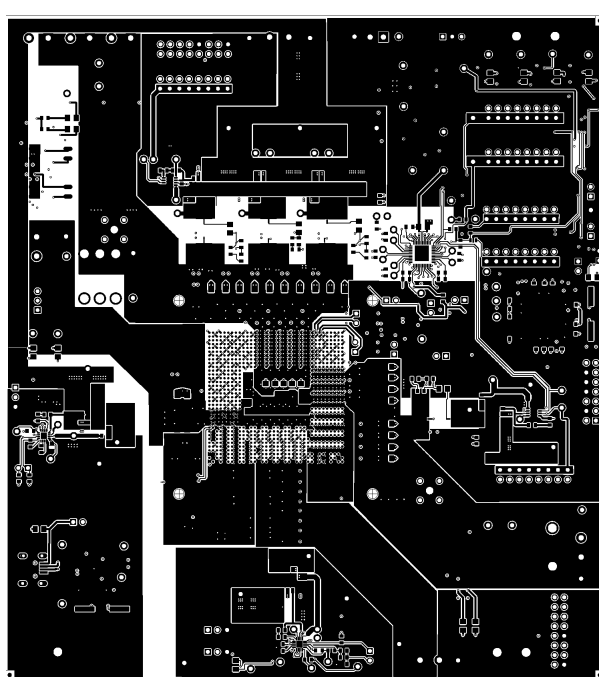


Figure 94. TPS59650EVM-753 Top Copper

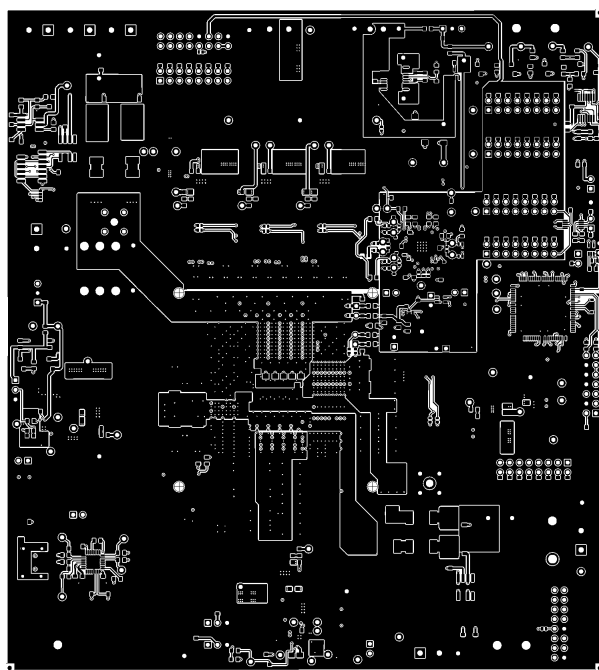


Figure 95. TPS59650EVM-753 Bottom Copper

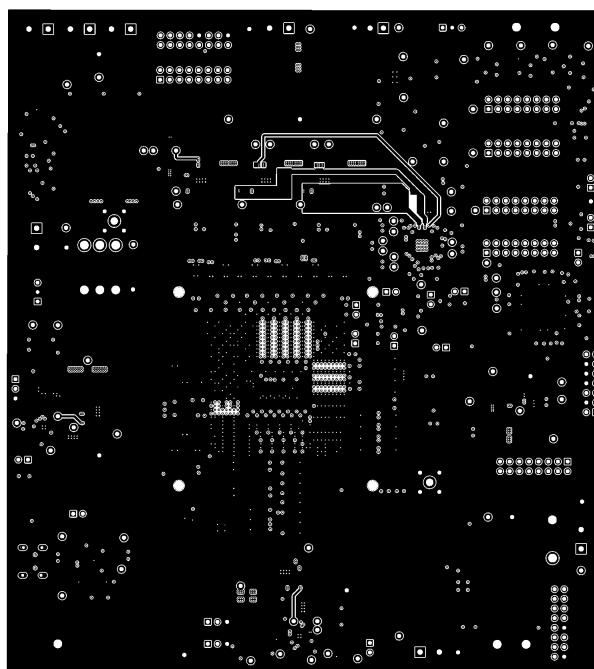


Figure 96. TPS59650EVM-753 Internal Layer 2

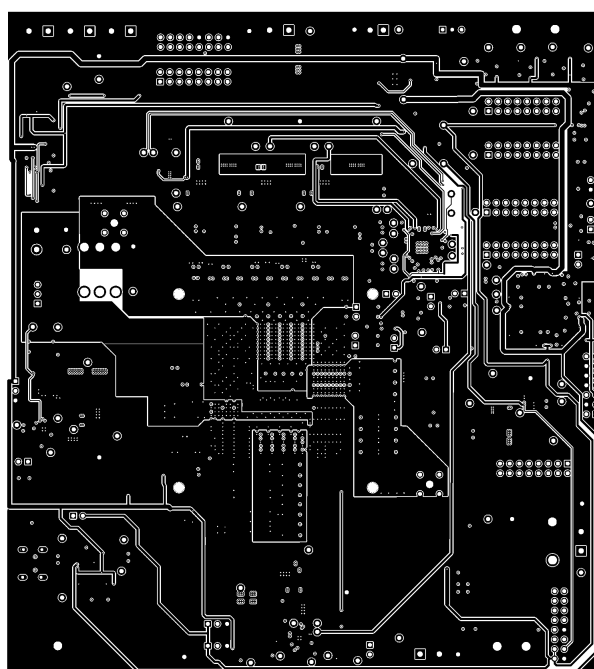


Figure 97. TPS59650EVM-753 Internal Layer 3

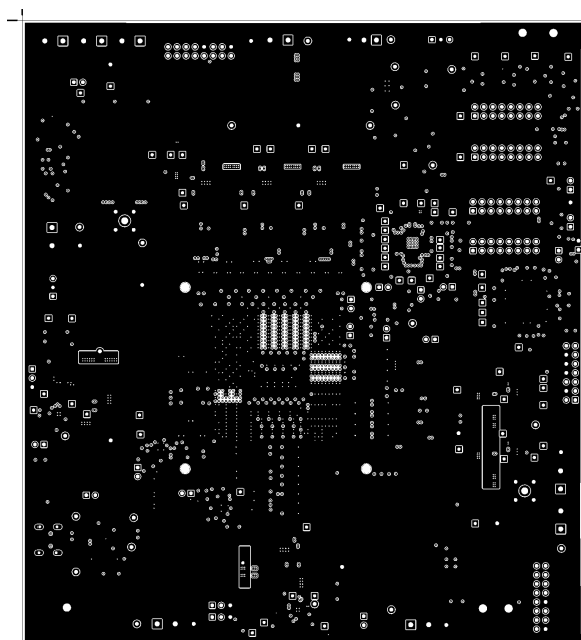


Figure 98. TPS59650EVM-753 Internal Layer 4

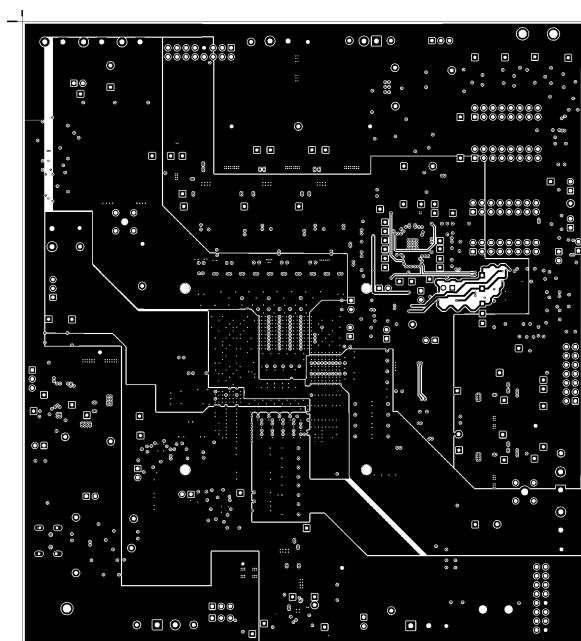


Figure 99. TPS59650EVM-753 Internal Layer 5

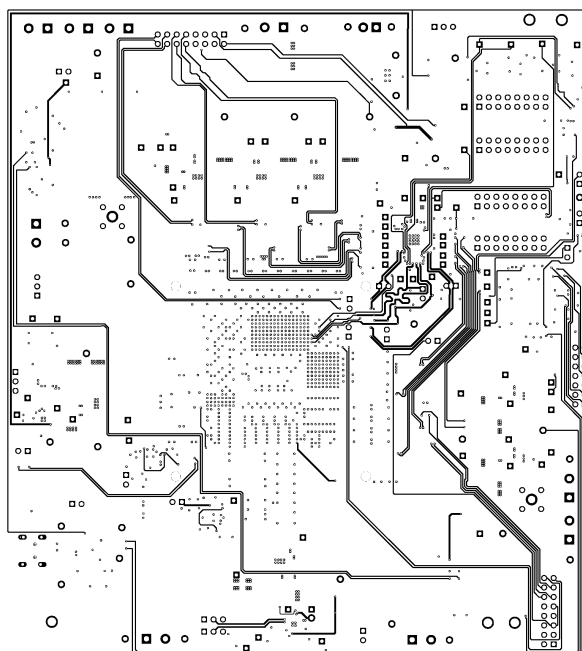


Figure 100. TPS59650EVM-753 Internal Layer 6

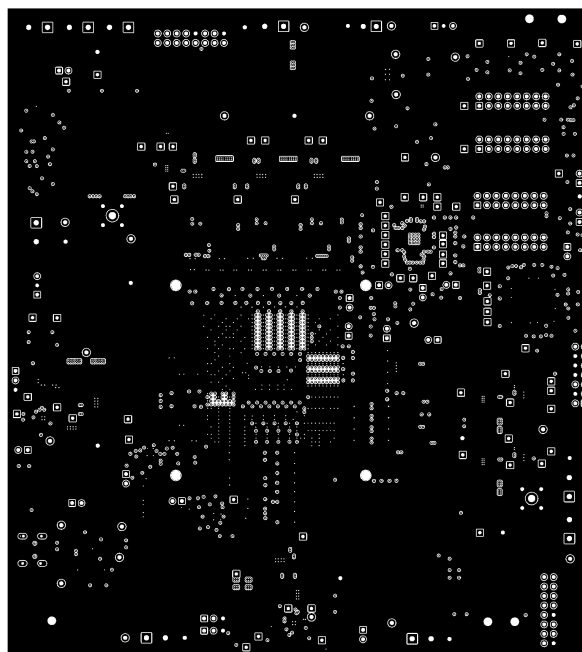


Figure 101. TPS59650EVM-753 Internal Layer 7

9 Bill of Materials

The EVM major components list according to the schematic shown in the following pages.

Table 13. EVM Major Components List

QTY	REF DES	Description	MFR	Part Number
11	C1, C12, C31, C69, C74, C124, C159, C121, C130, C184, C204	Capacitor, Ceramic, 1nF, 50V, X7R, 10%, 0603	STD	STD
5	C104, C108, C112, C115, C118	Capacitor, Ceramic, 33nF, 25V, X7R, 10%, 0603	STD	STD
29	C128, C164, C198, C199, C201, C127, C172, C188, C192, C203, C207, C190, C209, C210, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230	Capacitor, Ceramic, 0.1uF, 25V, X7R, 10%, 0603	STD	STD
3	C129, C133, C168	Capacitor, Polymer, 330uF, 2V, 6mohm, 20%, 7343	Sanyo	2TPF330M6
2	C13, C26	Capacitor, Ceramic, 100pF, 50V, C0G, 10%, 0603	STD	STD
3	C131, C239, C246	Capacitor, Ceramic, 10nF, 50V, X7R, 10%, 0603	STD	STD
6	C15, C16, C19, C20, C76, C77	Capacitor, Polymer, 470uF, 2V, 4mohm, 20%, D2T	Sanyo	2TPLF470M4E
1	C166	Capacitor, Ceramic, 2.2uF, 6.3V, X5R, 10%, 0805	STD	STD
1	C17	Capacitor, Ceramic, 0.33uF, 6.3V, X7R, 10%, 0603	STD	STD
1	C171	Capacitor, Ceramic, 0.22uF, 50V, X7R, 10%, 0603	STD	STD
15	C18, C23, C33, C75, C80, C196, C202, C208, C195, C200, C242, C250, C22, C233, C234	Capacitor, Ceramic, 1uF, 25V, X7R, 10%, 0603	STD	STD
7	C193, C36, C79, C82, C7, C135, C170	Capacitor, Ceramic, 2.2uF, 6.3V, X5R, 10%, 0603	STD	STD
3	C194, C197, C215	Capacitor, Ceramic, 0.01uF, 50V, X7R, 10%, 0603	STD	STD
28	C2, C3, C4, C5, C8, C9, C10, C11, C27, C28, C29, C30, C65, C66, C67, C68, C70, C71, C72, C73, C122, C123, C125, C126, C160, C161, C162, C163	Capacitor, Ceramic, 10uF, 25V, X7R, 20%, 1206	STD	STD
2	C205, C206	Capacitor, Ceramic, 10pF, 50V, C0G, 10%, 0603	STD	STD
2	C213, C214	Capacitor, Ceramic, 22pF, 50V, C0G, 10%, 0603	STD	STD
2	C240, C248	Capacitor, Ceramic, 0.22uF, 25V, X7R, 10%, 0402	STD	STD
2	C241, C249	Capacitor, Ceramic, 220pF, 25V, X7R, 10%, 0402	STD	STD
2	C243, C251	Capacitor, Ceramic, 680pF, 25V, X7R, 10%, 0402	STD	STD
2	C244, C252	Capacitor, Ceramic, 100pF, 25V, C0G, 10%, 0402	STD	STD
2	C245, C253	Capacitor, Ceramic, 1.8nF, 25V, X7R, 10%, 0402	STD	STD
2	C247, C254	Capacitor, Ceramic, 2200pF, 25V, X7R, 10%, 0402	STD	STD
44	C37, C38, C39, C40, C41, C42, C43, C45, C49, C50, C51, C52, C53, C54, C55, C56, C87, C88, C89, C90, C91, C92, C93, C94, C95, C100, C101, C102, C136, C140, C141, C143, C145, C146, C147, C148, C150, C151, C152, C154, C235, C236, C237, C238	Capacitor, Ceramic, 22uF, 6.3V, X5R, 10%, 0805	STD	STD
20	C44, C46, C57, C58, C59, C60, C61, C62, C63, C64, C173, C174, C175, C176, C180, C182, C165, C185, C189, C191	Capacitor, Ceramic, 10uF, 6.3V, X5R, 10%, 0805	STD	STD
1	C6	Capacitor, Ceramic, 4.7uF, 6.3V, X5R, 10%, 0805	STD	STD
8	D1, D2, D3, D9, D10, D12, D13, D14	Diode, LED, Green Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170GKT

Table 13. EVM Major Components List (continued)

QTY	REF DES	Description	MFR	Part Number
5	D4, D5, D7, D8, D11	Diode, LED, Red Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170CKT
1	D6	Diode, Schottky, 200mA, 30V, SOT-23,	Vishay-Liteon	BAT54-V-GS08
1	FB1	Bead, SMD,Ferrite, 100MHz Max, 200mA, +/-25%, 0603	WE	74279266A
5	L1, L2, L3, L4, L5	Inductor, SMT, 0.36uH, 35A , 0.82mohm, 10x11.5mm	Toko	FCUL1040-H-R36M
1	L6	Inductor, SMT, 0.42uH, 17A , 1.5mohm, 8.7x7.0mm	Panasonic	ETQP4LR42AFM
1	L7	Inductor, SMT, 1.0uH, 8.1A , 6.9mohm, 7.3x6.6mm	Panasonic	ETQP3W1R0WFN
7	Q1, Q2, Q3, Q4, Q5, Q8, Q10	MOSFET, Synchronous Buck NexFET Power Block SON 5X6mm	TI	CSD87350Q5D
4	Q11, Q12, Q13, Q14	MOSFET, Nchan, 25V, 31A, 2.5mohm, QFN5X6mm	TI	CSD16407Q5
1	Q15	MOSFET, Pchan, -60V, -0.33A, 2ohm, SOT23	Infineon	BSS83P
6	Q6, Q7, Q9, Q16, Q17, Q18	MOSFET, Nchan, 100V, 0.17A, 6ohm, SOT23	Fairchild	BSS123
1	R1	Resistor, Chip, 42.2k, 1/10W, 1%, 0603	STD	STD
4	R101, R102, R118, R119	Resistor, Chip, 56.2k, 1/10W, 1%, 0603	STD	STD
1	R104	Resistor, Chip, 2.43k, 1/10W, 1%, 0603	STD	STD
7	R106, R107, R122, R123, R141, R165, R166	Resistor, Chip, 30.1k, 1/10W, 1%, 0603	STD	STD
4	R108, R109, R124, R125	Resistor, Chip, 24.3k, 1/10W, 1%, 0603	STD	STD
22	R12, R15, R24, R31, R36, R41, R54, R58, R73, R76, R140, R142, R144, R145, R156, R157, R159, R161, R232, R233, R250, R268	Resistor, Chip, 0, 1/10W, 1%, 0603	STD	STD
7	R130, R131, R147, R215, R216, R217, R222	Resistor, Chip, 180, 1/10W, 1%, 0603	STD	STD
14	R132, R148, R149, R150, R158, R183, R185, R205, R214, R219, R220, R221, R230, R231	Resistor, Chip, 10.0k, 1/10W, 1%, 0603	STD	STD
5	R133, R134, R151, R213, R218	Resistor, Chip, 1.00k, 1/10W, 1%, 0603	STD	STD
1	R139	Resistor, Chip, 10.5k, 1/10W, 1%, 0603	STD	STD
1	R152	Resistor, Chip, 22.1k, 1/10W, 1%, 0603	STD	STD
6	R16, R110, R111, R126, R127, R160	Resistor, Chip, 20.0k, 1/10W, 1%, 0603	STD	STD
1	R163	Resistor, Chip, 15.0k, 1/10W, 1%, 0603	STD	STD
4	R164, R237, R238, R239	Resistor, Chip, 2.00k, 1/10W, 1%, 0603	STD	STD
1	R167	Resistor, Chip, 51.1k, 1/10W, 1%, 0603	STD	STD
1	R168	Resistor, Chip, 1, 1/10W, 1%, 0603	STD	STD
1	R176	Resistor, Chip Array, 10.0k, 62.5mW, 5%, 1206	Yageo	TC164-JR-0710KL
3	R169, R170, R171	Resistor, Chip, 1, 1/8W, 1%, 0805	STD	STD
3	R172, R173, R178	Resistor, Chip, 0.01, 1W, 1%, 2512	STD	STD
5	R174, R175, R177, R179, R180	Resistor, Chip, 0.05, 1W, 1%, 2512	STD	STD
5	R176, R177, R178, R179, R199	Resistor, Chip, 330, 1/10W, 1%, 0603	STD	STD
7	R18, R194, R202, R246, R248, R260, R262	Resistor, Chip, 10.0k, 1/16W, 1%, 0402	STD	STD
2	R181, R189	Resistor, Chip, 0.005, 1W, 1%, 2512	STD	STD
1	R182	Resistor, Chip, 8.06k, 1/10W, 1%, 0603	STD	STD
5	R186, R187, R188, R190, R212	Resistor, Chip, 330, 1/10W, 1%, 0603	STD	STD
1	R192	Resistor, Chip, 100, 1/10W, 1%, 0603	STD	STD
10	R193, R195, R196, R197, R198, R199, R203, R204, R206, R207	Resistor, Chip, 1M, 1/16W, 1%, 0402	STD	STD
1	R2	Resistor, Chip, 130, 1/16W, 1%, 0402	STD	STD

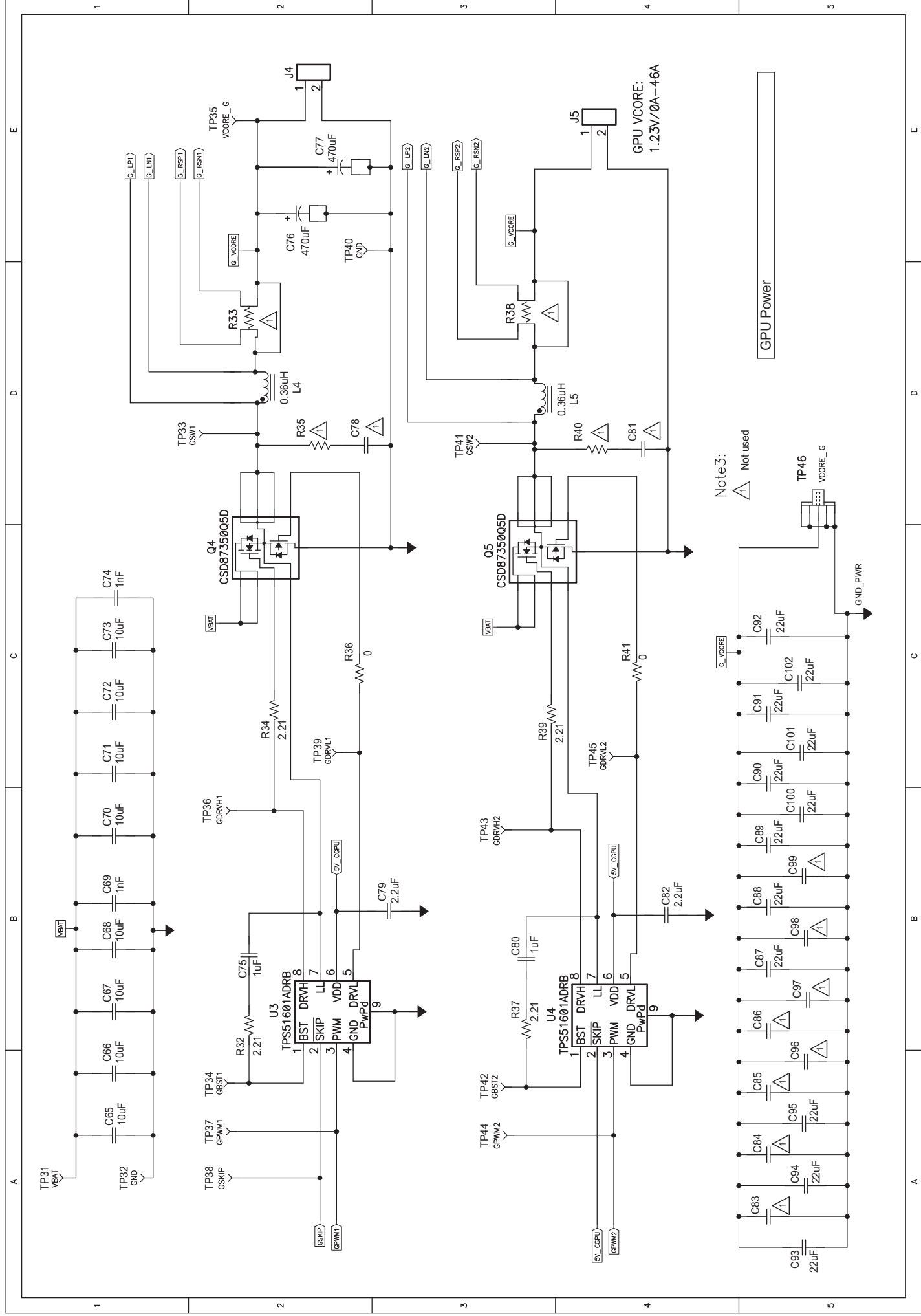
Table 13. EVM Major Components List (continued)

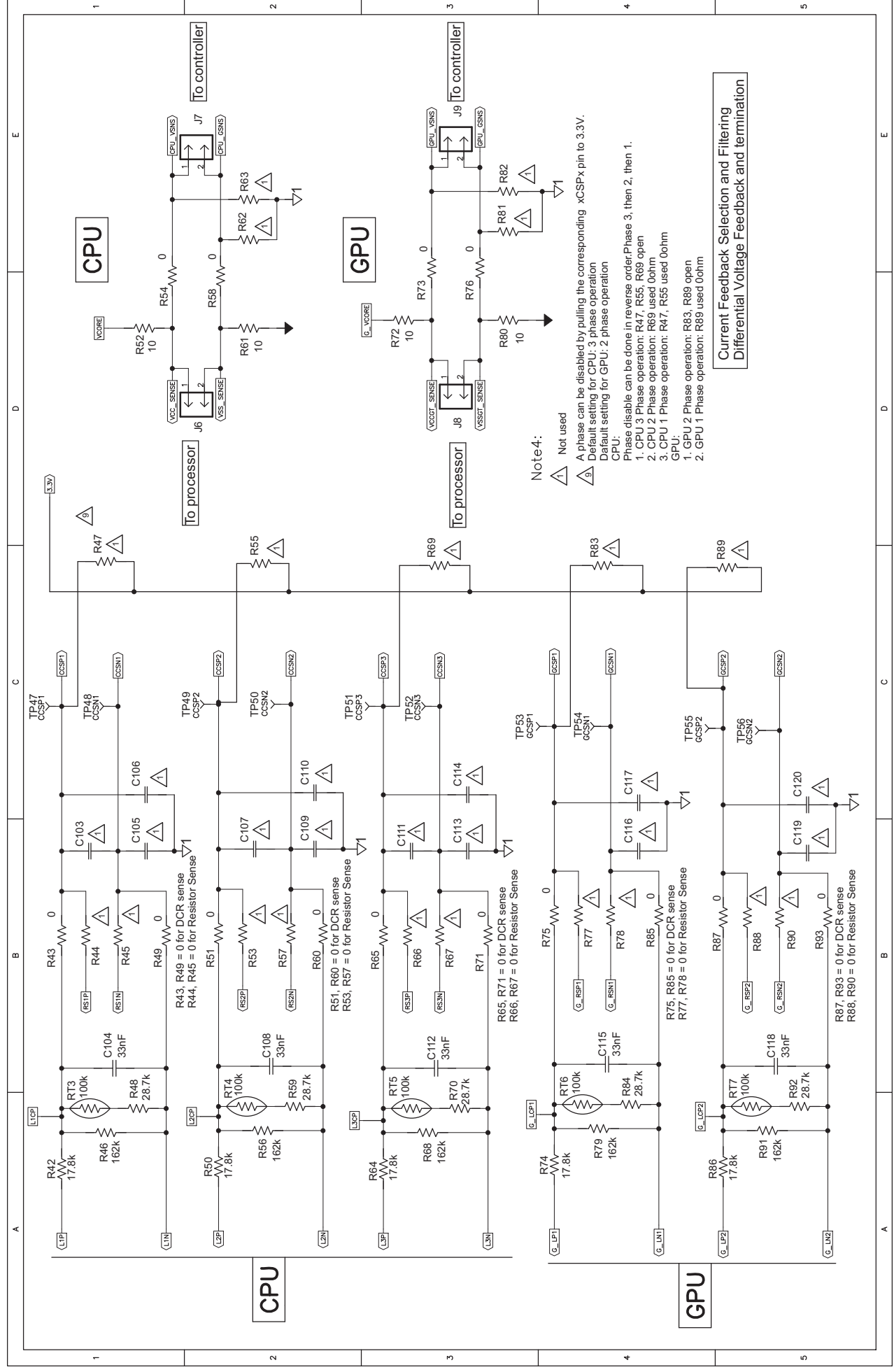
QTY	REF DES	Description	MFR	Part Number
20	R43, R49, R51, R60, R65, R71, R75, R85, R87, R93, R200, R201, R208, R209, R243, R249, R253, R254, R263, R265	Resistor, Chip, 0, 1/16W, 1%, 0402	STD	STD
1	R21	Resistor, Chip, 200k, 1/10W, 1%, 0603	STD	STD
2	R210, R211	Resistor, Chip, 3.01k, 1/10W, 1%, 0603	STD	STD
1	R224	Resistor, Chip, 75, 1/10W, 1%, 0603	STD	STD
1	R225	Resistor, Chip, 130, 1/10W, 1%, 0603	STD	STD
1	R226	Resistor, Chip, 43.2, 1/10W, 1%, 0603	STD	STD
1	R227	Resistor, Chip, 1.50k, 1/10W, 1%, 0603	STD	STD
2	R228, R229	Resistor, Chip, 33.2, 1/10W, 1%, 0603	STD	STD
1	R23	Resistor, Chip, 4.02k, 1/10W, 1%, 0603	STD	STD
2	R234, R236	Resistor, Chip, 470, 1/10W, 1%, 0603	STD	STD
1	R235	Resistor, Chip, 2.21k, 1/10W, 1%, 0603	STD	STD
2	R240, R241	Resistor, Chip, 2.74k, 1/10W, 1%, 0603	STD	STD
2	R242, R251	Resistor, Chip, 2.21, 1/16W, 1%, 0402	STD	STD
2	R244, R255	Resistor, Chip, 475k, 1/16W, 1%, 0402	STD	STD
2	R245, R257	Resistor, Chip, 5.62k, 1/16W, 1%, 0402	STD	STD
2	R252, R264	Resistor, Chip, 2.00k, 1/16W, 1%, 0402	STD	STD
1	R258	Resistor, Chip, 3.09k, 1/16W, 1%, 0402	STD	STD
1	R259	Resistor, Chip, 20.0k, 1/16W, 1%, 0402	STD	STD
7	R26, R97, R98, R114, R115, R162, R184	Resistor, Chip, 100k, 1/10W, 1%, 0603	STD	STD
1	R267	Resistor, Chip, 1.37k, 1/16W, 1%, 0603	STD	STD
1	R4	Resistor, Chip, 54.9, 1/16W, 1%, 0402	STD	STD
5	R42, R50, R64, R74, R86	Resistor, Chip, 17.8k, 1/8W, 1%, 0805	STD	STD
5	R46, R56, R68, R79, R91	Resistor, Chip, 162k, 1/10W, 1%, 0603	STD	STD
5	R48, R59, R70, R84, R92	Resistor, Chip, 28.7k, 1/10W, 1%, 0603	STD	STD
7	R5, R52, R61, R72, R80, R143, R146	Resistor, Chip, 10, 1/10W, 1%, 0603	STD	STD
1	R6	Resistor, Chip, 8.25k, 1/10W, 1%, 0603	STD	STD
2	R7, R22	Resistor, Chip, 15.4k, 1/10W, 1%, 0603	STD	STD
14	R8, R11, R14, R20, R28, R29, R32, R34, R37, R39, R135, R136, R153, R154	Resistor, Chip, 2.21, 1/10W, 1%, 0603	STD	STD
5	R94, R103, R105, R120, R121	Resistor, Chip, 39.2k, 1/10W, 1%, 0603	STD	STD
4	R95, R96, R112, R113	Resistor, Chip, 150k, 1/10W, 1%, 0603	STD	STD
4	R99, R100, R116, R117	Resistor, Chip, 75.0k, 1/10W, 1%, 0603	STD	STD
7	RT1, RT2, RT3, RT4, RT5, RT6, RT7	NTC Thermistor, 100k, 0603, 5%	Murata	NCP18WF104J03RB
1	U1	IC, 3+2 phase, IMVP-7 VCORE CPU and GPU Controller, QFN-48	TI	TPS59650RSL
1	U12	IC, Timer, Low-Power CMOS, SO-8	TI	TLC555CDR
1	U13	IC, Dual 10 ohm SPDT Analogy Switch, DGS_10P	TI	TS5A23157DGS
1	U14	IC, Nano Power, Open output comparators, PW14	TI	TLV3404IPW
1	U15	IC, USB to series port controller, QFN-32	TI	TUSB3410RHB
1	U16	IC, CMOS programmable controller, QFP-100	TI	TMS320F2808PZS
3	U17, U19, U20	IC, Dual Schmitt-trigger inverter, DCK-6	TI	SN74LVC2G07DCK
1	U18	IC, Dual-bit dual-supply bus transceiver, RSW-10	TI	SN74AVC2T245RSW
3	U2, U3, U4	IC, Dual high voltage, efficient synchronous MOSFET buck driver, QFN-8	TI	TPS51601ADRB
1	U5	IC, High performance, single synchronous step down controller, QFN-16	TI	TPS51219RTE
1	U6	IC, Complete DDR2, DDR3 and DDR3L memory power solution, QFN-20	TI	TPS51916RUK
1	U7	IC, Dual low dropout regulator, 500mA and 250mA outputs, PWP20	TI	TPS70102PWP
1	U8	IC, 150mA, low Iq, wide bandwidth, LDO, SC70	TI	TPS71712DCK

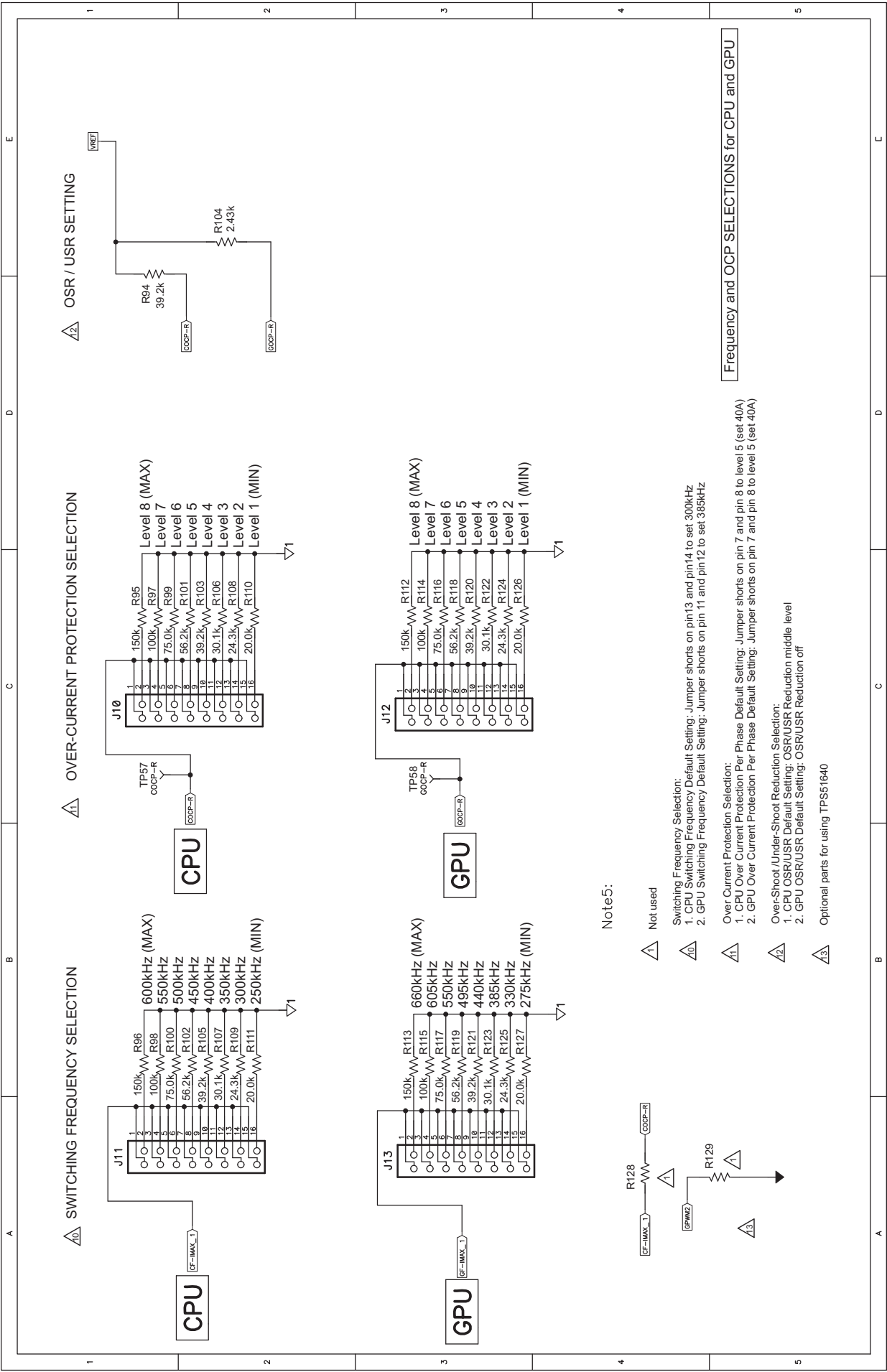
Table 13. EVM Major Components List (continued)

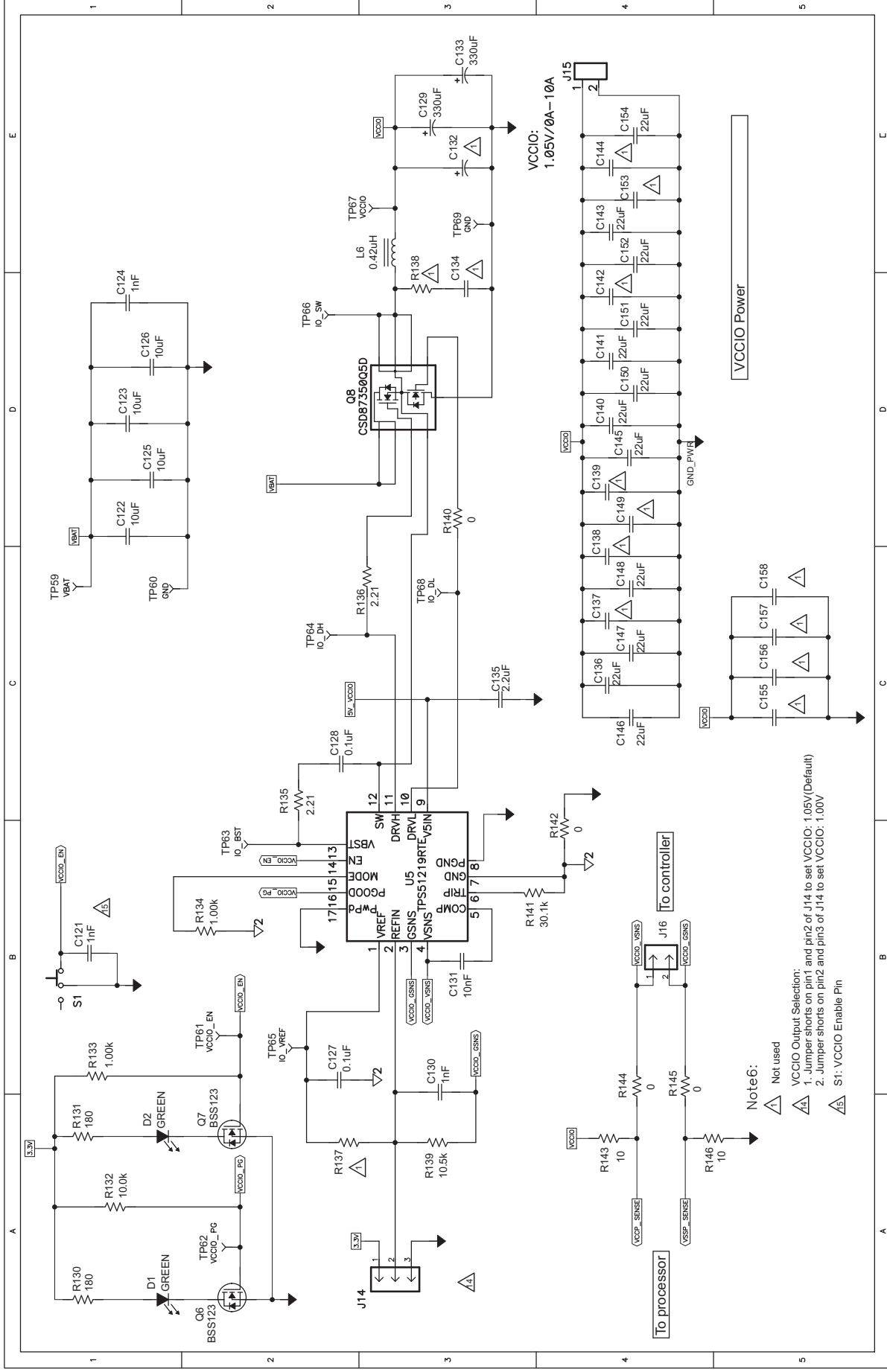
QTY	REF DES	Description	MFR	Part Number
1	U9	IC, Quadruple 2-input positive –AND gates, SO-14	TI	SN74HC08D
2	U10, U11	IC, Dual 4A High speed low side power MOSFET drivers, SO-8	TI	UCC27324D
1	X1	Crystal, controlled oscillators, 0.150"x0.528"	ABRACON	ABLS-20.000MHZ-B2-T
1	Y1	Crystal, controlled oscillators, 0.150"x0.528"	ABRACON	ABLS-12.000MHZ-B2-T
1	XU1	Socket, CPU	Molex	rPGA989

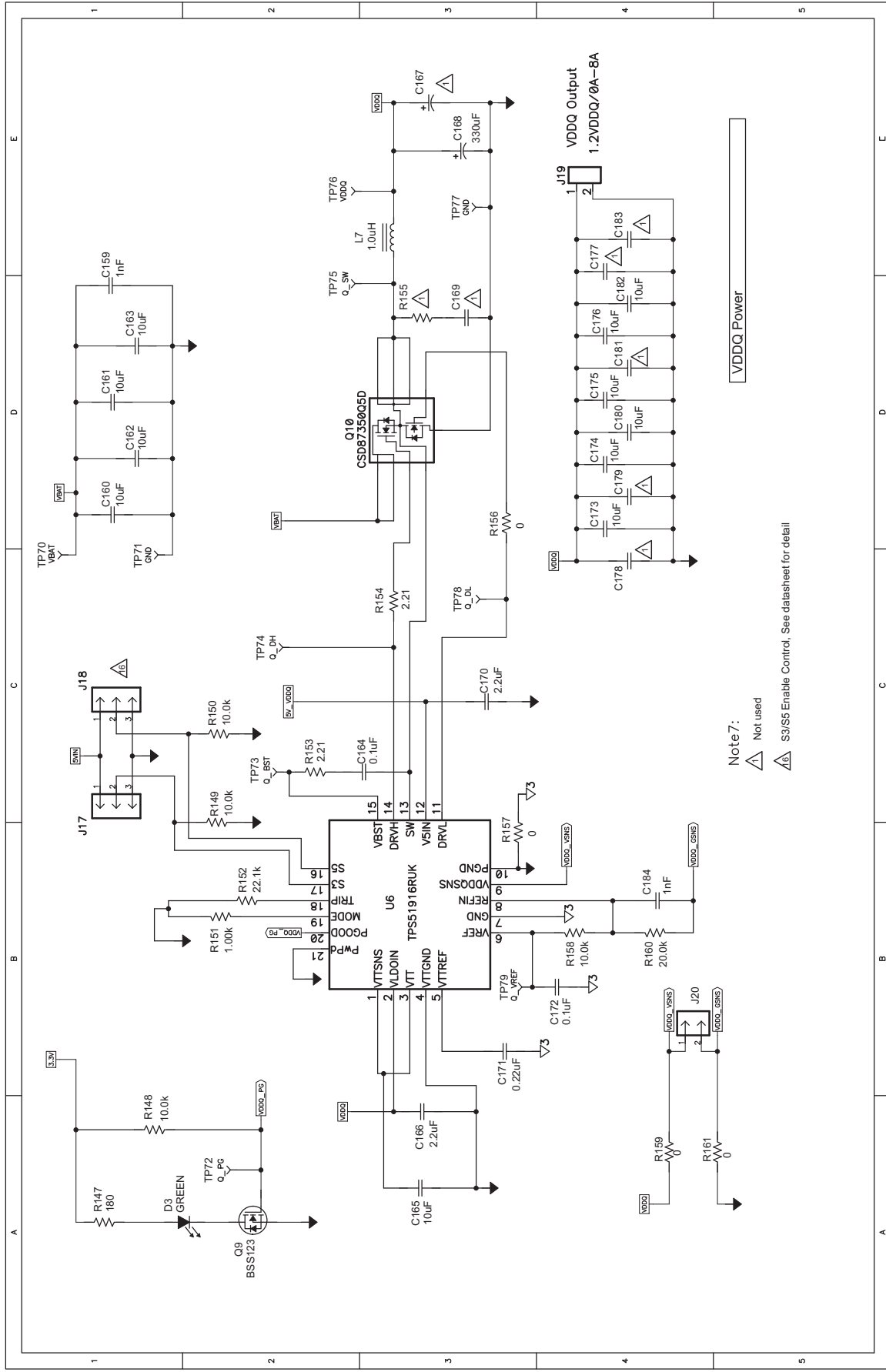
10 Schematics





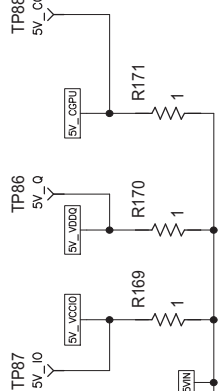
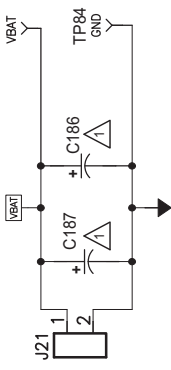






VBAT Conversion Voltage Input:

9V -20V



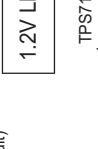
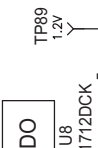
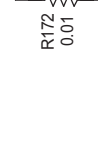
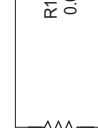
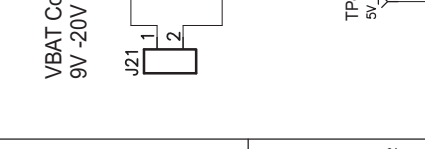
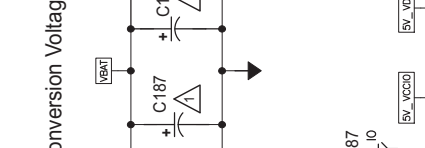
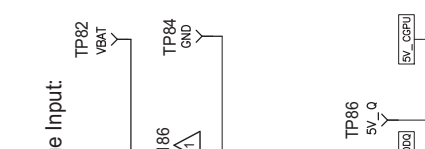
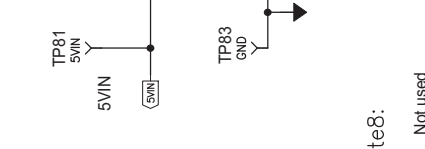
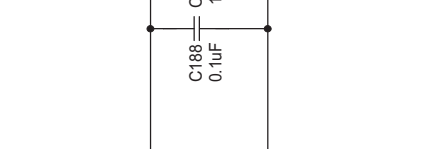
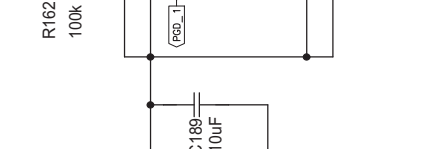
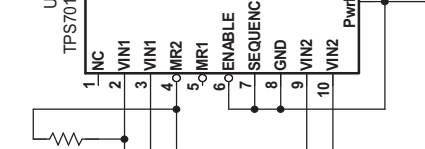
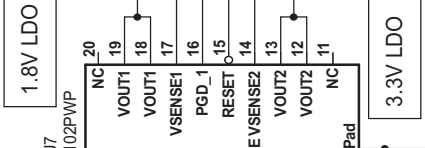
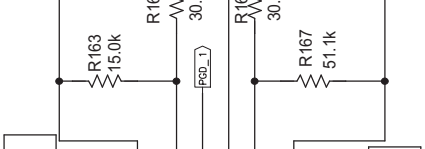
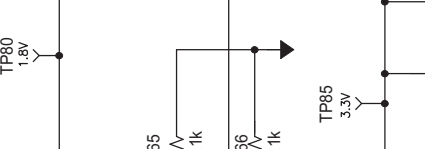
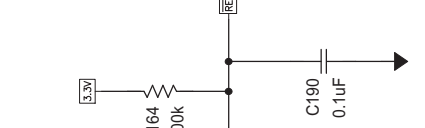
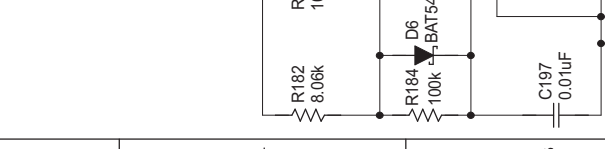
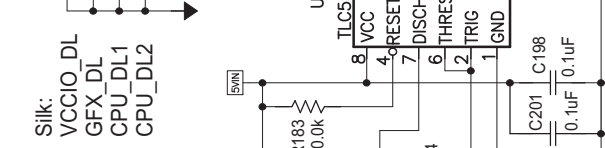
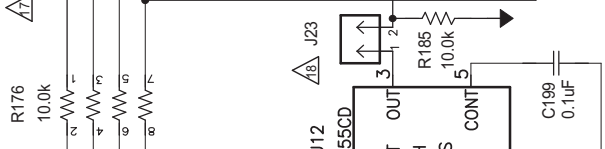
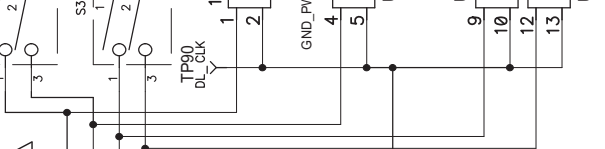
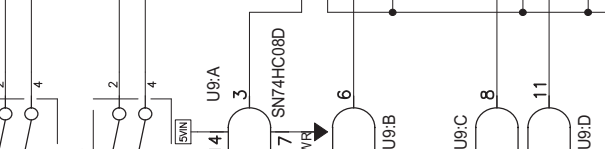
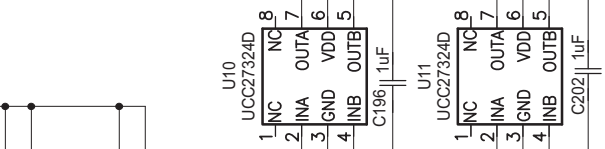
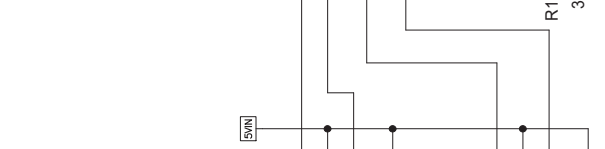
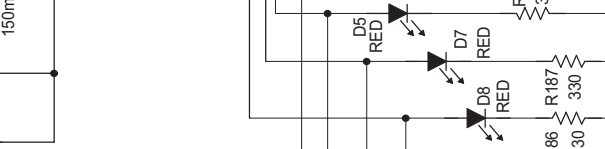
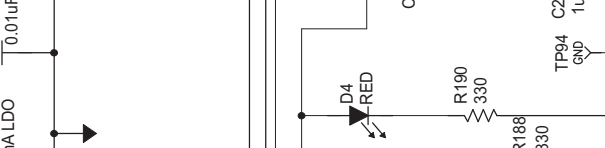
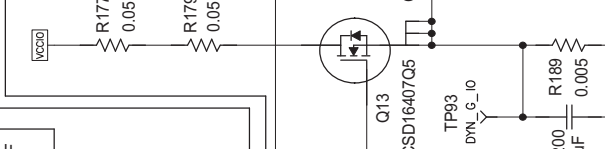
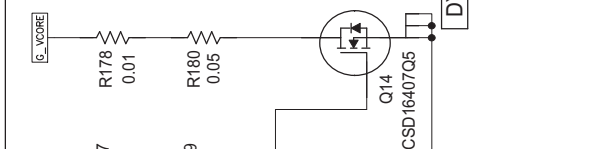
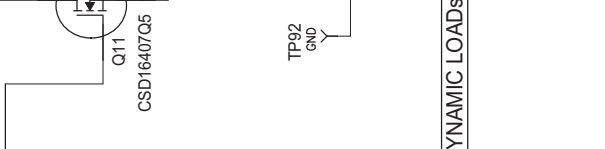
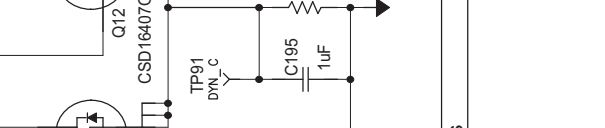
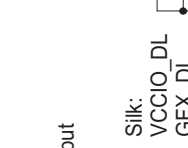
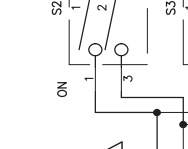
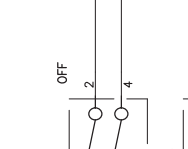
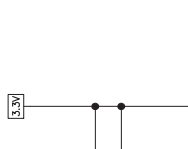
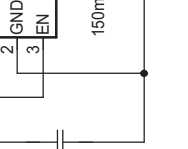
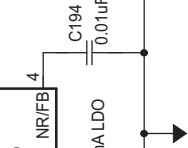
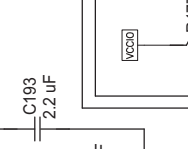
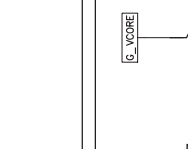
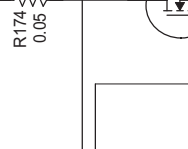
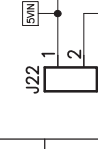
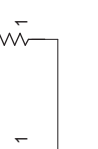
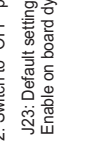
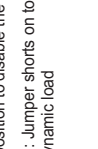
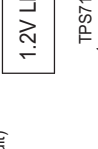
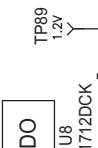
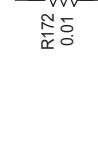
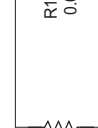
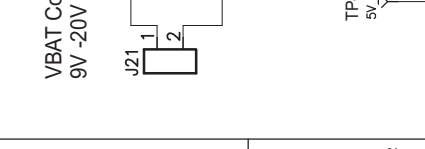
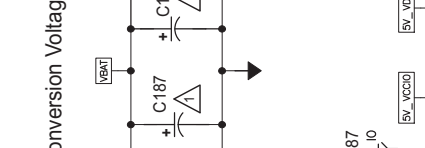
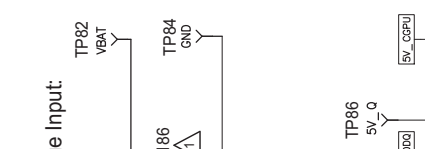
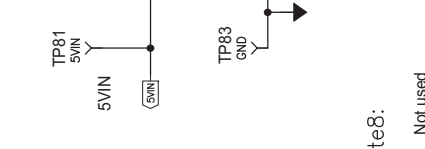
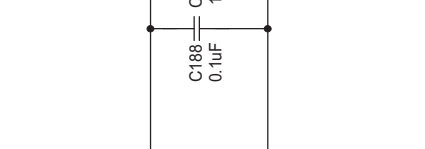
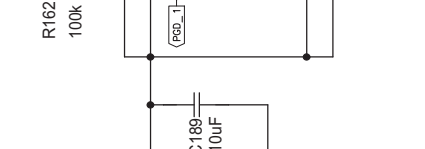
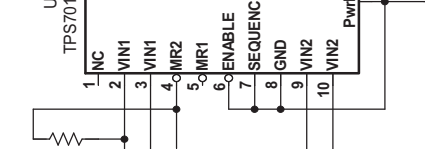
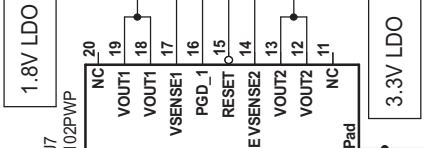
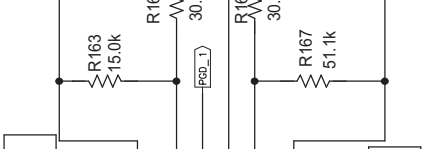
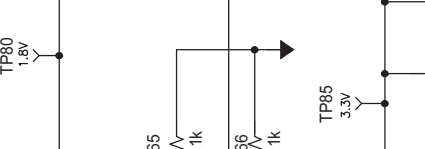
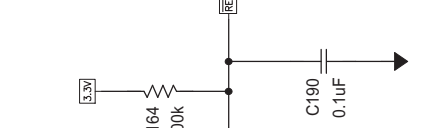
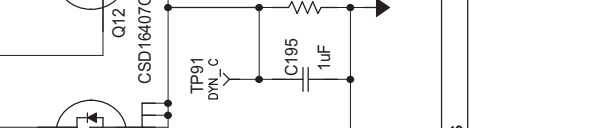
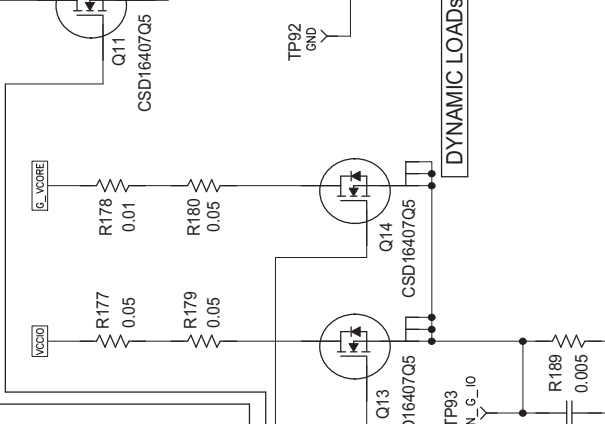
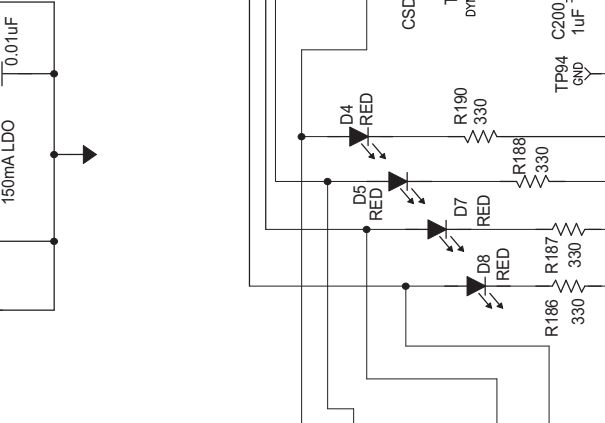
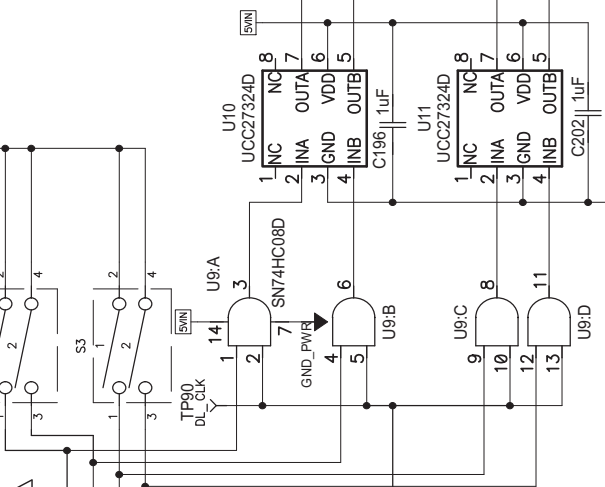
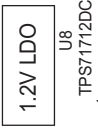
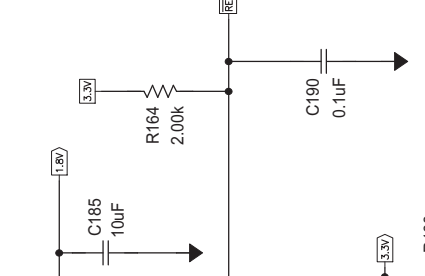
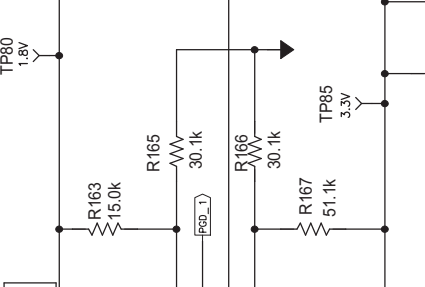
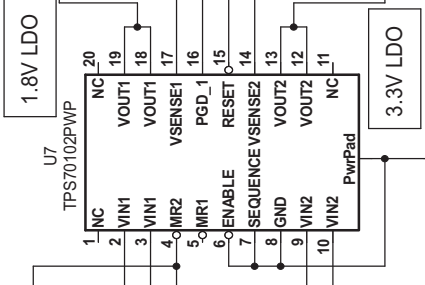
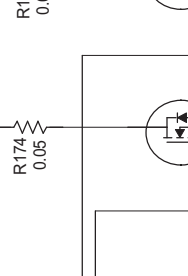
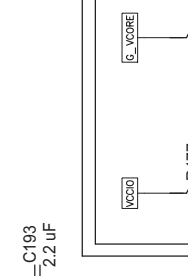
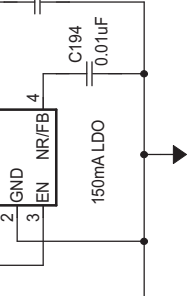
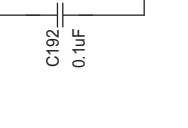
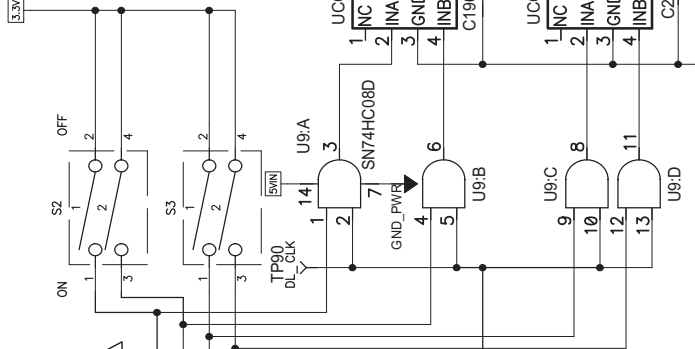
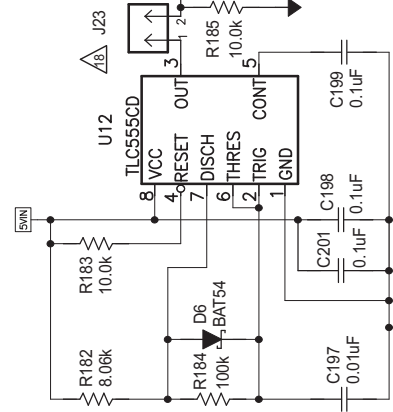
Note8:

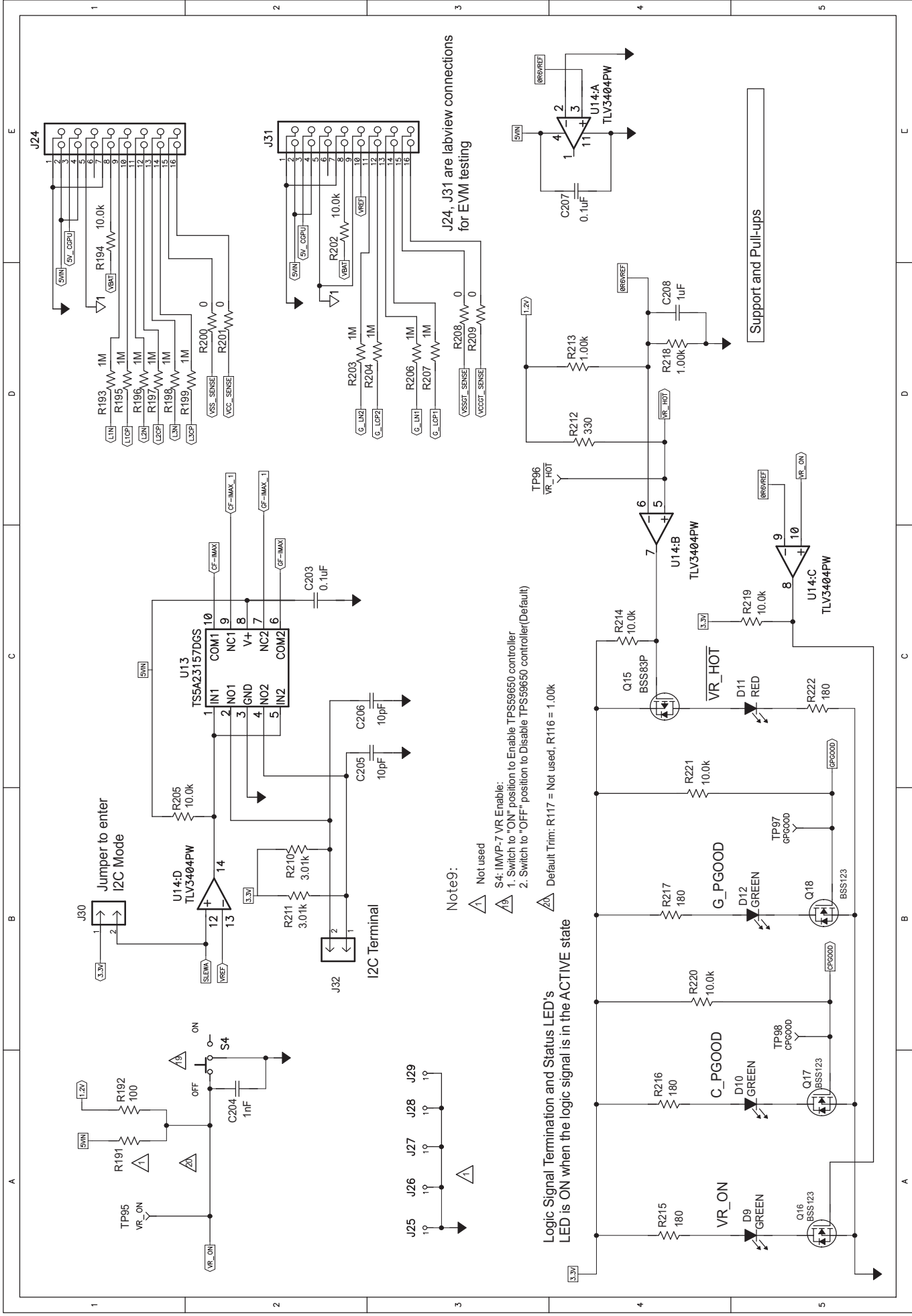
- 1. Not used
- 2. VCCIO, GPU and CPU Dynamic Load:
- 3. Switch to "ON" position to enable the Dynamic Load
- 4. Switch to "OFF" position to disable the Dynamic Load (Default)
- 5. J23: Default setting: Jumper shorts on to Enable on board dynamic load

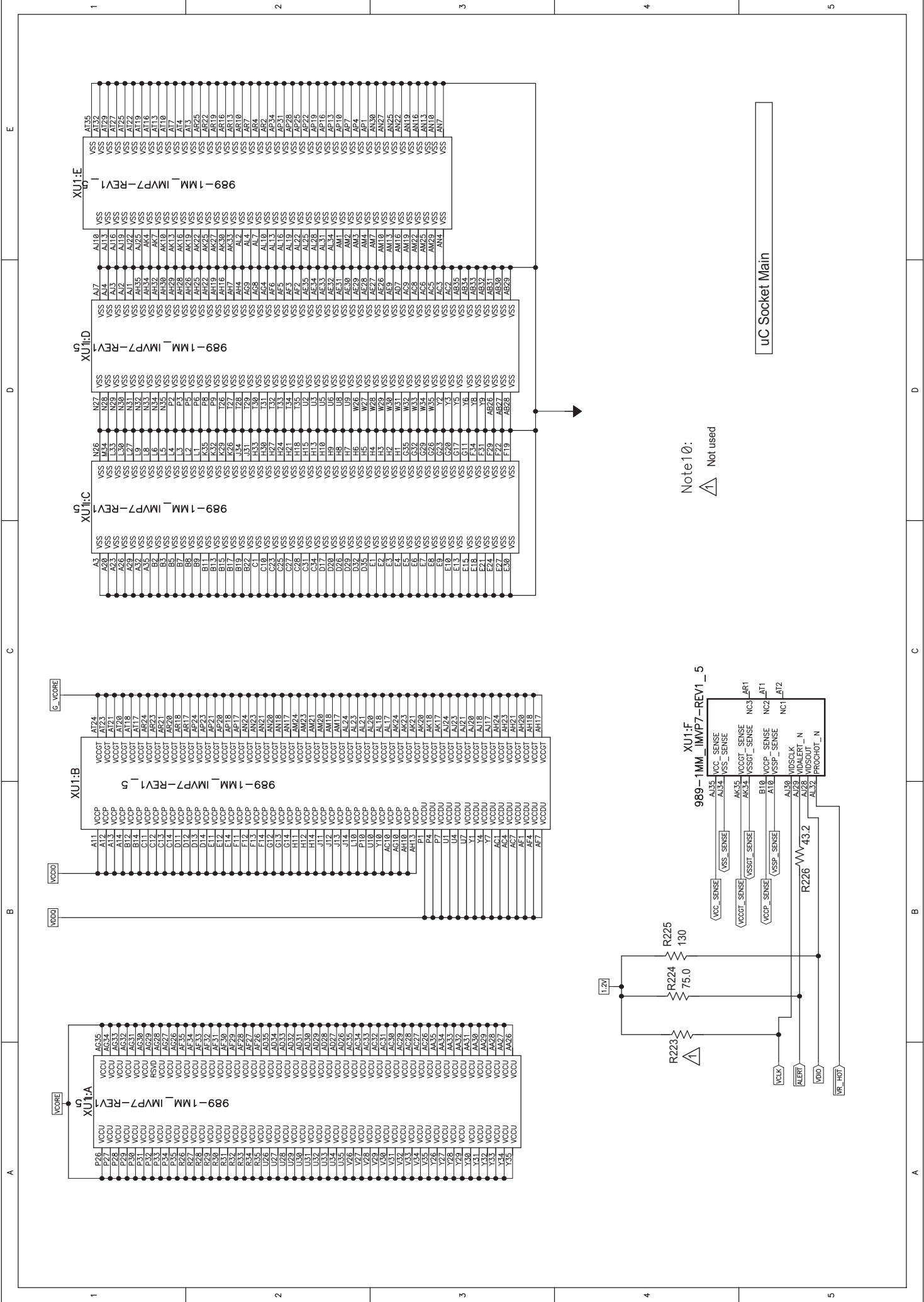
5V Bias Voltage Input

Silk:

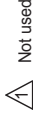
- VCCIO_DL
- GFX_DL
- CPU_DL1
- CPU_DL2





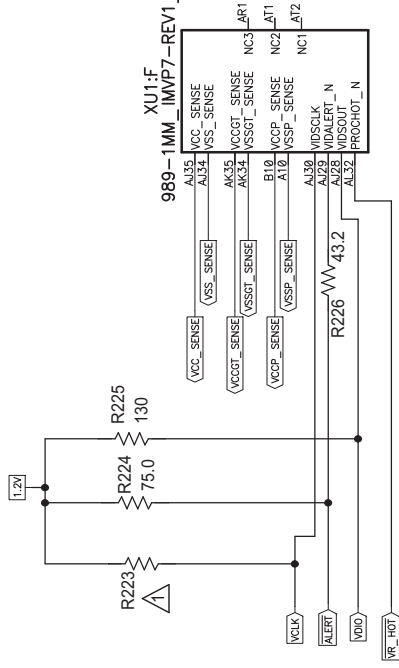


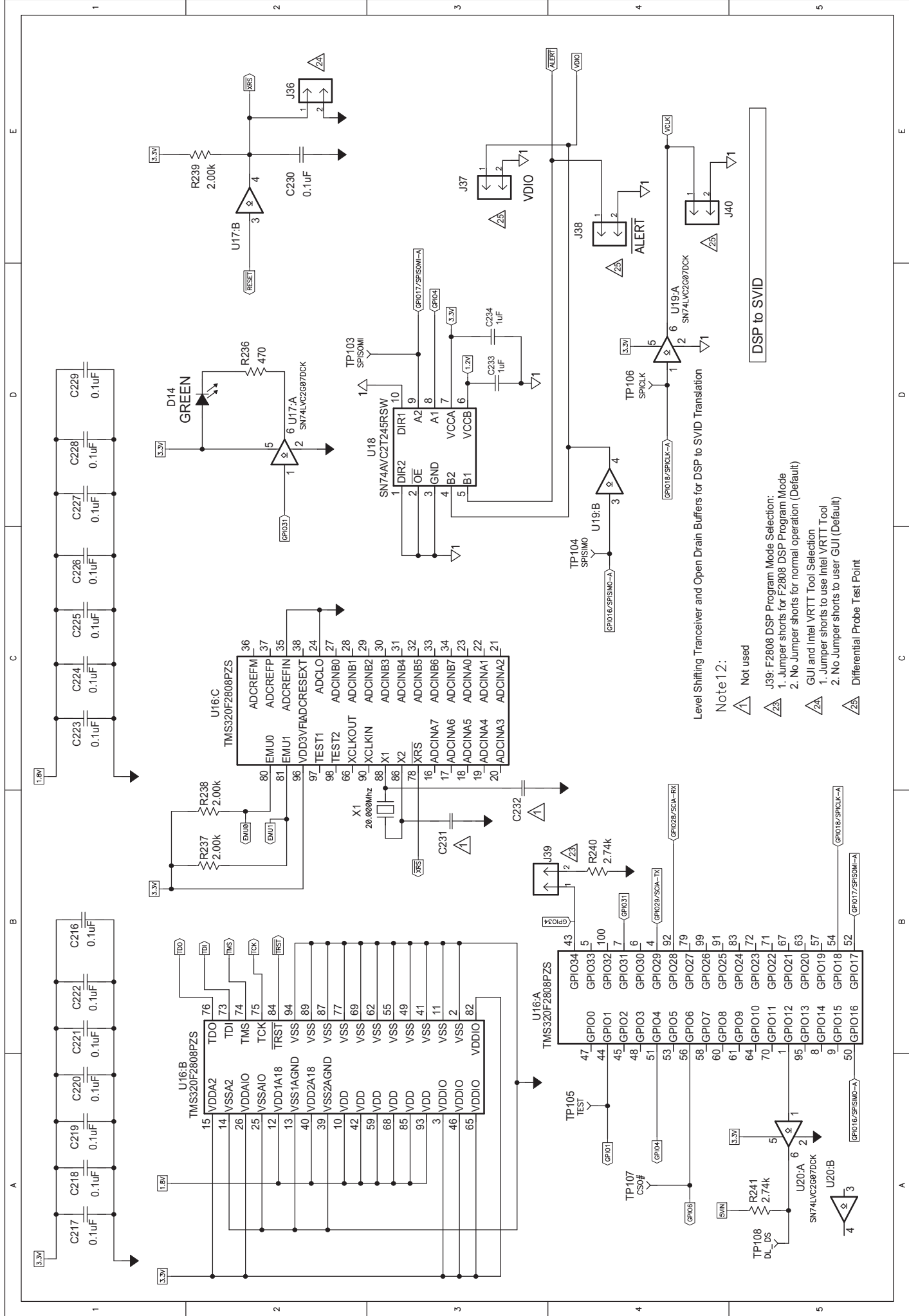
Note 10:

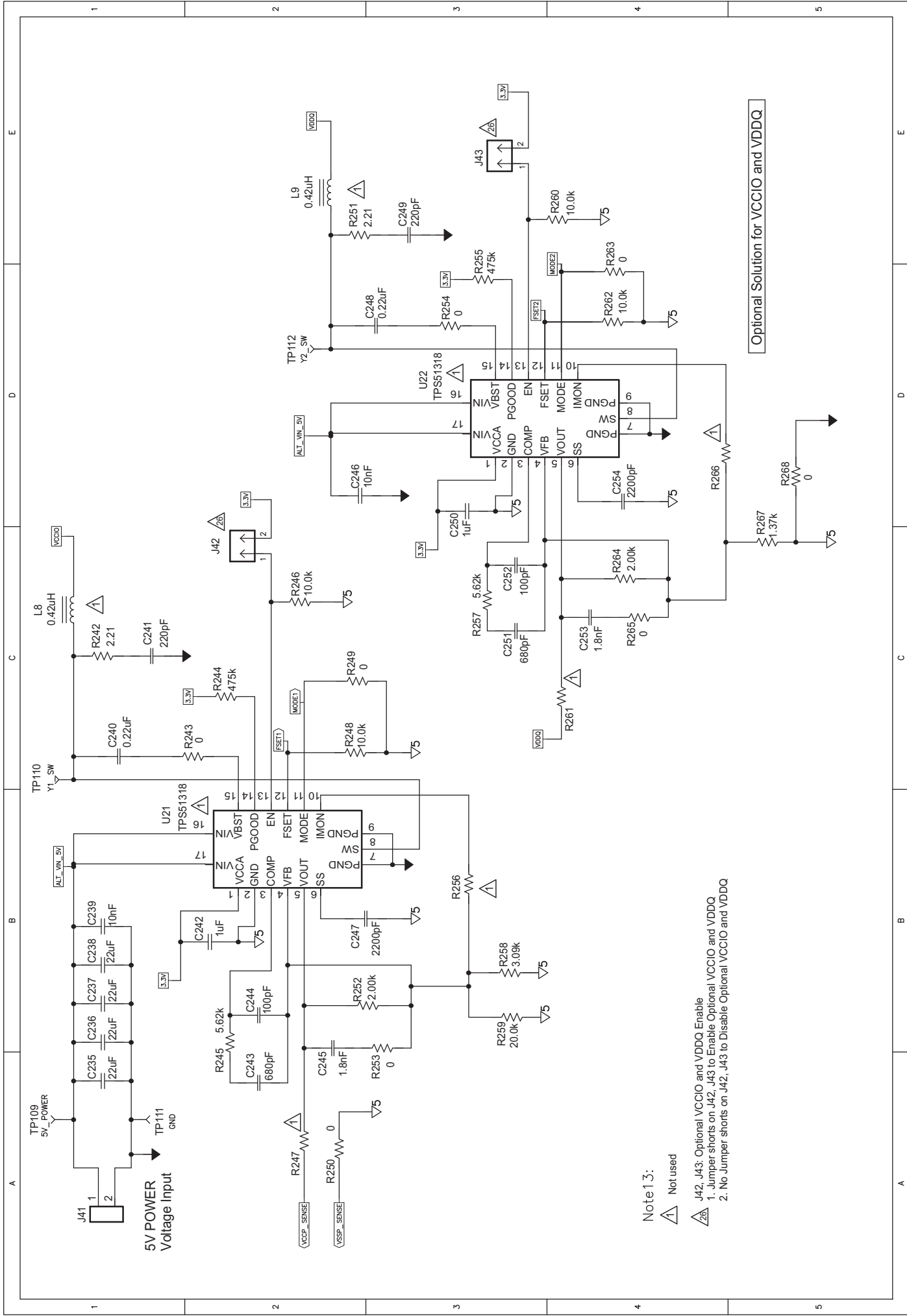


Not used

XU1:F 989-1MM_IMVP7-REV1_5







Note 13:

1. Not used

J42, J43: Optional VCCIO and VDDQ Enable

1. Jumper shorts on J42, J43 to Enable Optional VCCIO and VDDQ
2. No Jumper shorts on J42, J43 to Disable Optional VCCIO and VDDQ

Optional Solution for VCCIO and VDDQ

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

<http://www.tij.co.jp>

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4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

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