AN 18.8

Migrating from the LAN9115 to the LAN9220

1 Objective

The purpose of this application note is to assist SMSC customers with existing LAN9115 designs when upgrading to the new LAN9220 devices. Migrating from the LAN9115 to the LAN9220 will require PCB modifications to support the new LAN9220 package type and the HP Auto-MDIX PHY (even if this mode is not used). This application note addresses all the differences between the LAN9115 and the LAN9220 devices, making this transition as easy as possible.

1.1 References

- LAN9220 Datasheet
- LAN9115 Datasheet
- Reference Design for the LAN9220
- Reference Design for the LAN9115
- Application Note 8-13 Suggested Magnetics

1.2 Overview of Changes Required

Table 1.1 summarizes the changes needed to migrate from the LAN9115 to the LAN9220.

Table 1.1 Summary of Changes Required

CHANGE REQUIRED	COMMENTS	REFERENCES
New PCB	Needed to support footprint change, magnetics and passive component changes.	This application note, Datasheets and Reference Designs are available at www.smsc.com.
New magnetics and passive component network on PHY side of magnetics	Needed to support HP Auto-MDIX.	See Application Note 8-13 for a list of recommended magnetics. AN 8-13 is available at www.smsc.com
Bus Timing & Output Buffer De-rated	Needed to support variable IO voltages < 3.0V.	Refer to section Section 2.3.5
Internal PU/PD resistors augmented & stronger external PU/PD resistors	Needed to support variable IO voltages < 3.0V.	Refer to section Section 2.3.5
Firmware upgrade	Needed to take advantage of mixed endian support	This application note and Datasheets are available at www.smsc.com.
Upgrade drivers	Recognize new device ID and utilize new Checksum Offload Engine	Refer to Table 5.1

2 Hardware Changes

2.1 Component Changes

2.1.1 Device Package

The LAN9220 is packaged in a 56-pin QFN with an exposed VSS pad. Therefore, the LAN9220 is not a drop in replacement for the LAN9115 and will require a new PCB. The recommended PCB land pattern can be found in Chapter 8 of the LAN9220 Datasheet. It is recommended to place a 4x4 grid of vias at 60mil spacing in the exposed pad area for connection to the board's ground plane, as shown in Figure 2.1 below. Please consult with your Assembly House for their process capabilities and recommendations.

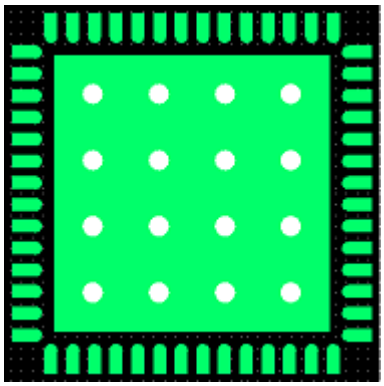

Figure 2.1 PCB Land Pattern

2.1.2 Magnetics

Migrating to the LAN9220 requires different magnetics than those used on the LAN9115. These magnetics have symmetrical channel configurations to allow for the switching of the receive and transmit channels. A list of suggested magnetics for the LAN9220 can be found in Application Note 8-13, entitled "Suggested Magnetics".

2.2 Circuit Changes

2.2.1 Transmit Circuit

The transmit circuit used by the LAN9220, as shown in Figure 2.2 below, is similar to that of the LAN9115.

The similarities between the LAN9220 and the LAN9115 are as follows:

- A 49.9 ohm, 1% resistor from each side of the twisted pair to VDD33A (+3.3V)
- A 10 ohm, 1% resistor from the transmit center tap to VDD33A (+3.3V).

The differences between the LAN9220 and the LAN9115 are as follows:

- The LAN9220 uses magnetics that support HP Auto-MDIX.
- The device-side center tap of the transmit core (TCT) is attached to the device-side center-tap of the receive core (RCT).
- The 49.9 ohm resistors should be placed as close as possible to the LAN9220.

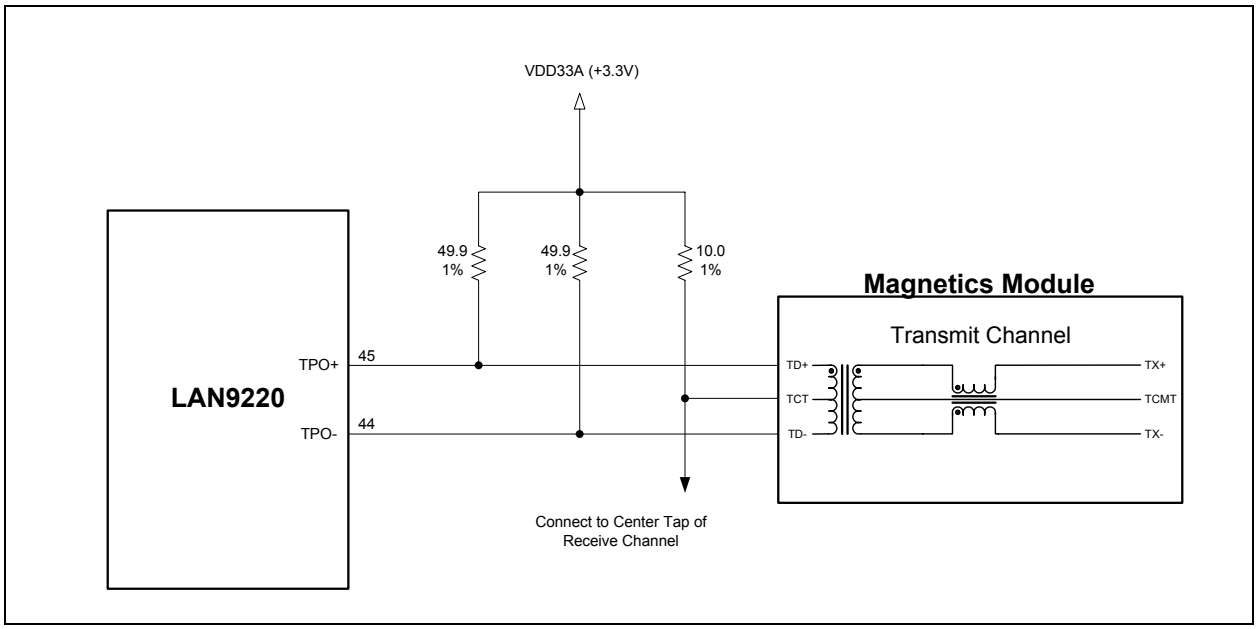

Figure 2.2 LAN9220 Transmit Circuit

2.2.2 Receive Circuit

The receive circuit used by the LAN9220, as shown in Figure 2.3 below, is similar to that of the LAN9115.

The similarities between the LAN9220 and the LAN9115 are as follows:

- Both designs have two 49.9 ohm, 1% resistors between the two signals in the twisted pair.

The differences between the LAN9220 and the LAN9115 are as follows:

- The LAN9220 uses magnetics that support HP Auto-MDIX.
- The LAN9115 had two 6.8nf capacitors, one in series with each side of the twisted pair. These are eliminated (shorted) in the LAN9220.
- In the LAN9115, the mid-point between the two 49.9 ohm resistors is tied to the center tap of the magnetics (RCT) and to a 0.01uF bypass capacitor to ground. In the LAN9220, both resistors are tied to VDD33A (+3.3V), and the 0.01uF bypass capacitor has been eliminated. The center-tap of the receive channel of the magnetics is tied to the transmit center tap (TCT) and to a common 0.022uF bypass capacitor to ground.
- The 49.9 ohm resistors should be placed as close as possible to the LAN9220.

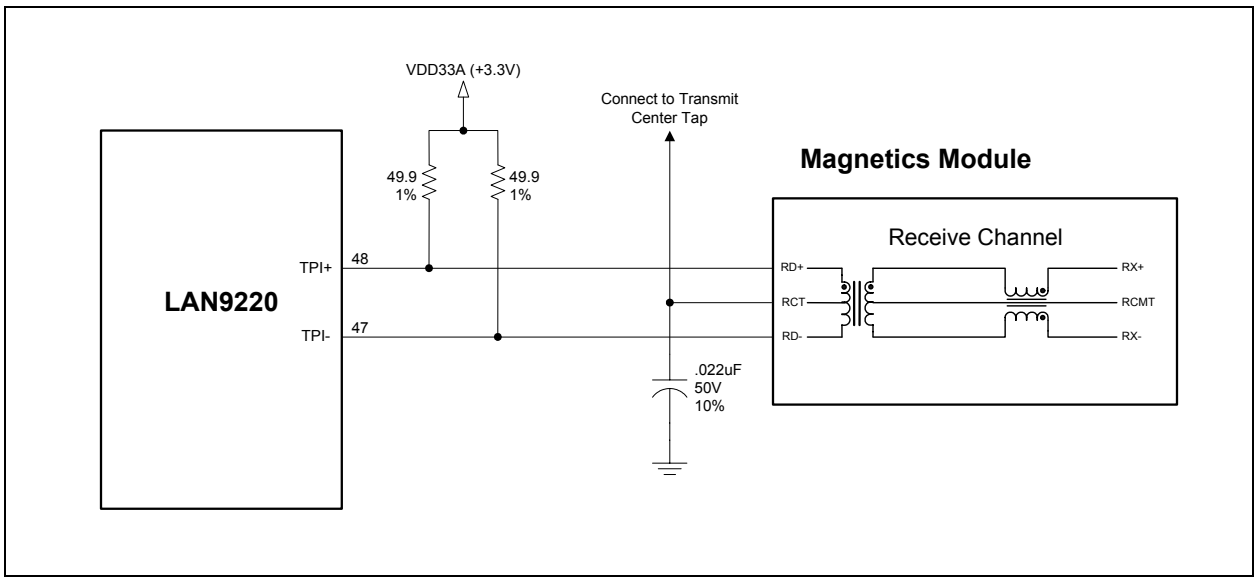

Figure 2.3 LAN9220 Receive Circuit

2.2.3 EMC Considerations

For LAN9220 designs that must operate in an EMI constrained environment, the designer should include four low valued capacitors (less than 15pF) on the TPO+, TPO-, TPI+ & TPI- pins and terminate them to digital ground. These capacitors should be placed as close as possible to the magnetics. These capacitors can then be populated as required for EMI compliance. Additionally, the use of a discrete magnetic and RJ-45 connector is highly recommended, as the integrated magnetics are known to cause EMI compliance issues.

2.3 Pin Changes

2.3.1 Pin Cross-Reference

Table 2.1 below cross-references signal/pin changes between the LAN9115 and the LAN9220.

Table 2.1 Pin Cross-Reference

LAN9115		LAN9220	
SIGNAL	**PIN**	**SIGNAL**	**PIN**
D[15:0]	43-46, 49-53, 56-59, 62-64	D[15:0]	19-23, 25-29, 31-36
A[7:1]	12-18	A[7:1]	6-12
nRD	92	nRD	15
nWR	93	nWR	16
nCS	94	nCS	17
IRQ	72	IRQ	43
Reserved	71, 73, 84, 90, 91		
		TEST	14
		AMDIX_EN	52
SPEED_SEL	74		
FIFO_SEL	76	FIFO_SEL	13
TPO+	79	TPO+	45
TPO-	78	TPO-	44
TPI+	83	TPI+	48
TPI-	82	TPI-	47
EXRES1	87	EXRES1	50
EEDIO	67	EEDIO	38
EECS	68	EECS	39
EECLK	69	EECLK	40
XTAL1	6	XTAL1	55
XTAL2	5	XTAL2	54
nRESET	95	nRESET	42
PME	70	PME	41
GPIO[2:0]	100, 99, 98	GPIO[2:0]/nLED[3:1]	5, 4, 3
RBIAS	10		
ATEST	9		
VREG	2	VDD33REG	1
VDD_IO	20, 28, 35, 42, 48, 55, 61, 97	VDDVARIO	18, 24, 30, 56
GND_IO	19, 27, 34, 41, 47, 54, 60, 96		
VDD_A	81, 85, 89	VDD33A	46, 49, 51

Table 2.1 Pin Cross-Reference (continued)

LAN9115		LAN9220	
SIGNAL	**PIN**	**SIGNAL**	**PIN**
VSS_A	77, 80, 86, 88		
VDD_CORE	3, 65	VDD18CORE	2, 37
GND_CORE	1, 66		
VDD_PLL	7		
VSS_PLL	4		
VDD_REF	8		
VSS_REF	11		
		VDD18A	53
		VSS	Exposed Pad
TX_CLK	40		
TXD[3:0]	36-39		
TX_EN	21		
RX_CLK	26		
RX_ER	25		
COL	33		
RXD[3:0]	24, 23, 22, 75		
CRS	32		
RX_DV	29		
MDIO	30		
MDC	31		

2.3.2 Signal Pins not Available on the LAN9220

The following signal pins are not available on the LAN9220:

- SPEED_SEL
- RBIAS
- ATEST
- TX_CLK, TXD[3:0], TX_EN
- RX_CLK, RX_ER, RXD[3:0], RX_DV
- COL, CRS
- MDIO, MDC

2.3.3 Operating Voltage Requirements

The LAN9220 operating voltage requirements for both VDD33A and VDD33REG have been tightened from +3.3V +/-10% (2.97V - 3.63V) to +3.3 +/-300mV (3.00V - 3.60V).

2.3.4 Power and Ground Pin Changes

The LAN9115 has several different ground pins (GND_IO, VSS_A, GND_CORE, VSS_PLL and VSS_REF). However, the LAN9220 uses a single ground connection (VSS) on the exposed pad. Also, the LAN9220 does not have VDD_PLL, VDD_REF, and VREG power pins.

The LAN9220 has a VDD18A (pin 53) that must be externally connected to VDD18CORE (pins 2, 37) with traces at least 10 mil wide and connected to a 10uF low ESR ceramic capacitor. Each of these 3 pins must be individually decoupled with a 0.01uF capacitor as close as possible to the pin, as shown in Figure 2.4, "Power Connections".

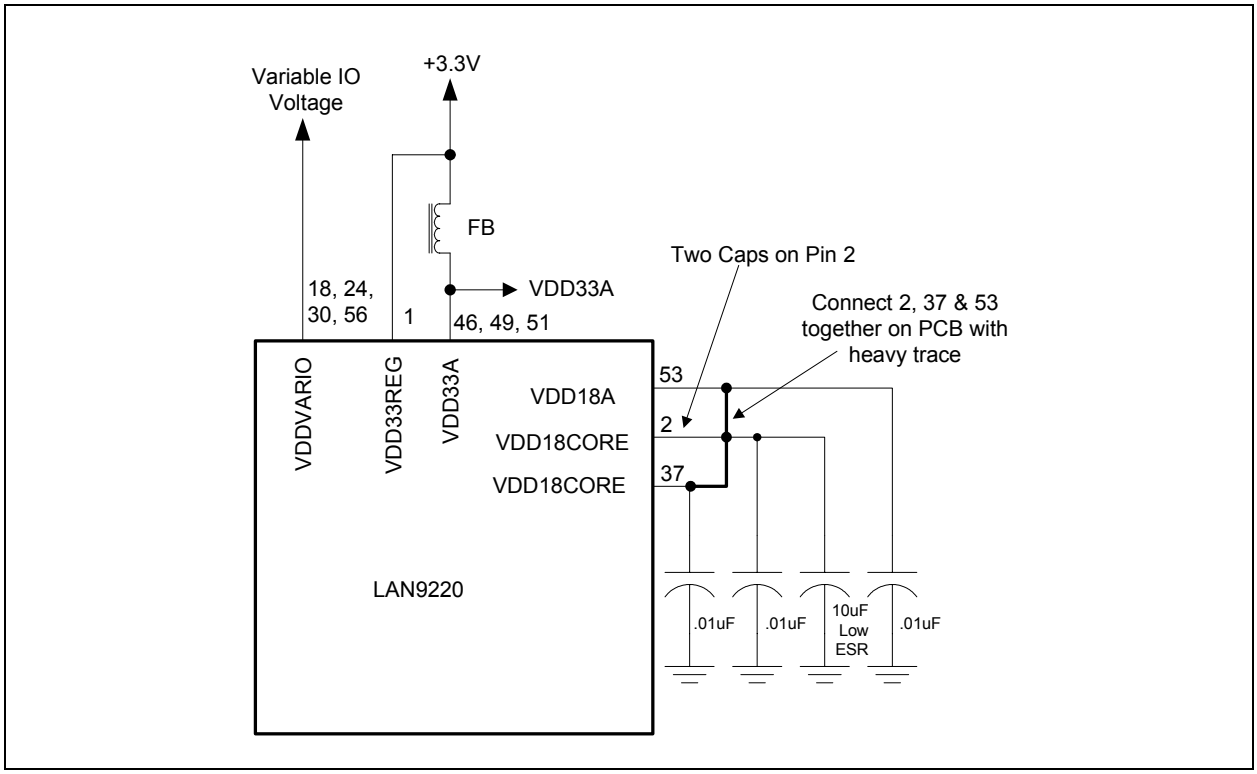

Figure 2.4 Power Connections

2.3.5 Variable I/O Pads

The LAN9220 incorporates variable voltage IO pads that are capable of operation at:

- 1.8V +/-10% (1.62V - 1.98V)
- 2.5V +/-10% (2.25V - 2.75V)
- 3.3V +/- 300mV (3.00V - 3.60V)

The VDDVARIO pins (18, 24, 30 and 56) of the LAN9220 must be supplied with the appropriate IO voltage.

Caution: In the case of a +1.8V I/O application, the VDDVARIO pins cannot be supplied from the VDD18CORE regulator of the LAN9220/LAN9221. The VDDVARIO pins must be supplied from an on-board, external +1.8V regulator.

If you wish to take advantage of the variable IO capablility, there are some changes you should be aware of.

- Bus timing is maintained regardless of VDDVARIO, except that at VDDVARIO = 3.3V or 2.5V, the maximum t_{doff} is 7ns and at VDDVARIO = 1.8V, the maximum t_{doff} is 9ns.

- The specified load capacitance is reduced from 25pF to 10pF at VDDVARIO = 1.8V and 2.5V. For higher capacitance the bus timing must be de-rated.
- Maximum output current is de-rated at reduced VDDVARIO (see Table 2.2).

Table 2.2 IO Buffer Current De-rating

IO BUFFER	3.3V	2.5V	1.8V
VO12	12mA	9mA	4mA
VOD12	12mA	9mA	4mA
VO8	8mA	6mA	3mA
VOD8	8mA	6mA	3mA

- Internal PU/PD resistors must be augmented with external resistors at VDDVARIO < 3.0V, including default selections (see Table 2.3).
- Stronger external PU/PDs are recommended at VDDVARIO < 3.0V, 10K resistors are still acceptable for 3.3V applications (see Table 2.3).

When an EEPROM is used, it must be compatible with the selected VDDVARIO voltage.

Table 2.3 External Pull-Up/Pull-Down Resistor Values

I/O VOLTAGE	PULL-UP/PULL-DOWN RESISTOR VALUE (OHMS)
3.3V +/- 300mV	10K
2.5V +/- 10%	7.5K
1.8V +/- 10%	4.7K

2.3.6 AMDIX_EN (Pin 52)

The LAN9220 includes an HP Auto-MDIX enabled PHY, this pin can be used to enable/disable Auto-MDIX on power-up/reset. This pin has an internal pull-up and must be pulled low to disable Auto-MDIX. To enable Auto-MDIX, this pin should be pulled high or left unconnected. The state of this pin can be read via the HW_CFG register and can also be overridden via Phy register 27, as described in Section 3.3.2, "Special Control/Status Indications (offset: 27)" below.

Note: When operating at reduced VDDVARIO voltage levels (less than 3.0V), this pin must be pulled to a valid level with an external resistor. Refer to Section 2.3.5, "Variable I/O Pads" for more information.

2.3.7 TEST (Pin 14)

Reserved for internal test purposes only.

Note: When operating at a reduced VDDVARIO voltage (less than 3.0V), this pin must be connected to ground or pulled-low with an external resistor. When VDDVARIO = 3.3V, this pin may be left unconnected. Refer to Section 2.3.5, "Variable I/O Pads" for more information.

3 Register Changes

3.1 SCSR Register Changes

3.1.1 ID_REV Register (offset: 50h)

- For the LAN9220 - Bit 31:16 changed to 9220h

3.1.2 HW_CFG Register (offset: 74h)

- Bit 29 becomes FPORTEND, FIFO Port Endian Ordering. This control bit determines the endianess of RX and TX data FIFO host accesses when accessed through the RX/TX Data FIFO ports, including the alias addresses (any access from 00h to 3Ch). When this bit is cleared, data FIFO port accesses utilize little endian byte ordering. When this bit is set, data FIFO port accesses utilize big endian byte ordering. Please refer to Section 3.8 of the LAN9220 Datasheet for more information on this feature.
- Bit 28 becomes FSELEND, Direct FIFO Access Endian Ordering**.** This control bit determines the endianess of RX and TX data FIFO host accesses when accessed using the FIFO_SEL signal. When this bit is cleared, FIFO_SEL accesses utilize little endian byte ordering. When this bit is set, FIFO_SEL accesses utilize big endian byte ordering. Please refer to Section 3.8 of the LAN9220 Datasheet for more information on this feature.
- Bit 24 becomes AMDIX_EN Strap State. This read-only bit reflects the state of the AMDIX_EN strap pin (pin 52). This pin can be overridden by PHY registers 27.15 and 27.13.
- Bits 15:2 become reserved.

3.2 MAC Register Changes

3.2.1 COE_CR Register (offset: Dh)

The Checksum Offload Engine Control Register (COE_CR), has been added to the LAN9220 at offset Dh. This register controls the transmit and receive checksum offload engines. Please refer to Section 3.6 of the LAN9220 Datasheet for more information on this feature.

- Bits 31:17 - Reserved.
- Bit 16 - TX Checksum Offload Engine Enable (TXCOE_EN). TXCOE_EN may only be changed if the TX data path is disabled. If cleared, the TXCOE is bypassed. If set, the TXCOE is enabled.
- Bits 15:2 - Reserved.
- Bit 1 - RX Checksum Offload Engine Mode (RXCOE_MODE). This bit indicates whether the RXCOE will check for VLAN tags or a SNAP header prior to beginning its checksum calculation. In its default mode, the calculation will always begin 14 bytes into the frame. The RXCOE_MODE may only be changed if the ESS RX path is disabled. If set, begin checksum calculation at the start of L3 packet by adjusting for VLAN tags and/or SNAP header. If cleared, begin checksum calculation after first 14 bytes of the Ethernet Frame.
- Bit 0 - RX Checksum Offload Engine Enable (RXCOE_EN). RXCOE_EN may only be changed if the RX data path is disabled. If cleared, the RXCOE is bypassed. If set, the RXCOE is enabled.

Note: When the RXCOE is enabled, automatic pad stripping must be disabled (MAC_CR bit 8 - PADSTR) and vice versa. These functions cannot be enabled simultaneously.

3.3 PHY Register Changes

3.3.1 PHY Identifier 2 (offset: 4)

The value of this register is changed from 0xC0D1 to 0xC0C3.

3.3.2 Special Control/Status Indications (offset: 27)

- Bit 15 becomes Override AMDIX Strap.
  0 - AMDIX_EN (pin 52) enables or disables HP Auto-MDIX.
  1 - Override pin 52. PHY register 27.14 and 27.13 determine MDIX function.
- Bit 14 becomes Auto-MDIX Enable. Only effective when 27.15 = 1, otherwise ignored.
  0 = disable Auto-MDIX, 27.13 determines normal or reversed connection.
  1 = enable Auto-MDIX, 27.13 must be set to 0.
- Bit 13 becomes Auto-MDIX State. Only effective when 27.15 = 1, otherwise ignored.
  When 27.14 = 0 (manually set MDIX state):
  0 = no crossover (TPO = output, TPI = input)
  1 = crossover (TPO = input, TPI = output).
  When 27.14 = 1 (Auto-MDIX) this bit must be set to 0.
  Do not use the combination 27.15 = 1, 27.14 = 1, 27.13 = 1.

4 Additional Feature Changes

4.1 Mixed Endian Support

In addition to the Word Swap function supported by both the LAN9115 and the LAN9220, the LAN9220 also provides support for mixed endian data FIFO accesses. The LAN9220 provides the ability to select data FIFO endianess separately for accesses through the data FIFO ports (addresses 00h-3Ch) or using the FIFO_SEL input signal. This is accomplished via the FPORTEND and FSELEND bits of the HW_CFG—Hardware Configuration Register, respectively. Please refer to Section 3.7 of the LAN9220 Datasheet for more information.

Note: CSR and status FIFO accesses are not affected by the FPORTEND and FSELEND endianess select bits.

4.2 Checksum Offload Engine (COE)

The LAN9220 contains two checksum offload engines, which offload the calculation of the 16-bit checksum for transmitted and received Ethernet frames. Please refer to Section 3.6 of the LAN9220 Datasheet for detailed information on the use of the COE's. Please note that currently only the Linux driver supports checksum offloading.

4.2.1 Receive Checksum Offload Engine (RXCOE)

The receive checksum offload engine provides assistance to the CPU by calculating a 16-bit checksum for a received Ethernet frame. The RXCOE readily supports the following IEEE 802.3 frame formats:

- Type II Ethernet frames
- SNAP encapsulated frames
- Support for up to 2, 802.1q VLAN tags

4.2.2 Transmit Checksum Offload Engine (TXCOE)

The transmit checksum offload engine provides assistance to the CPU by calculating a 16-bit checksum, typically for TCP, for a transmit Ethernet frame. The TXCOE calculates the checksum and inserts the results back into the data stream as it is transferred to the MAC.

4.2.2.1 TX Command 'B'

The TX Command 'B' bit 14 has changed from Reserved to TX Checksum Enable (CK). When this bit is set in conjunction with the first segment (FS) bit in TX Command 'A' and the TX checksum offload engine enable bit (TXCOE_EN) in the COE_CR register is set, the TX checksum offload engine (TXCOE) will calculate a L3 checksum for the associated frame.

4.3 External PHY

The LAN9220 does not support an external PHY, therefore all signal pins associated with the external PHY on the LAN9115 are no longer available on the LAN9220. These include:

- TX_CLK, TXD[3:0], TX_EN
- RX_CLK, RX_ER, RXD[3:0], RX_DV
- COL, CRS
- MDIO, MDC

  Note: TX_CLK, TX_EN, RX_CLK and RX_DV can still be observed the GPO3 and GPO4 pins.

5 Driver Support

Table 5.1 below shows the version of drivers needed to support the LAN9220.

Table 5.1 Driver Support

DRIVER	REVISION
WinCE 5.0 - XScale (PXA270)	1.3 or later
Linux - XScale (PXA270)	1.56 or later
VXWorks 5.5 (SH3)	2.08 or later

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123