MIC68400 Evaluation Board



4A Sequencing LDO with Tracking and Ramp Control™

General Description

The MIC68400 is a high peak current LDO regulator designed specifically for powering applications such as FPGA core voltages that require high start up current with lower nominal operating current. Capable of sourcing 4A of current from start-up, the MIC68400 provides high power from a small MLF leadless package. The MIC68400 can also implement a variety of power-up and power-down protocols such as sequencing, tracking, and ratiometric tracking.

The MIC68400 operates from a wide input range of 1.65V to 5.5V. The MIC68400 incorporates a delay pin (Delay) for control of power on reset output (POR) at turn-on and power-down delay at turn-off. In addition there is a ramp control pin (RC) for either tracking applications or output voltage slew rate adjustment at turn-on and turn-off. On board jumpers allow selection of on board delay caps, tracking, or sequencing mode.

Features

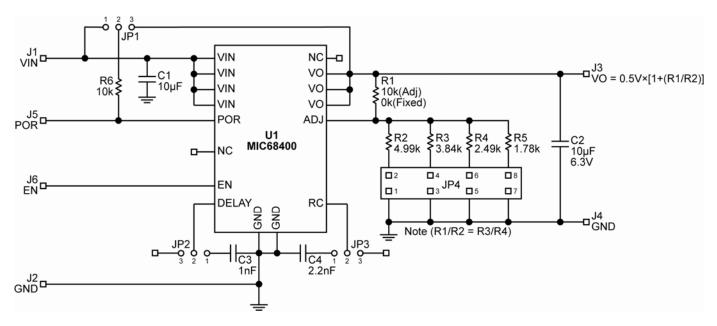
- Stable with 10uF ceramic capacitor
- Input voltage range: 1.65V to 5.5V
- Adjustable output voltage down to 0.5V
- 4A maximum output current peak start up
- 3A Continuous Operating Current
- Tracking on turn-on and turn-off
- Timing Controlled Sequencing
- Programmable Ramp Control™
- Power-on Reset (POR) supervisor with programmable delay time
- Tiny 4mm x 4mm MLFTM package

Terminal Description

PCB Connections	Terminal Name	Terminal Function
J1	VIN	Input
J2	GND	Ground
J3	VOUT	Output
J4	GND	Ground
J5	POR	Power On Reset (Power Good Flag)
J6	EN	Enable

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Schematic



Programming Jumpers

Jumper Number	Jumper Name	Jumper Function	
JP1	POR1 Source	[1:2] – Use VIN1; [2:3] – Use VC	O1 (min Q Current)
JP2	Delay1 Source	[1:2] – Use C3 (on board delay);	[2:3] - NC (min delay)
JP3	RC1 Source	[1:2] – Use C4 (on board ramp slope);	[2:3] - NC (min ramp slope)
JP4	ADJ Voltage Select	[1:2] – 1.5V [3:4] – 1.8V [5:6] No Jumper – (– 2.5V [7:8] – 3.3V 0.5V

Ordering Information

Part Number	Description
MIC68400YML EV	Evaluation board with MIC68400YML adjustable device.

NOTE: For additional voltage options, contact Micrel Marketing.

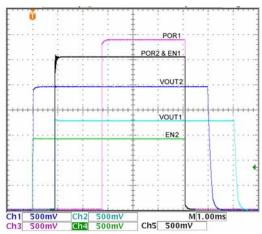
Applications InformationTypical Jumper Connections (Using two MIC68400YML EV boards)

Description	Enable Input	VIN1 & VIN2 J1	JP1 POR 1	JP2 DLY 1	JP3 RC 1	JP4 VO 1	JP5 POR 2	JP6 DLY 2	JP7 RC 2	JP8 VO 2	J6 EN 1	J6 EN 2
Delayed Sequencing: U2 Master w/ VOUT = 2.5V U1 Slave w/ VOUT = 1.8V	U2 J6	3.3V	1:2	1:2 2nF	2:3	3:4	1:2	1:2	2:3	5:6	U2 POR	EXT
Windowed Sequencing: U1 Master w/ VOUT = 2.5V U2 Slave w/ VOUT = 1.8V	U1 J6	3.3V	1:2	1:2 2nF	2:3	5:6	1:2	1:2	2:3	3:4	EXT	U1 POR
Normal Tracking: U1 Master w/ VOUT = 2.5 V U2 Slave w/ VOUT = 1.8V	U1, U2 J6	3.3V	1:2	1:2	1:2	5:6	1:2	2:3	U1 VO (1)	3:4	EXT	EXT
Ratiometric Tracking: U1 Master w/ VOUT = 2.5 V U2 Slave w/ VOUT = 1.8V	U1, U2 J6	3.3V	1:2	1:2	1:2 3nF	5:6	1:2	2:3	U1 RC	3:4	EXT	EXT

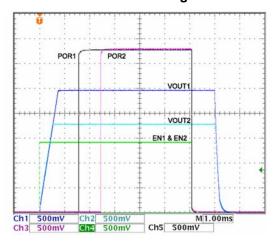
Note:

1. Requires external resistor divider connected to output pin of unit 1.

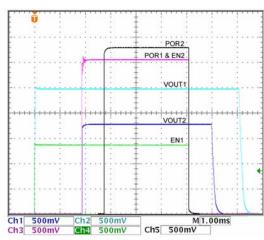
Delayed Sequencing



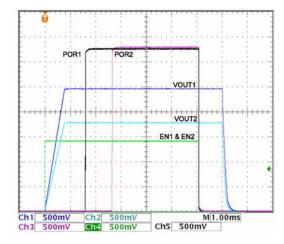
Normal Tracking



Windowed Sequencing



Ratiometric Tracking



MIC68400 Micrel, Inc.

Enable Input

The enable input is programmed via J6. The MIC68400 may be enabled 3 ways:

- 1) From VIN (short EN and VIN jumpers),
- 2) From POR of adjacent device (Connect EN to POR output of adjacent device)
- 3) From External source (drive the EN jumper)

Voltage Adjustment

Target voltage for the MIC68400 is controlled via JP4. Jumper settings are:

- 1) Pins 1&2 - 1.5V
- 2) Pins 3&4 - 1.8V
- 3) Pins 5&6 - 2.5V
- Pins 7&8 3.3V4)

Other voltages are possible by changing resistor values or adding a resistance from the adjust pin to GND. The formula for output voltage given resistance R from device adjust pin to GND is:

$$VOUT = 0.5 \times (1 + (10.0 \text{K/R}))$$

NOTE: If the MIC68400 adjustable device is replaced by a fixed device, R1 should be shorted or replaced with a low value resistor (1 Ohm).

Power on Reset (POR)

POR may be observed via J5. Jumper JP1 allows the POR pullup resistor to be supplied from either VIN (Pins 1&2 shorted) or VOUT (Pins 2&3 shorted).

Delay Programming

The Delay is programmed via JP2. For delay can be either minimum (Open, or Pins 2&3 shorted) or approximately 1mSec (Pins 1&2 shorted).

Ramp Control

Ramp Control and Tracking is programmed via JP3. Shorting Pins 1&2 sets the output turn-on slew time (time from turn on to full output) to approximately 0.5mSec for U1.

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2	GRM188R60J106ME47D	muRata	10μF/6.3V X5R	2
	C1608X5R0J106K	TDK		
	JMK107 BJ106MA	TAIO YUDEN		
	08056D106KAT	AVX	10uF/10V X5R	
C3	VJ0603A102KXQPW1BC	Vitramon	1nF/10V	1
C4	VJ0603Y222KXXCW1BC	Vitramon	2.2nF/25V	1
R1, R6	CRCW06031002FKEYE3	Vishay Dale	10K , 0603, 1/16W, 1%	2
R1	CRCW06030000FKEYE3	Vishay Dale	Fixed Voltage: 0 Ohm , 0603, 1/16W, 1%, R2-R5 open	1
R2	CRCW06034991FKEYE3	Vishay Dale	4.99K , 0603, 1/16W, 1%	1
R3	CRCW06033831FKEYE3	Vishay Dale	3.83K , 0603, 1/16W, 1%	1
R4	CRCW06032491FKEYE3	Vishay Dale	2.49K , 0603, 1/16W, 1%	1
R5	CRCW06031781FKEYE3	Vishay Dale	1.78K , 0603, 1/16W, 1%	1
U1	MIC68400YML	Micrel, Inc.	4A FPGA LDO Regulator	1

Notes:

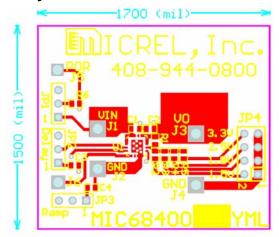
1. AVX: www.avx.com 2. Murata: <u>www.murata.com</u> 3. TDK: www.tdk.com 4. Vishay: www.vishay.com

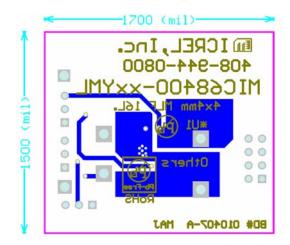
5. Taiyo Yuden: www.t-yuden.com

6. Vitramon: www.vitramon.com

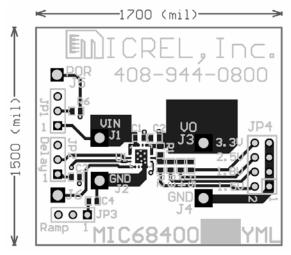
7. Micrel Semiconductor: www.micrel.com

PCB Layout Artwork





TOP **BOTTOM**



TOP SILKSCREEN

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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