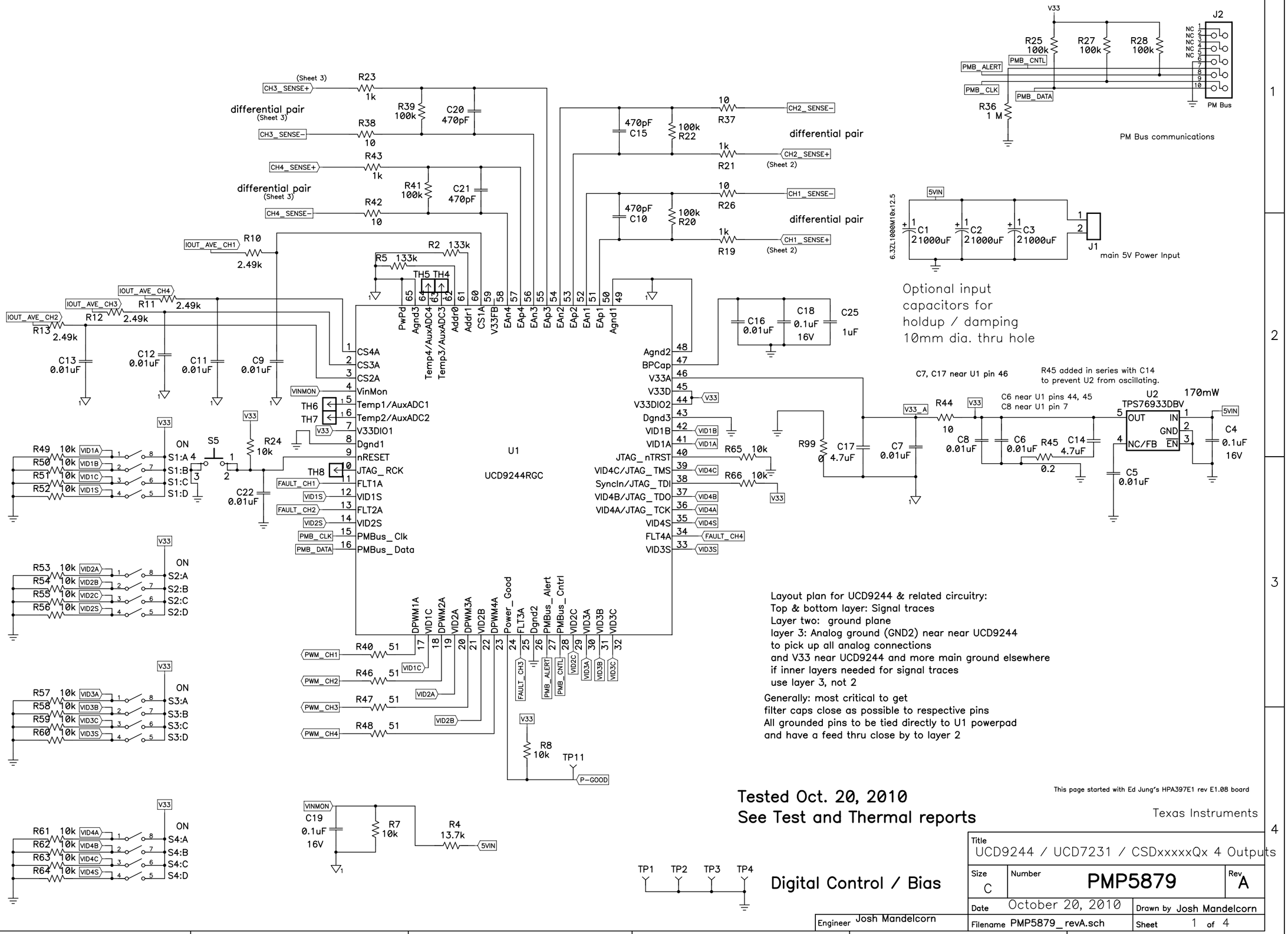
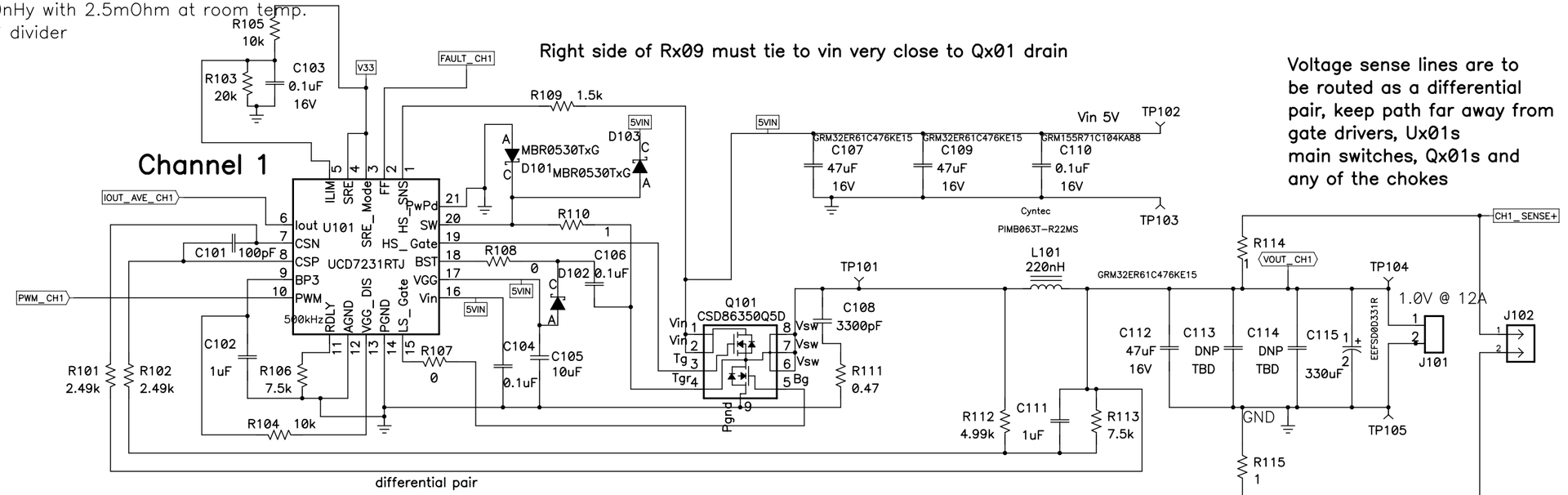
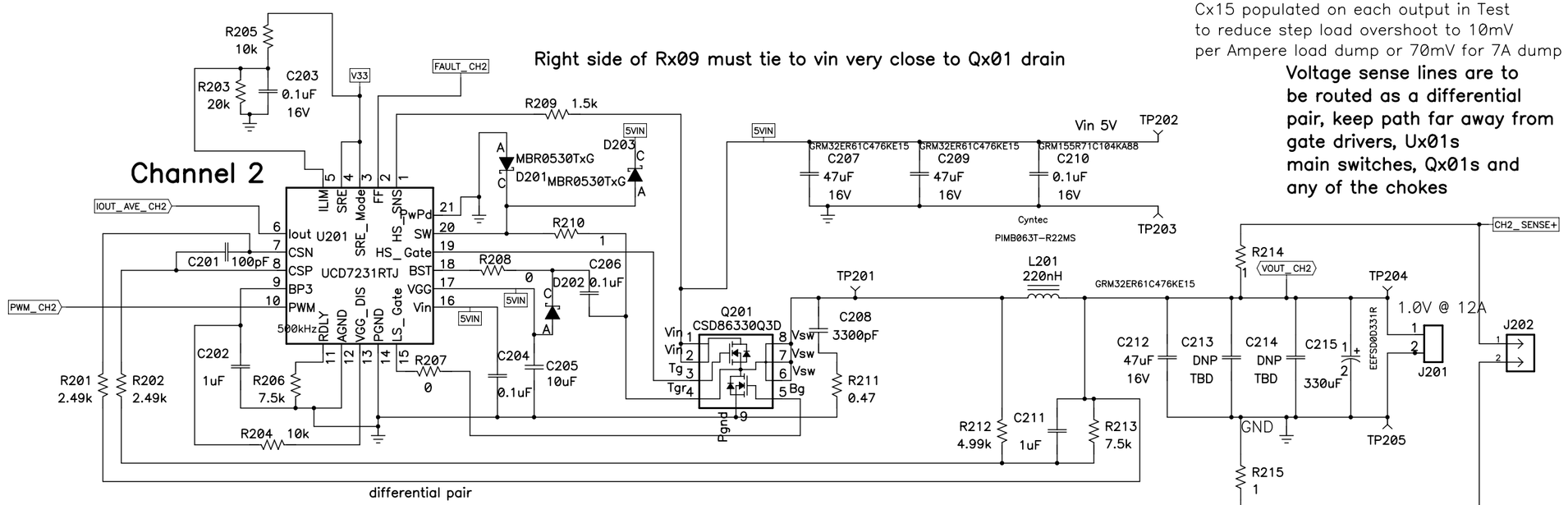

(Sheet 3)
CH3_SENSE+
R23
1k
differential pair
(Sheet 3)
CH3_SENSE-
R38
10
R39
100k
C20
470pF
CH4_SENSE+
R43
1k
differential pair
(Sheet 3)
CH4_SENSE-
R42
10
R41
100k
C21
470pF
IOUT_AVE_CH1
R10
2.49k
R2 133k
R5 133k
TH5 TH4
IOUT_AVE_CH4
IOUT_AVE_CH3
R11 2.49k
IOUT_AVE_CH2
R12 2.49k
R13 2.49k
C13 0.01uF
C12 0.01uF
C11 0.01uF
C9 0.01uF
PwPd
Agnd3
Temp4/AuxADC4
Temp3/AuxADC3
Addr0
Addr1
CS1A
V33FB
EAn4
EAp4
EAn3
EAp3
EAn2
EAp2
EAn1
EAp1
Agnd1
1 CS4A
2 CS3A
3 CS2A
4 VinMon
5 Temp1/AuxADC1
6 Temp2/AuxADC2
7 V33DIO1
8 Dgnd1
9 nRESET
10 JTAG_RCK
11 FLT1A
12 VID1S
13 FLT2A
14 VID2S
15 PMBus_Clk
16 PMBus_Data
U1
UCD9244RGC
Agnd2 48
BPCap 47
V33A 46
V33D 45
V33DIO2 44
Dgnd3 43
VID1B 42
VID1A 41
JTAG_nTRST 40
VID4C/JTAG_TMS 39
SyncIn/JTAG_TDI 38
VID4B/JTAG_TDO 37
VID4A/JTAG_TCK 36
VID4S 35
FLT4A 34
VID3S 33
C16 0.01uF
C18 0.1uF 16V
C25 1uF
470pF C15
100k R22
10 R37
1k R21
(Sheet 2)
CH2_SENSE-
CH2_SENSE+
differential pair
470pF C10
100k R20
10 R26
1k R19
(Sheet 2)
CH1_SENSE-
CH1_SENSE+
differential pair
R65 10k
R66 10k
R99 0
C17 4.7uF
C7 0.01uF
V33_A
R44 10
C8 0.01uF
C6 0.01uF
R45 0.2
C14 4.7uF
C5 0.01uF
U2 TPS76933DBV 170mW
OUT
IN
GND
NC/FB
EN
C4 0.1uF 16V
C7, C17 near U1 pin 46
R45 added in series with C14
to prevent U2 from oscillating.
C6 near U1 pins 44, 45
C8 near U1 pin 7
R49 10k VID1A
R50 10k VID1B
R51 10k VID1C
R52 10k VID1S
S5
ON
S1:A
S1:B
S1:C
S1:D
R24 10k
C22 0.01uF
TH6
TH7
TH8
FAULT_CH1
FAULT_CH2
R53 10k VID2A
R54 10k VID2B
R55 10k VID2C
R56 10k VID2S
S2:A
S2:B
S2:C
S2:D
R57 10k VID3A
R58 10k VID3B
R59 10k VID3C
R60 10k VID3S
S3:A
S3:B
S3:C
S3:D
R61 10k VID4A
R62 10k VID4B
R63 10k VID4C
R64 10k VID4S
S4:A
S4:B
S4:C
S4:D
DPWM1A
VID1C
DPWM2A
VID2A
DPWM3A
VID2B
DPWM4A
Power_Good
FLT3A
Dgnd2
PMBus_Alert
PMBus_Cntrl
VID2C
VID3A
VID3B
VID3C
FAULT_CH3
PMB_ALERT
PMB_CNTL
PWM_CH1
PWM_CH2
PWM_CH3
PWM_CH4
R40 51
R46 51
R47 51
R48 51
R8 10k
TP11
P-GOOD
VINMON
C19 0.1uF 16V
R7 10k
R4 13.7k
5VIN
TP1
TP2
TP3
TP4
V33
R36 1 M
R25 100k
R27 100k
R28 100k
PMB_ALERT
PMB_CNTL
PMB_CLK
PMB_DATA
J2
NC
PM Bus
PM Bus communications
5VIN
6.3ZL1000M10x12.5
C1 21000uF
C2 21000uF
C3 21000uF
J1
main 5V Power Input
Optional input
capacitors for
holdup / damping
10mm dia. thru hole
Layout plan for UCD9244 & related circuitry:
Top & bottom layer: Signal traces
Layer two: ground plane
layer 3: Analog ground (GND2) near near UCD9244
to pick up all analog connections
and V33 near UCD9244 and more main ground elsewhere
if inner layers needed for signal traces
use layer 3, not 2
Generally: most critical to get
filter caps close as possible to respective pins
All grounded pins to be tied directly to U1 powerpad
and have a feed thru close by to layer 2
Tested Oct. 20, 2010
See Test and Thermal reports
This page started with Ed Jung's HPA397E1 rev E1.08 board
Texas Instruments
Digital Control / Bias
Title
UCD9244 / UCD7231 / CSDxxxxQx 4 Outputs
Size C
Number PMP5879
Rev A
Date October 20, 2010
Drawn by Josh Mandelcorn
Engineer Josh Mandelcorn
Filename PMP5879_revA.sch
Sheet 1 of 4

0.5V + 80mV/A of channel current
at 25 degrees C and
about 0.5V + 100mV/A
at 100 degrees C
for 220nHy with 2.5mOhm at room temp.
and 60% divider



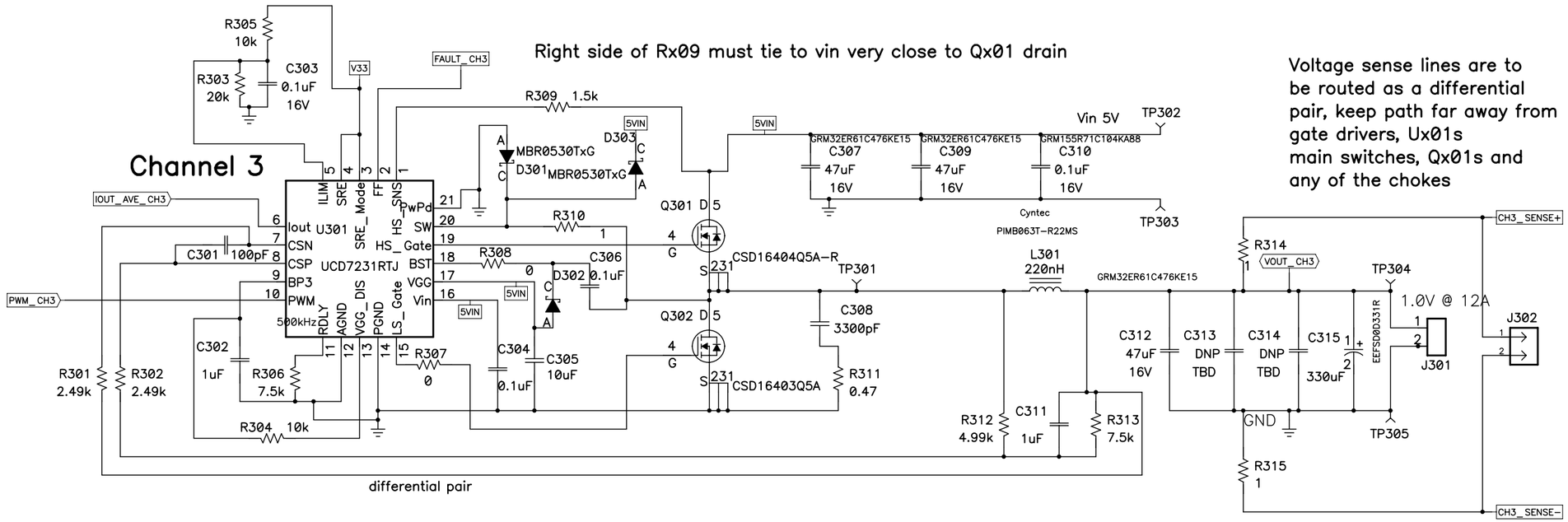



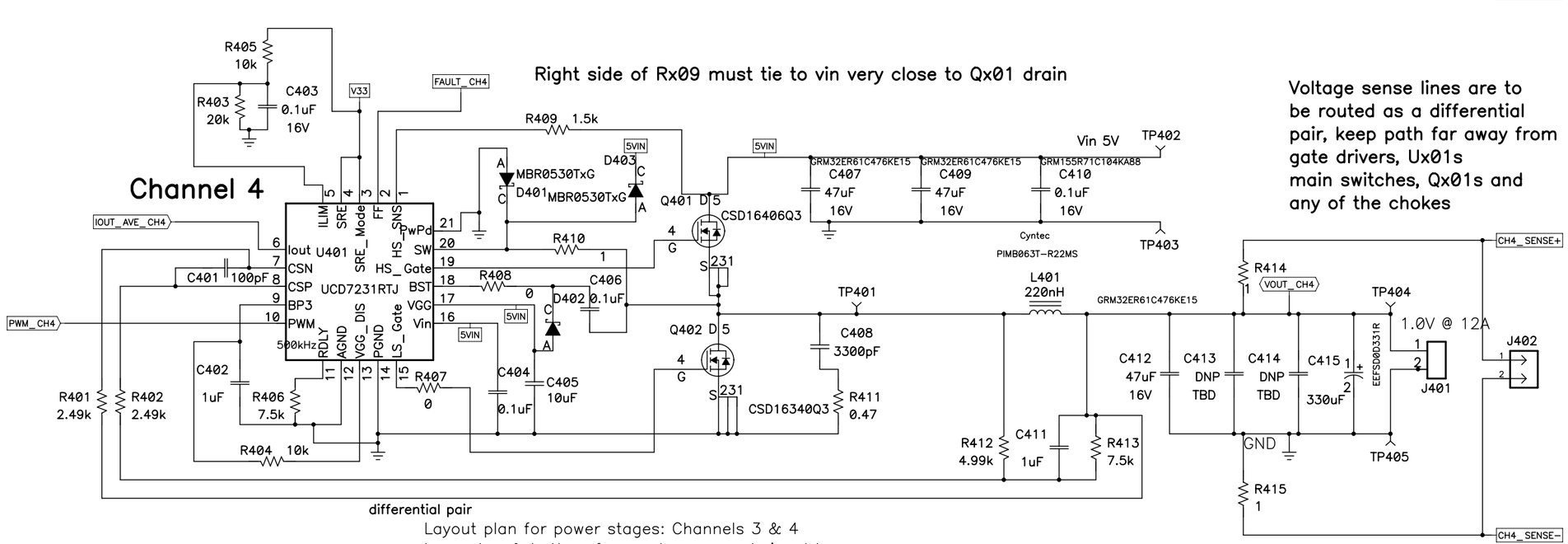

Layout plan for power stages: Channels 1 & 2
layers top & bottom for most power and signal traces
layer 2 will be ground,
power pad of Ux01 & Qx01 to ground with several vias
layer 3 will be 5VIN where needed, but be ground
under and near Q101, Q201
Also provide ground pads on layer 4 as much as feasible
under and near these 2 switches to enhance cooling

## Channels 1 & 2

Texas Instruments

| | | | |
|---|---|---|---|
| Title | UCD9244 / UCD7231 / CSDxxxxQx 4 Outputs | | |
| Size C | Number PMP5879 | | Rev A |
| Date October 20, 2010 | | Drawn by Josh Mandelcorn | |
| Engineer Josh Mandelcorn | Filename PMP5879_revA.sch | Sheet 2 of 4 | |




Layout plan for power stages: Channels 3 & 4
layers top & bottom for most power and signal traces
layer 2 will be ground,
power pad of U301 & U401 to ground with several vias
layer 3 will be 5VIN where needed especially
under and near Q301, Q401 with several vias from under Q301 & Q401
Also provide ground pads on layer 4 as much as feasible
under and near these 2 switches to enhance cooling

## Channels 3 & 4

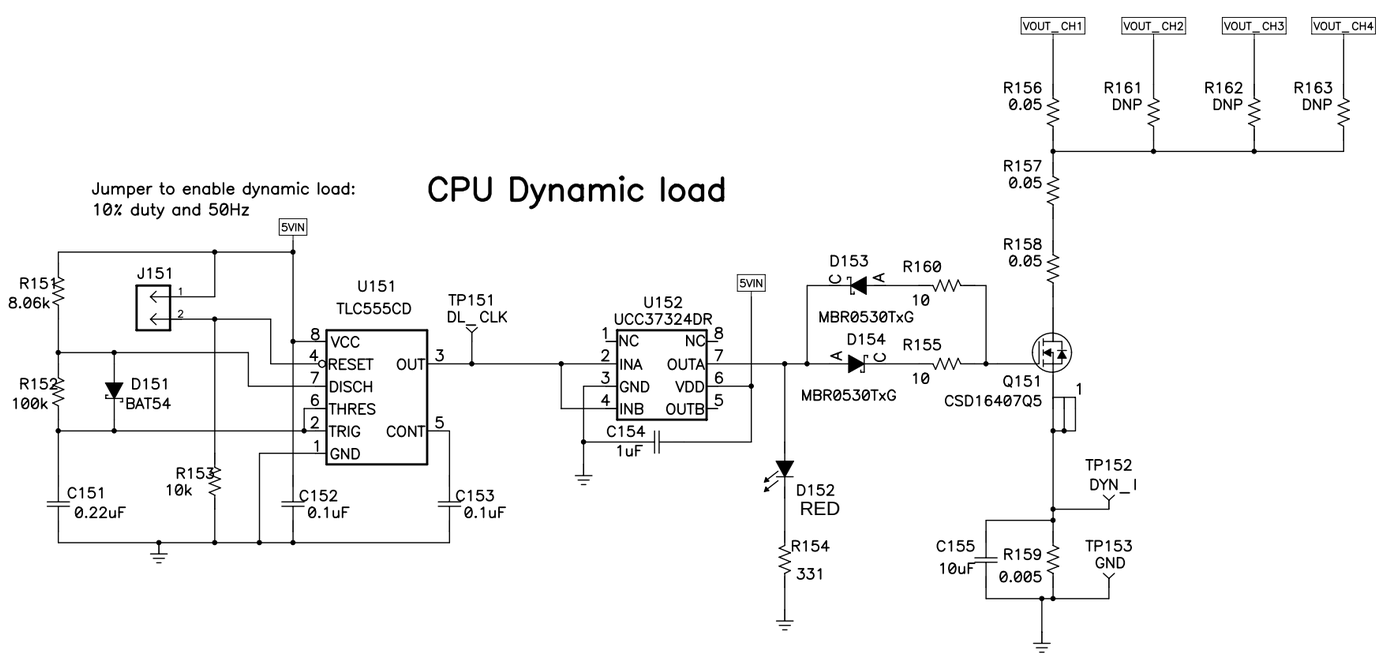
Texas Instruments

| | | | |
|---|---|---|---|
| Title | UCD9244 / UCD7231 / CSDxxxxxQx 4 Outputs | | |
| Size C | Number PMP5879 | | Rev A |
| Date October 20, 2010 | | Drawn by Josh Mandelcorn | |
| Engineer | Filename PMP5879_revA.sch | Sheet 3 of 4 | |

# CPU Dynamic load

Traces to channels need to be 250 mils or 6.3 mm wide.

Jumper to enable dynamic load:
10% duty and 50Hz




## Dynamic Load

Texas Instruments

| | | | |
|---|---|---|---|
| Title: UCD9244 / UCD7231 / CSDxxxxxQx 4 Outputs | | | |
| Size: C | Number: PMP5879 | | Rev: A |
| Date: October 20, 2010 | | Drawn by: Josh Mandelcorn | |
| Engineer: | Filename: PMP5879_revA.sch | Sheet: 4 of 4 | |

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