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See separate Thermal Report for thermal images:
Thermal summary also in this report at bottom page 5:
All testing for this report and the thermal report done on model t1.
Model t3 shipped to customer October 21.

Output conversion efficiency from the 5V input.

Regulation, losses and efficiency (from 5V excluding 81mA when all converters off):

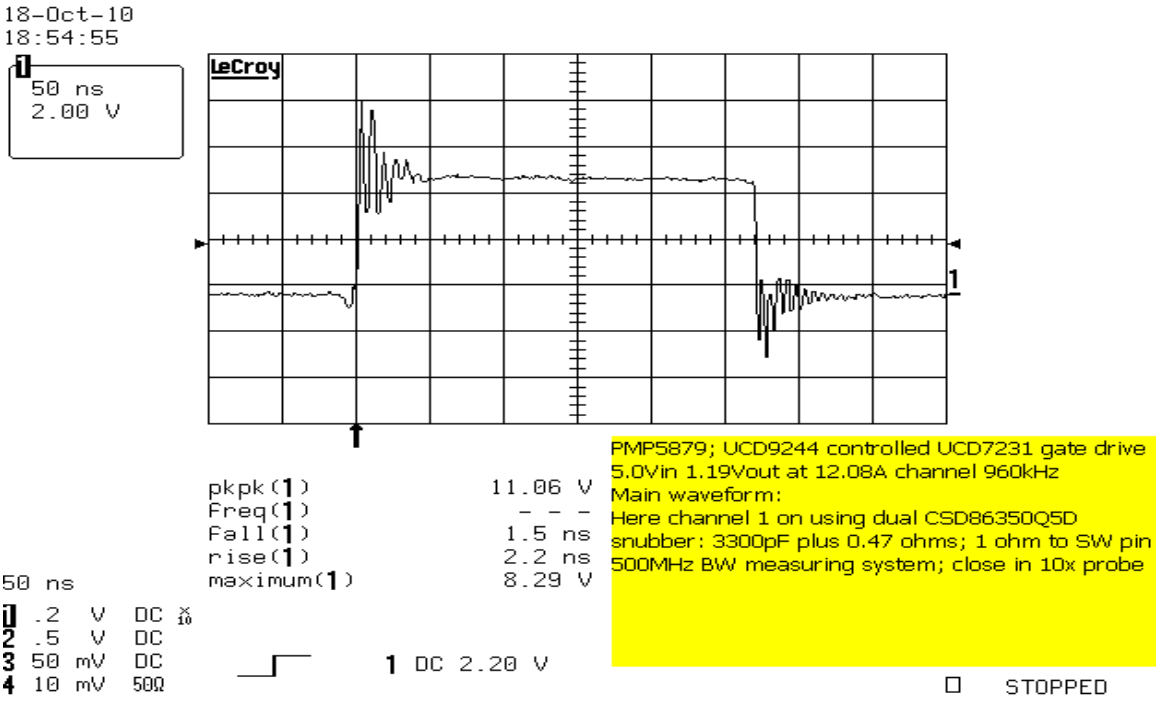
Vin Volts	Iin mA	Vout1 mVolts	Iout1 A	Efficiency %	Losses in mW
Ch. 1 only	5x6	CSD86350	Q5D	960kHz	
5.01	3233	1192	12.08	88.9	1798
5.02	2669	1192	10.08	89.7	1383
5.01	2131	1192	8.08	90.2	1045
5.01	1601	1192	6.08	90.4	774
5.00	1087	1192	4.08	89.5	572
5.00	576	1192	2.08	86.1	401
5.03	323	1192	1.08	79.2	337
5.00	56	1192	0	N/A	280
Ch. 2 only	3x3	CSD86330	Q3D	960kHz	
5.03	3291	1190	12.08	86.8	2179
5.02	2717	1190	10.08	87.9	1644
5.02	2150	1190	8.08	89.1	1178
5.00	1611	1190	6.08	89.8	820
5.00	1081	1191	4.08	89.9	546
5.00	564	1191	2.08	87.8	343
5.04	307	1191	1.08	83.1	261
5.01	45	1191	0	N/A	225

Qq

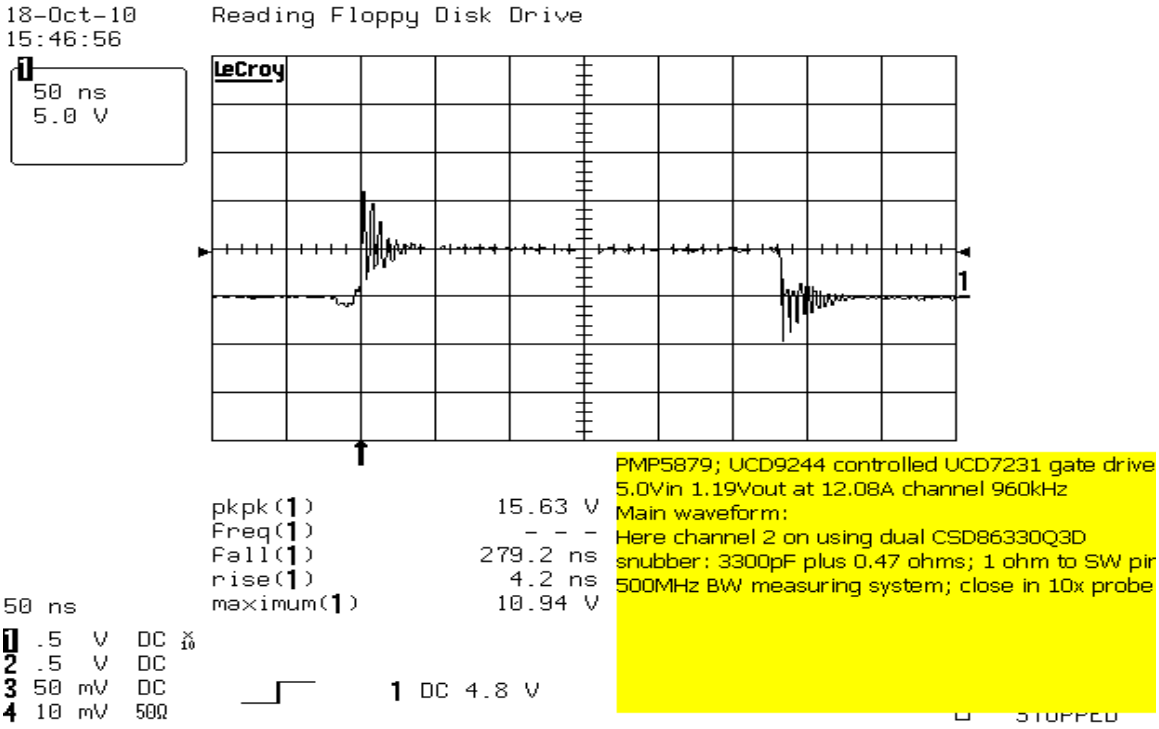
Initial application will be using a dual FET. Hence, Efficiency tests above were done for the two channels that use dual FETs and not the two channels that use discrete FETs. Also, thermal runs show that dual FETs work better thermally than two single FETs with 960kHz operation. See thermal summary page 5.

Major switching waveform for each of 4 channels at full load off 5Vin:

Channel 1:



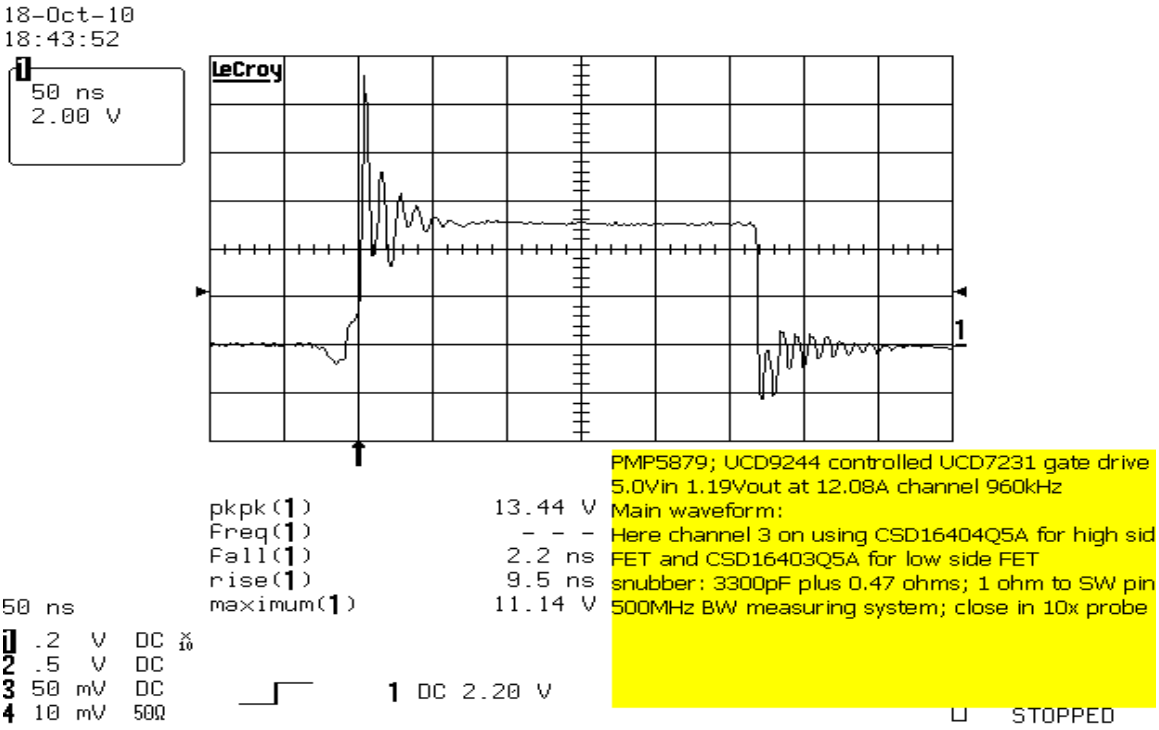
Channel 2:



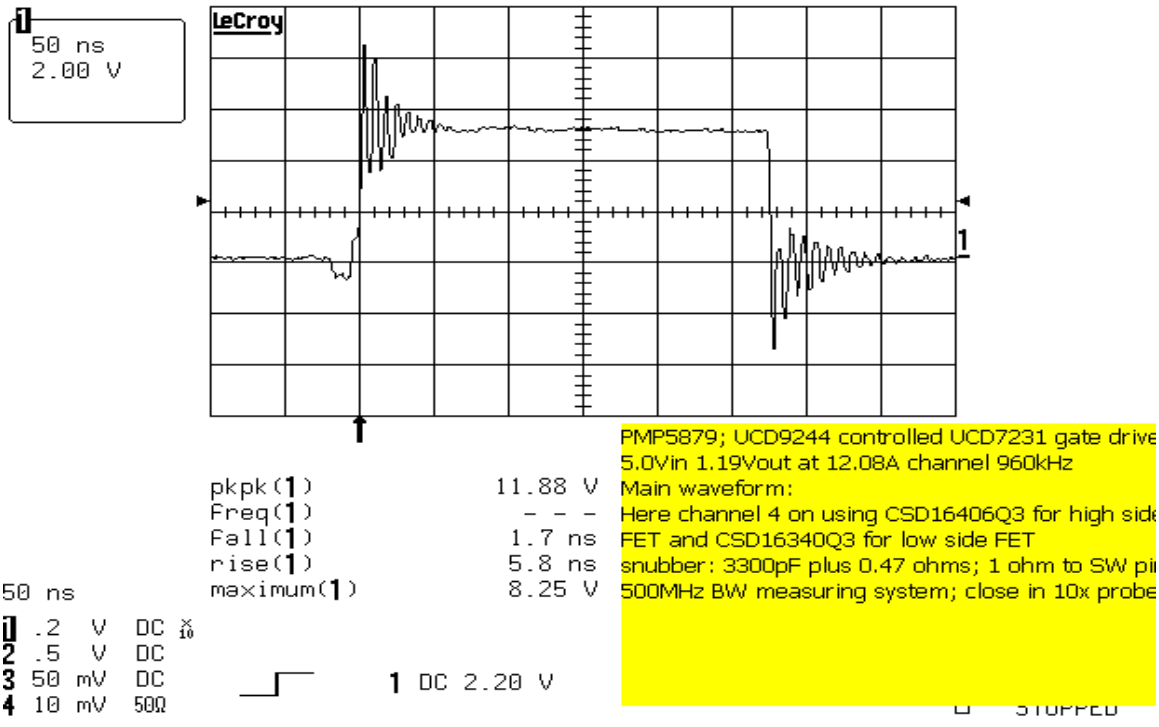
Qq

Major switching waveform for each of 4 channels at full load off 5Vin: (cont.)

Channel 3:

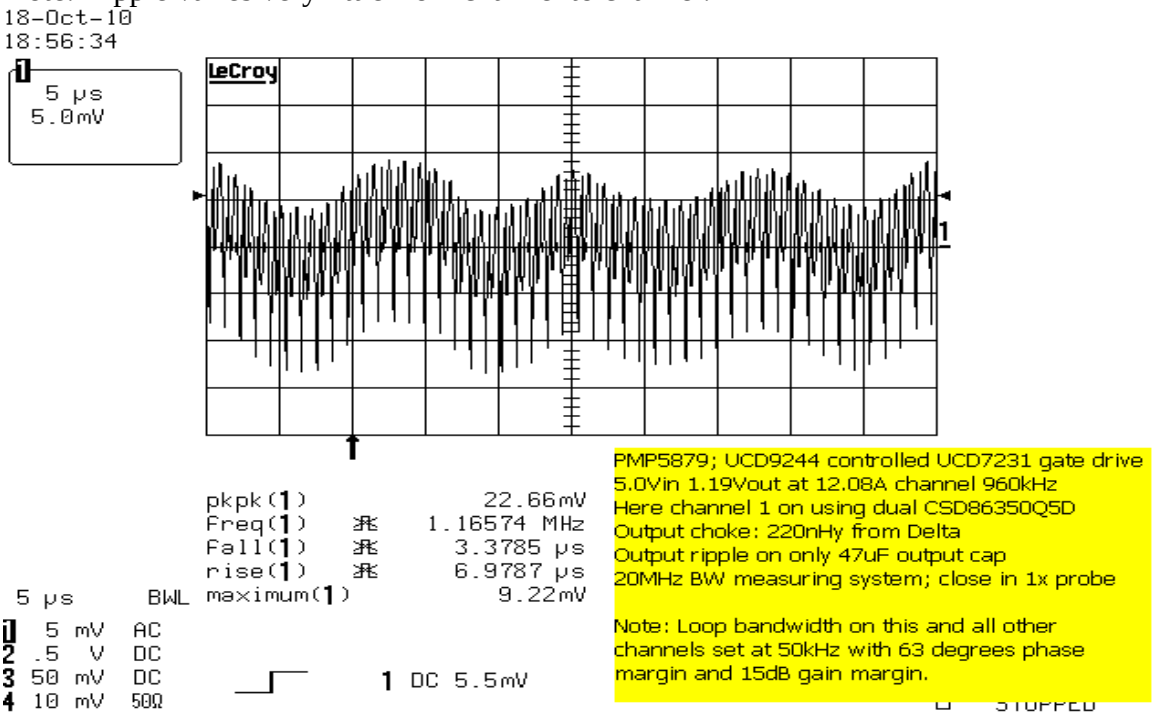


Channel 4:

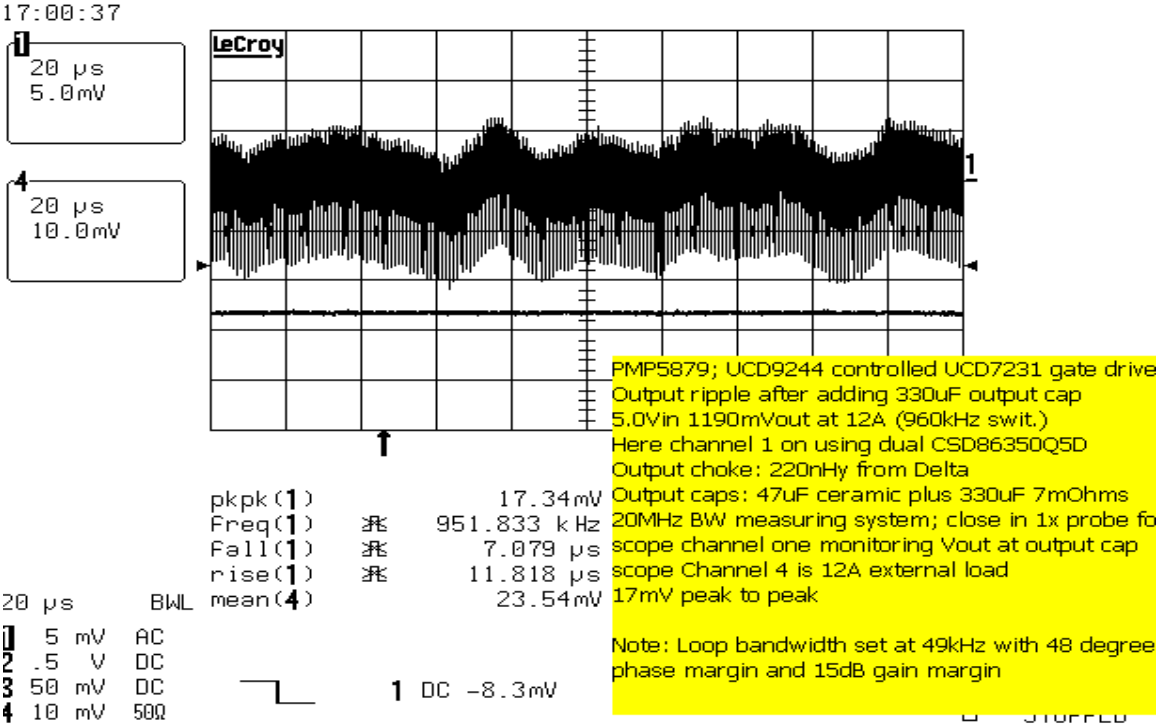


Qq

Output ripple:
Full load ripple when only 47uF output cap used:
Note: Ripple varies very little from channel to channel:

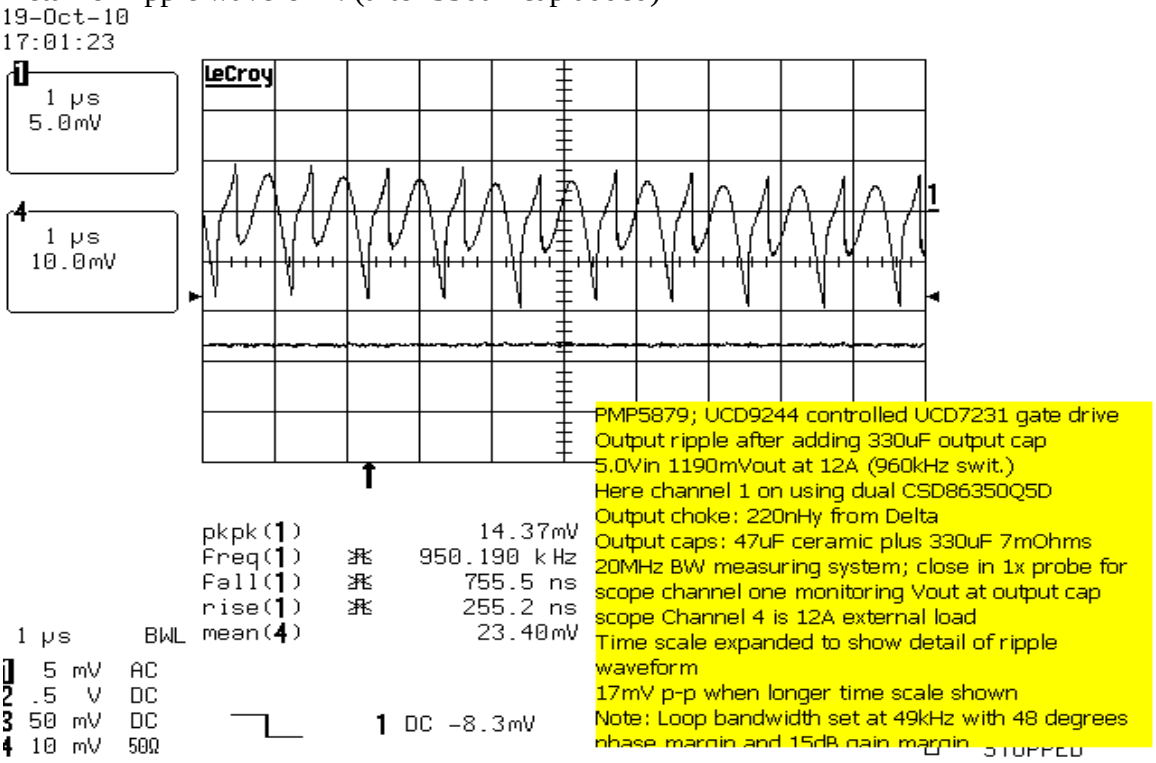


Output ripple after 330uF 7mOhm added:
Note: main reason for adding 330uF was for step load / load dump response, not ripple



Qq

Detail of ripple waveform: (after 330uF cap added)



Qq

Thermal summary:
PMP5279 Thermal Image with one channel on at 1.19V 12.1A off 5.0Vin and 960kHz operation: UCD9244 VID overall controller:

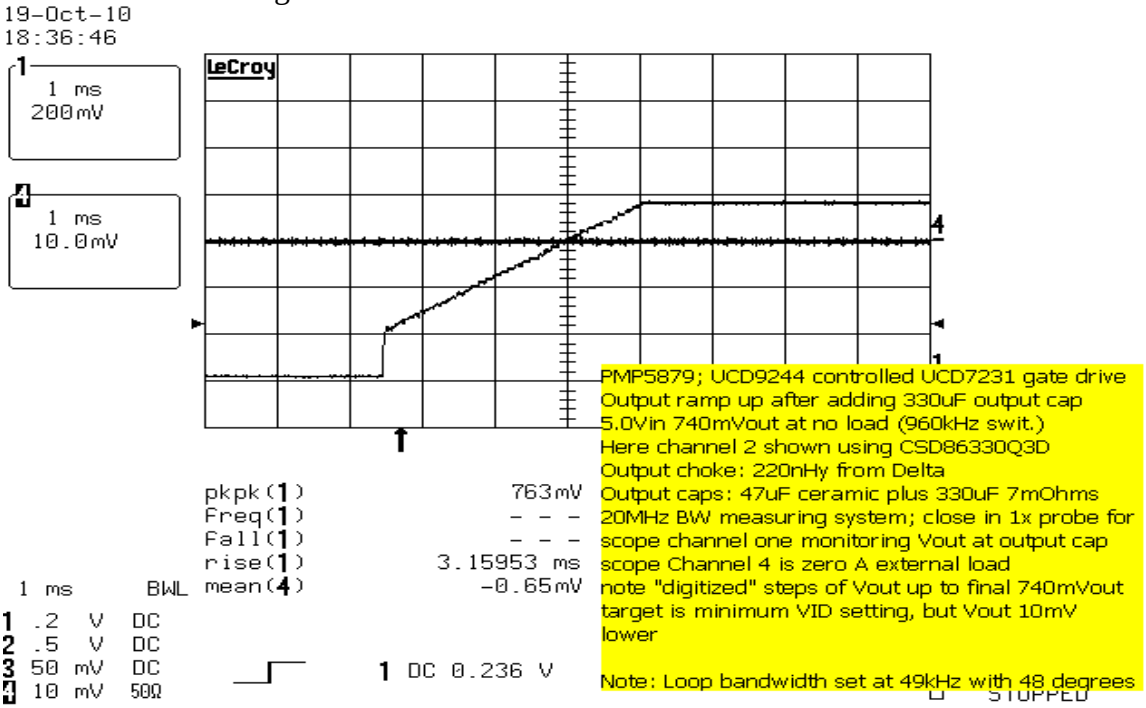
Large Dual FET
Channel 1; main switch is CSD86350Q5D at 47 degrees C;
choke at 47 degrees C peak; ambient 23-25 deg. C

Small Dual FET
Channel 2; main switch is CSD86330Q3D at 54 degrees C;
choke at 52 degrees C peak; ambient 23-25 deg. C

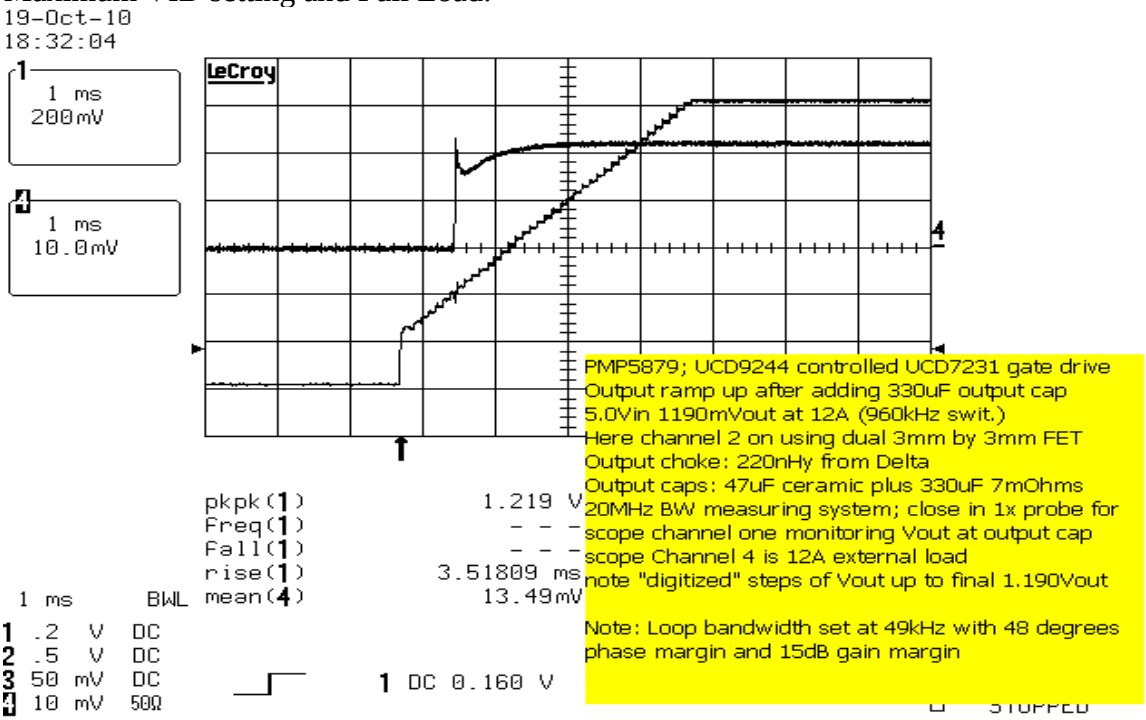
Two large FETs
Channel 3; main switches are CSD16404Q5A & CSD16403Q5A at 49 & 50 degrees C;
choke at 48 degrees C peak; ambient 23-25 deg. C

Two small FETs
Channel 4; main switches are CSD16406Q3 & CSD16340Q3 at 58 & 61.5 degrees C;
choke at 56 degrees C peak; ambient 23-25 deg. C

Start up when channels enabled:
Minimum VID setting and no load:



Maximum VID setting and Full Load:



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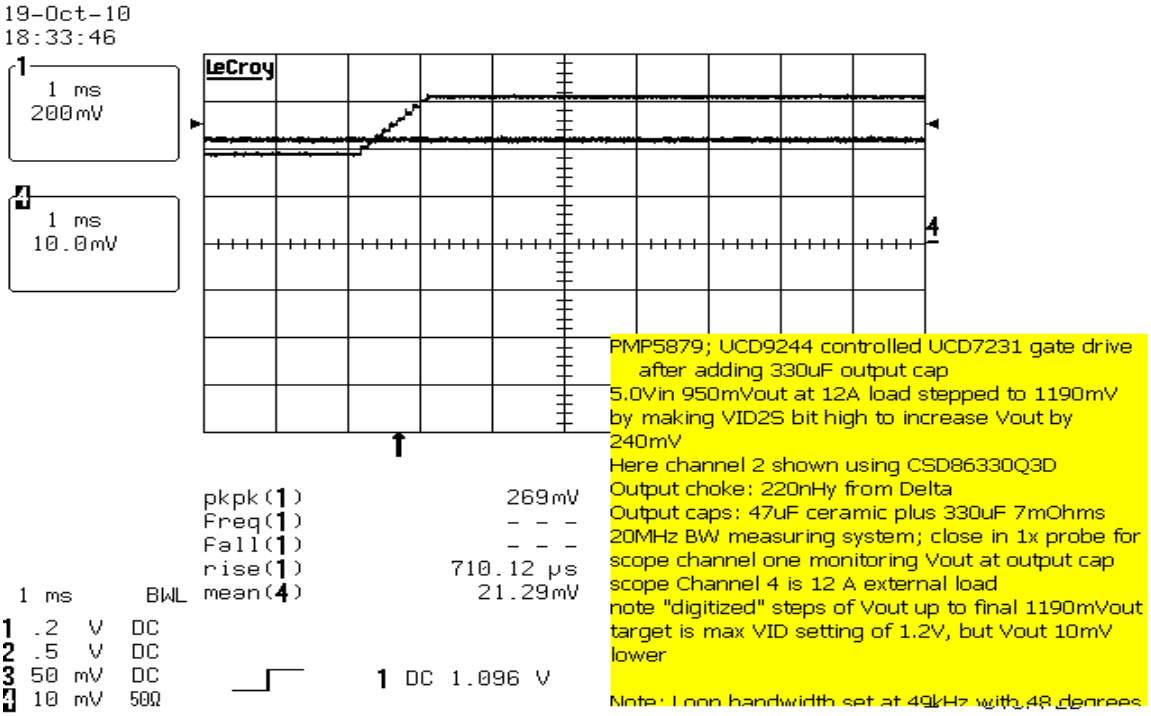
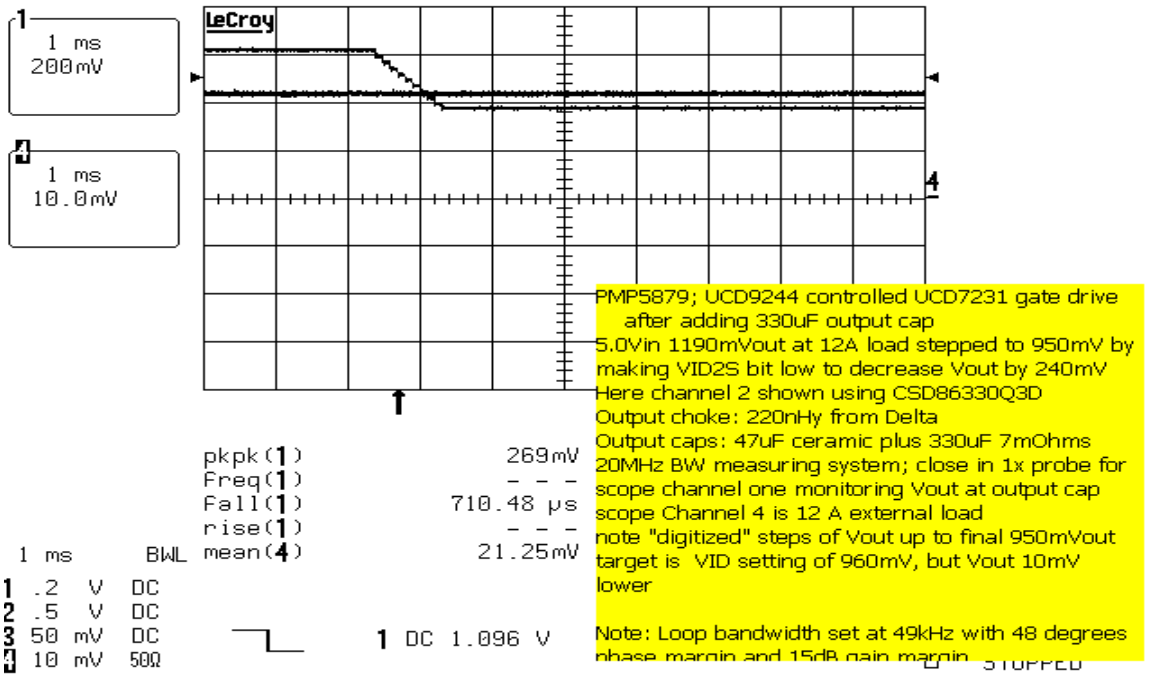
Output transistions when Most significant Bit (MSB) of VID switched:
This bit switches Vout by 240mV:
Bit from zero to one:



Bit from one to zero:



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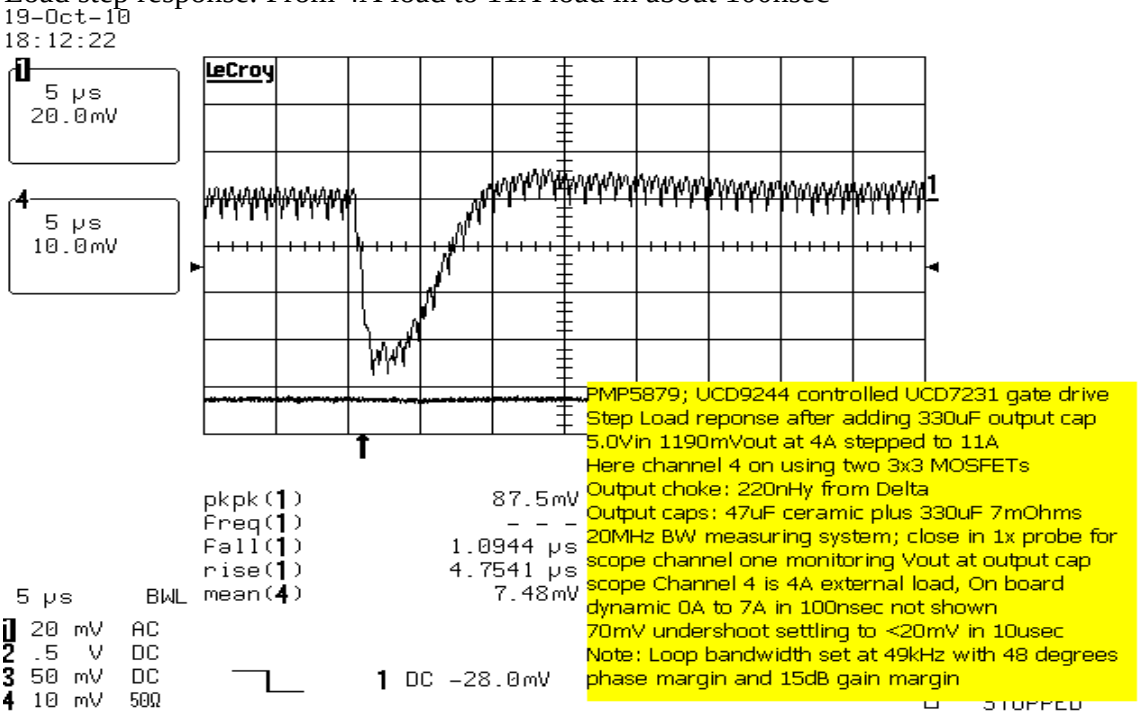
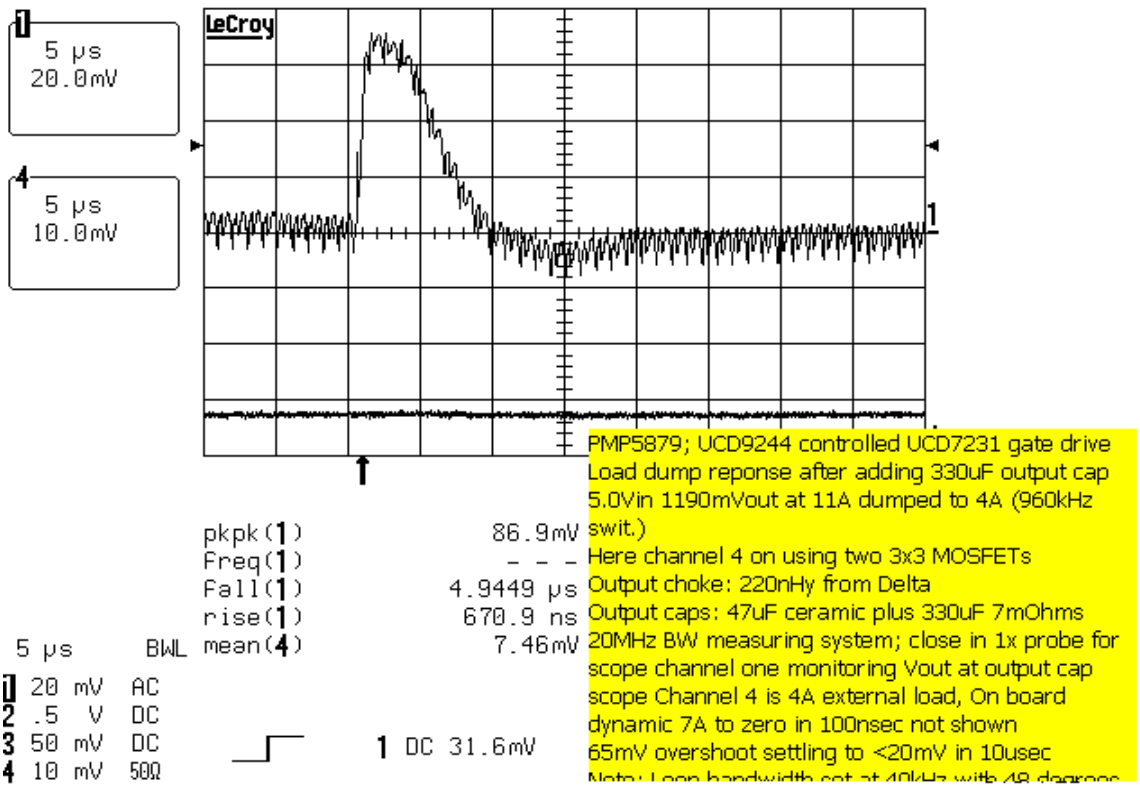
Load step response: From 4A load to 11A load in about 100nsec



Load dump response: From 11A load to 4A load in about 100nsec



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