PMP4591RevC Test Results

The board is built on PCB from PMP4590 Rev.A, with BOM as PMP4590 Rev.C. It is configured for Master operation.
Design calculations are based on MathCad file TPS40140_5V@10A_PMP4591_RevC and MathCad file TPS40140_16V@4A_PMP4590-1_RevC.
Operations of the board together with a slave one (PMP4591_Rev.C) have been also tested.

1 Pictures of the converter

Figure 1 shows the Master Board.
Figure 2, shows Master and Slave Boards, connected for synchronization from Master to Slave.

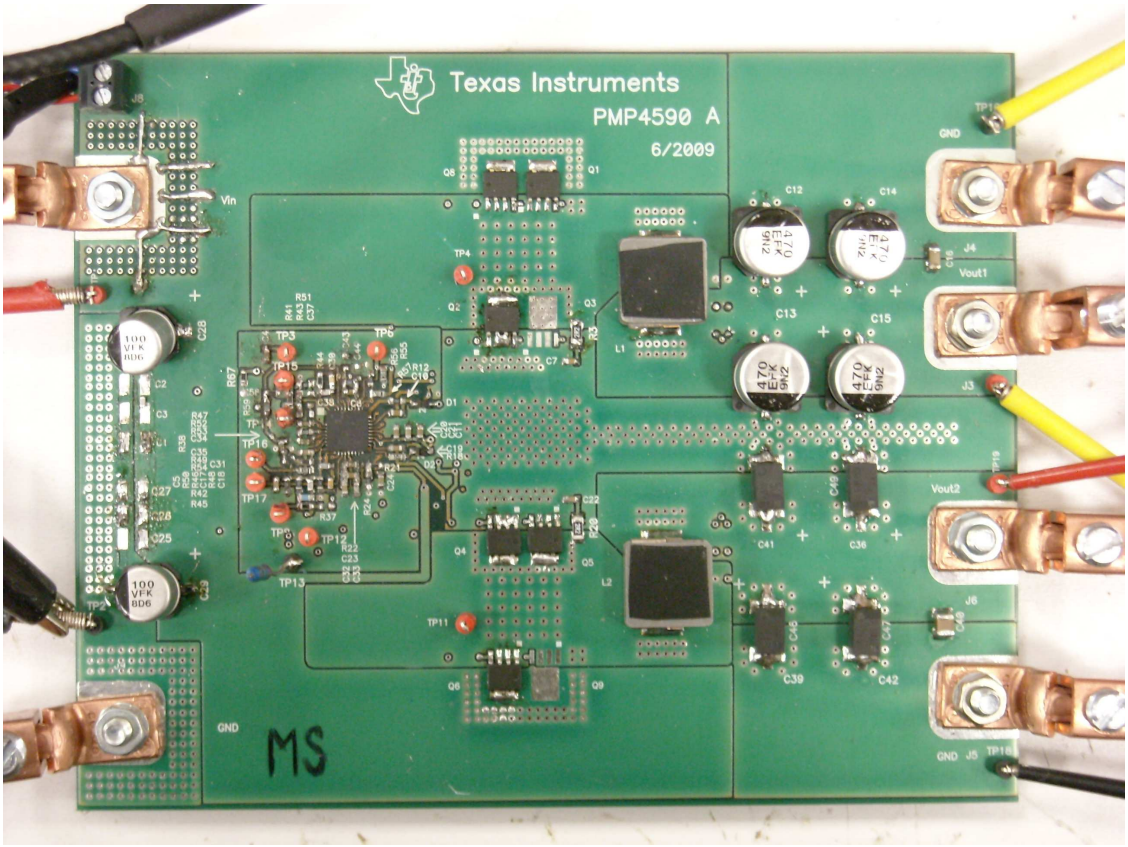

Figure 1

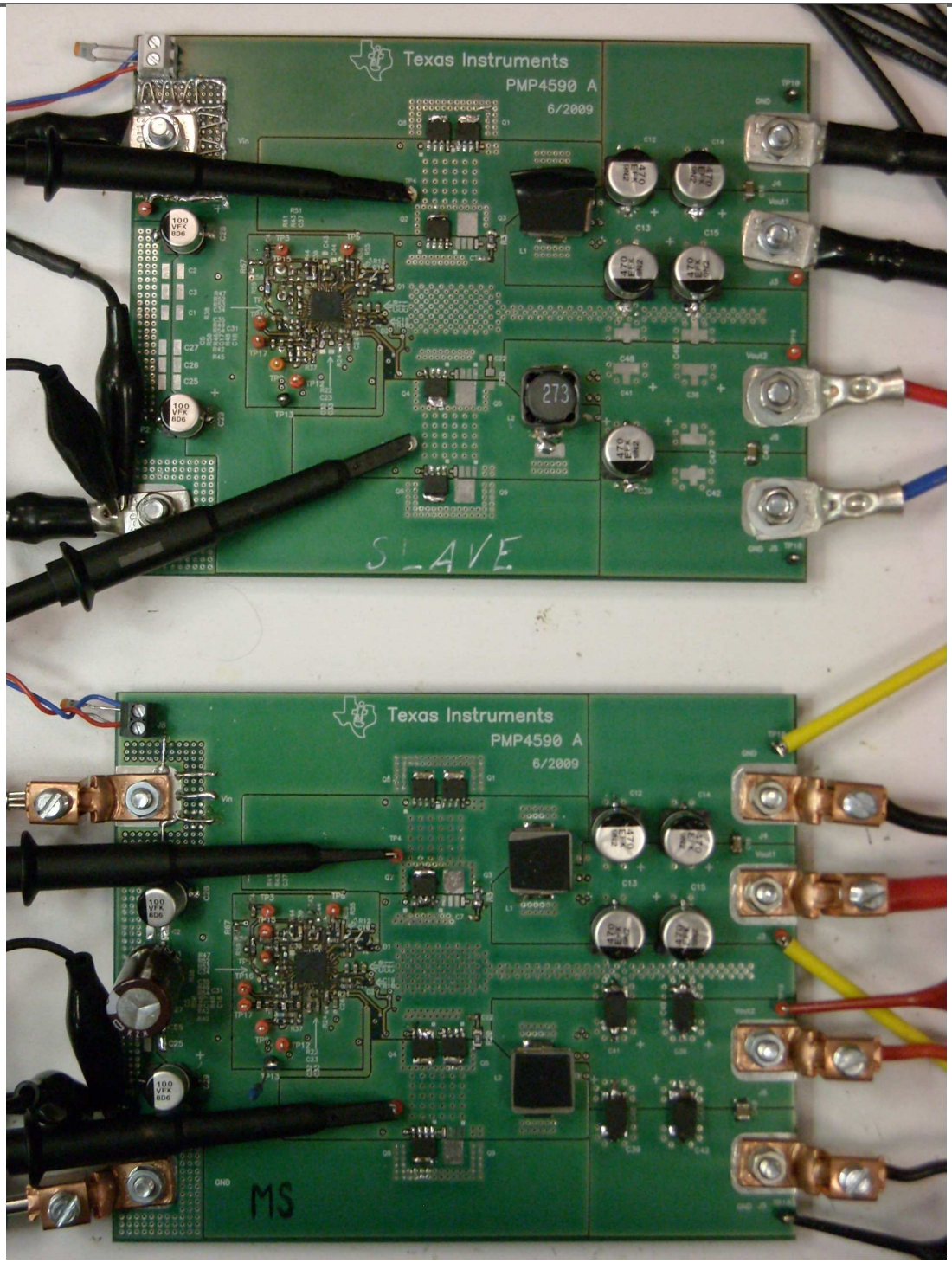
Texas Instruments
PMP4590 A
6/2009
SLAVE
Texas Instruments
PMP4590 A
6/2009
MS

Figure 2

2 Startup

The startup waveform is shown in the Figure 3. The input voltage was set at 25V, with full load on the two outputs (16V and 5V).

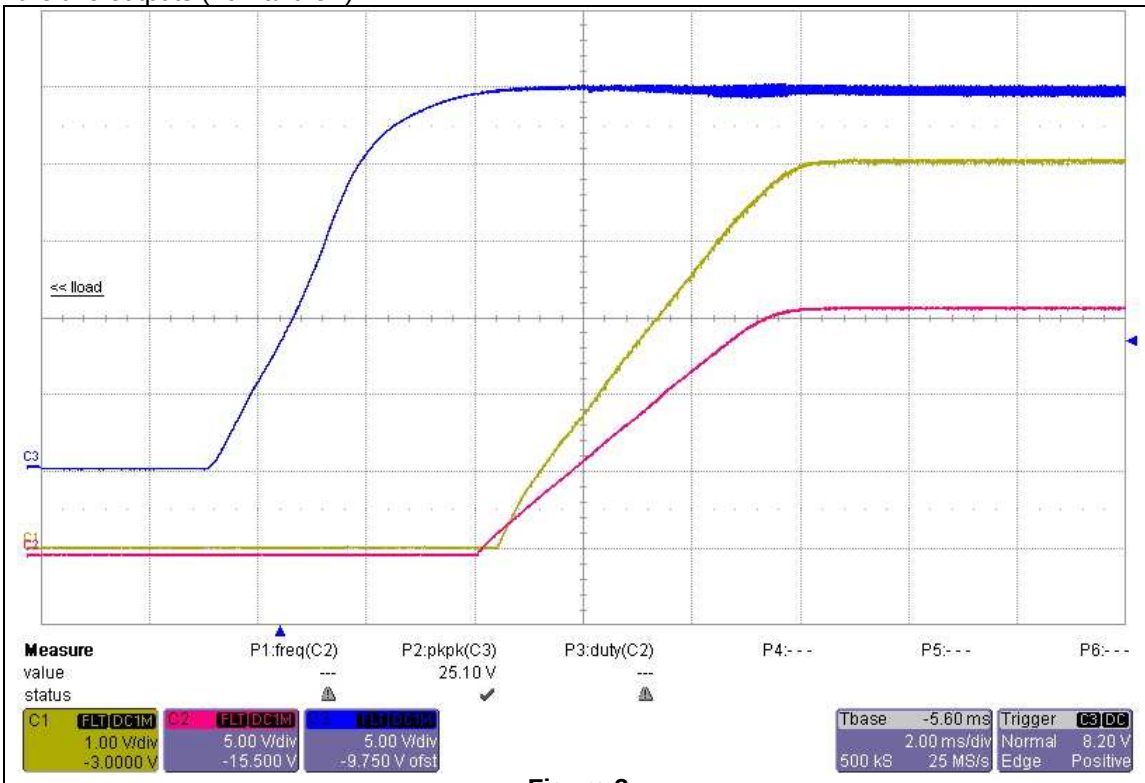

Figure 3

Ch2=> input voltage 10V/div

Ch1=> output voltage1 5V/div (16V)

Ch3=> output voltage2 5V/div

20ms/div

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3 Efficiency

The efficiency curve by varying the IOUT1 (16V /12A) is shown in the Figure 4 below. Input voltage was set at 24V.

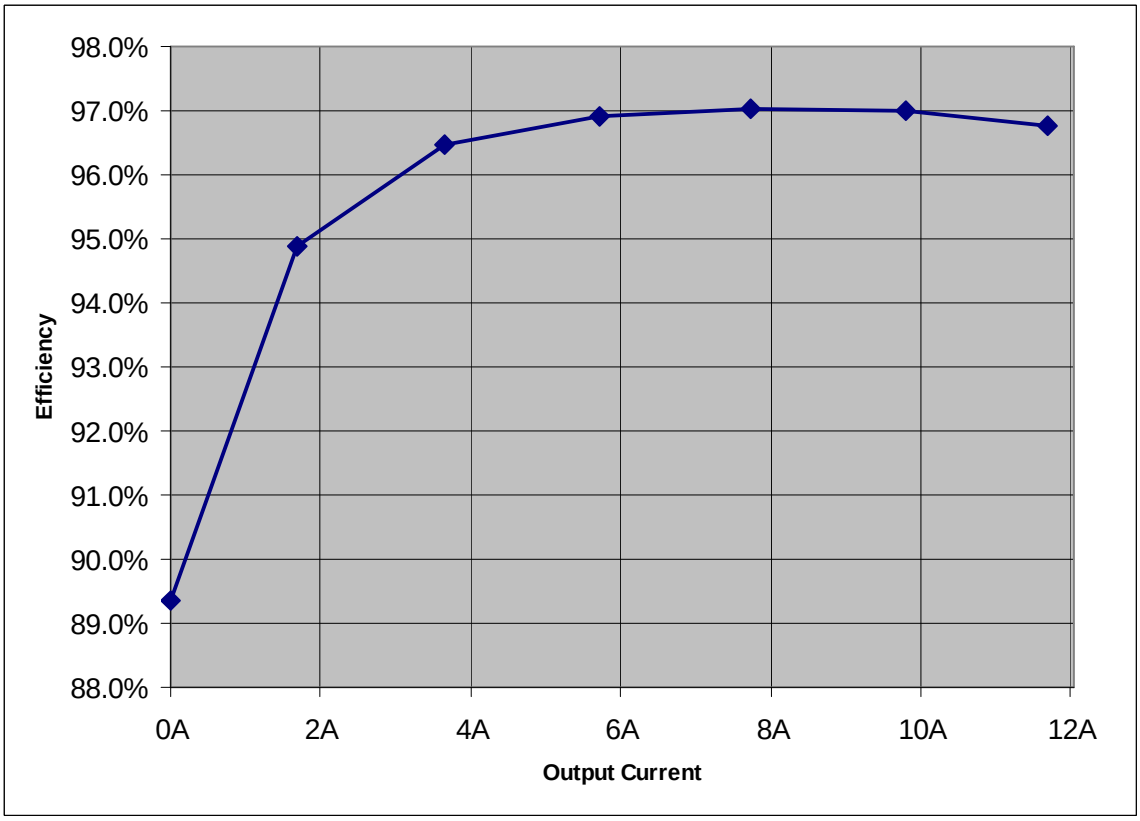


Figure 4

Measured values are in the following table.

VIN[V]	*IIN[A]*	*VOUT1[V]*	*IOUT1[A]*	*VOUT2[A]*	*IOUT2[A]*	*PIN[W]*	*POUT1[W]*	*POUT2[W]*	*POUT [W]*	*Eff [%]*
24.96	9.924	**16.2**	**11.69**	**5.03**	**9.996**	247.7	**189.4**	**50.3**	239.7	**0.968**
24.2	8.91	**16.2**	**9.8**	**5.04**	**9.996**	215.6	**158.8**	**50.4**	209.1	**0.970**
24.35	7.436	**16.21**	**7.73**	**5.04**	**9.996**	181.1	**125.3**	**50.4**	175.7	**0.970**
24.48	6.032	**16.21**	**5.72**	**5.04**	**9.996**	147.7	**92.7**	**50.4**	143.1	**0.969**
24.62	4.614	**16.22**	**3.65**	**5.04**	**9.996**	113.6	**59.2**	**50.4**	109.6	**0.965**
24.74	3.321	**16.22**	**1.7**	**5.04**	**9.996**	82.2	**27.6**	**50.4**	78.0	**0.949**
24.84	2.27	**16.22**	**0**	**5.04**	**9.996**	56.4	**0.0**	**50.4**	50.4	**0.893**

Table 1

The efficiency curve by varying the IOUT2 (5V /10A) is shown in the Figure 5 below.

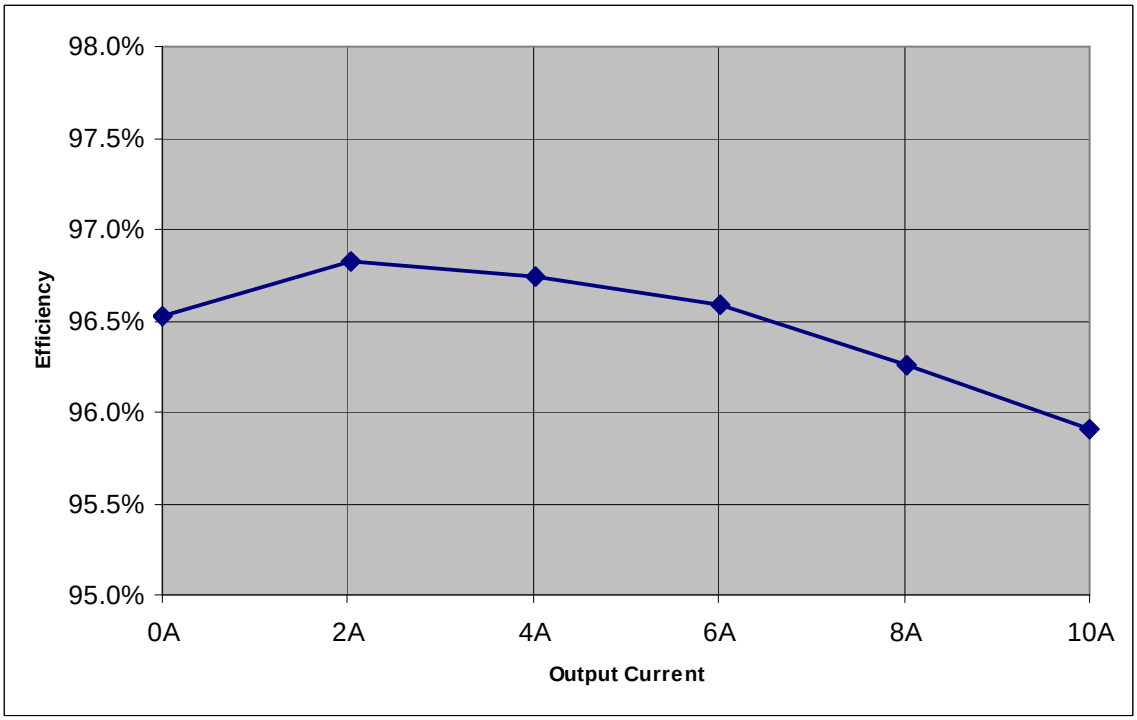


Figure 5

VIN[V]	IIN[A]	VOUT1[V]	IOUT1[A]	VOUT2[A]	IOUT2[A]	PIN[W]	POUT1[W]	POUT2[W]	POUT [W]	Eff [%]
24.91	9.98	**16.22**	**11.6**	**5.03**	**9.996**	248.6	**188.2**	**50.3**	238.4	**0.959**
24.24	9.787	**16.2**	**11.6**	**5.04**	**8.025**	237.2	**187.9**	**40.4**	228.4	**0.963**
24.29	9.308	**16.21**	**11.6**	**5.04**	**6.022**	226.1	**188.0**	**30.4**	218.4	**0.966**
24.34	8.849	**16.21**	**11.6**	**5.04**	**4.034**	215.4	**188.0**	**20.3**	208.4	**0.967**
24.38	8.399	**16.21**	**11.6**	**5.04**	**2.031**	204.8	**188.0**	**10.2**	198.3	**0.968**
24.29	8.02	**16.21**	**11.6**	**5.04**	**0**	194.8	**188.0**	**0.0**	188.0	**0.965**

Table2

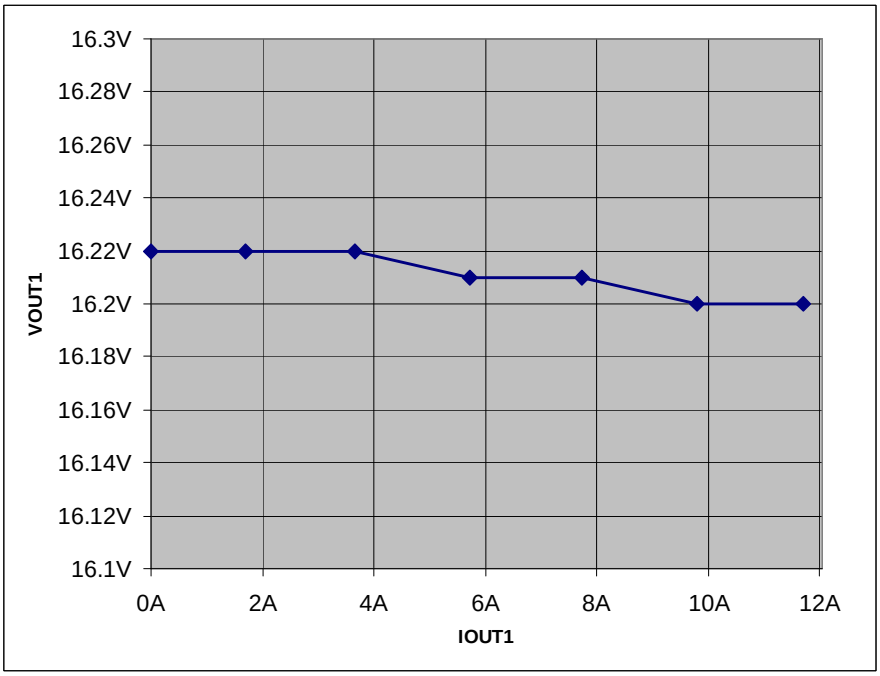
With no load at both outputs, values in the following table are obtained.

VIN[V]	IIN[A]	VOUT1[V]	IOUT1[A]	VOUT2[A]	IOUT2[A]	PIN[W]
25.18	**0.0967**	**16.24**	**0**	**5.05**	**0**	**2.4**

Table3

4 Load Regulation.

The load regulation of the output is shown in the **Figure 6** below. The input voltages were adjusted to 24V. IOUT1 was varied.



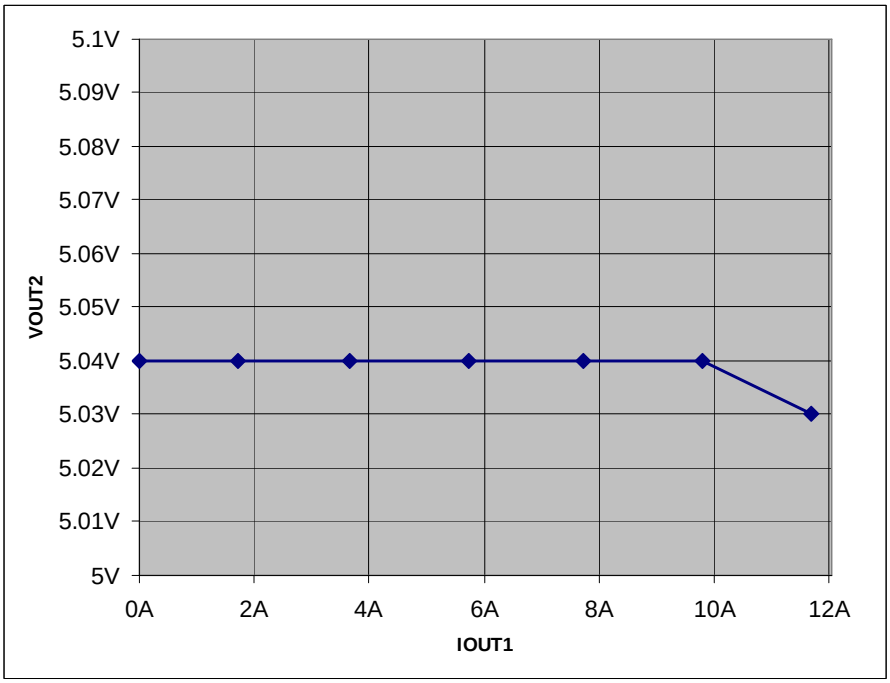


Figure 6

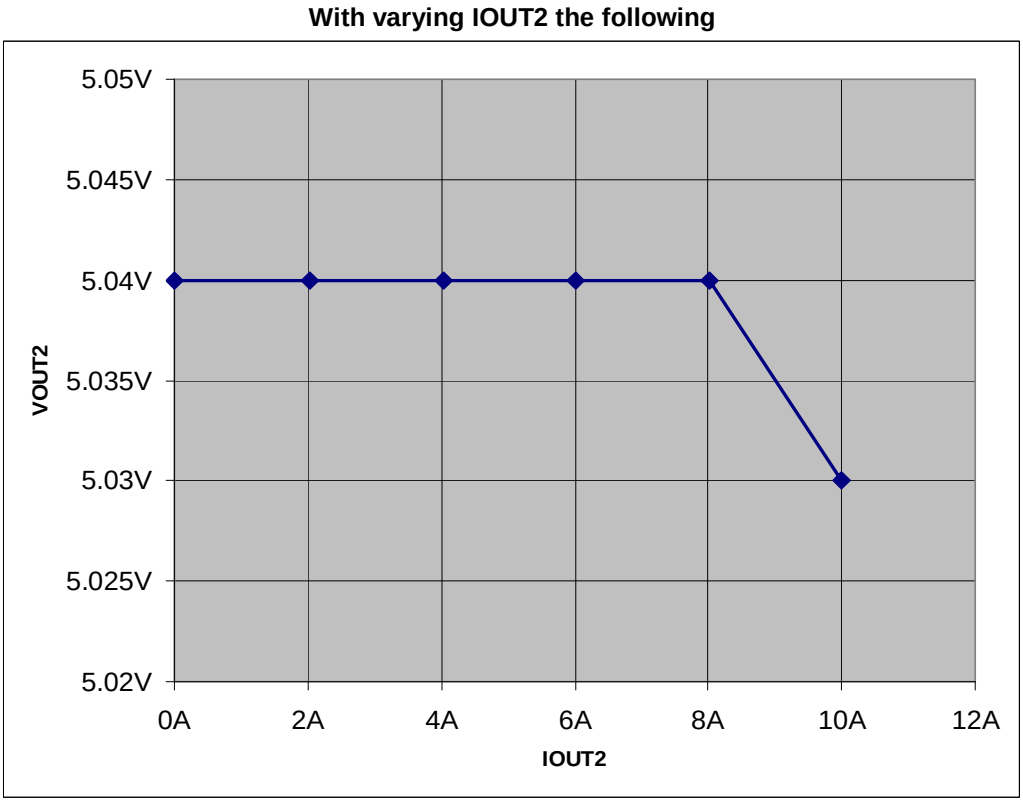
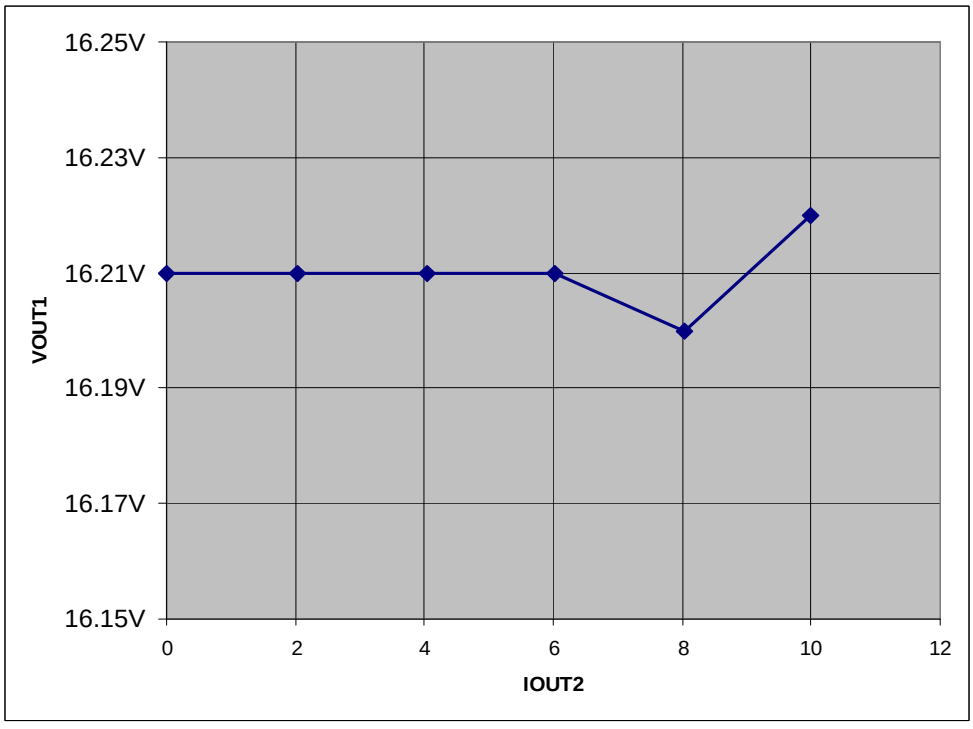


Figure 7 was obtained.



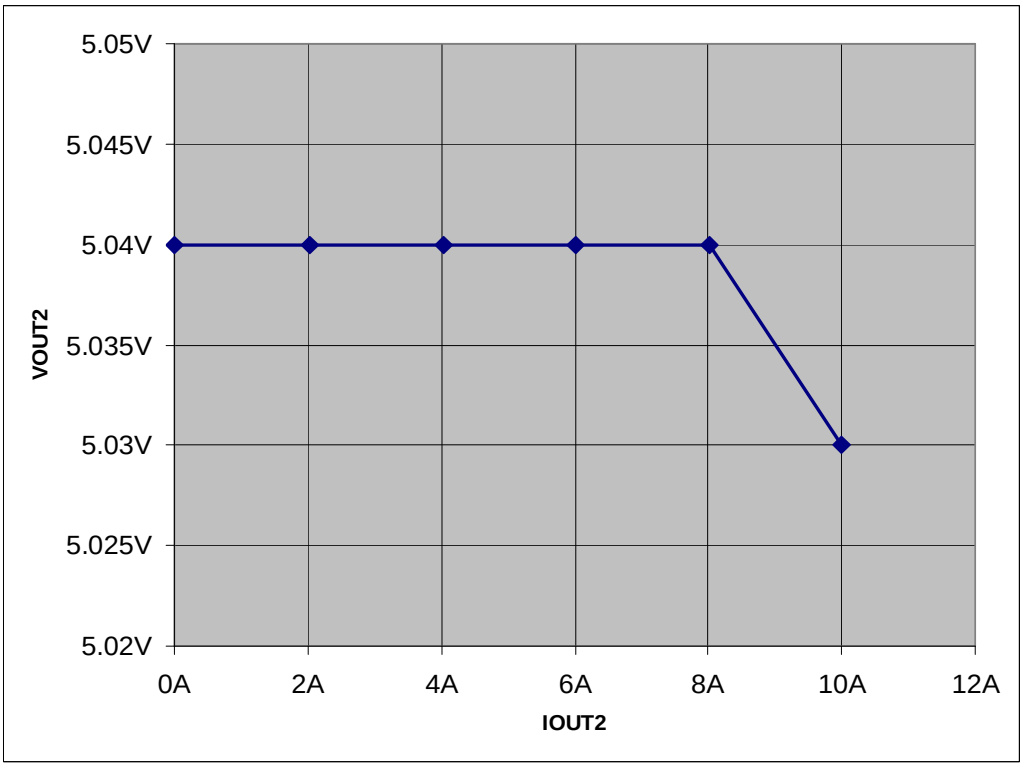

5.05V
5.045V
5.04V
5.035V
5.03V
5.025V
5.02V
VOUT2
0A
2A
4A
6A
8A
10A
12A
IOUT2

Figure 7

5 Ripple Voltage

The output ripple voltage at VOUT1=16V, with Iout1=12A (IOUT2=10A), is shown in Figure 8.

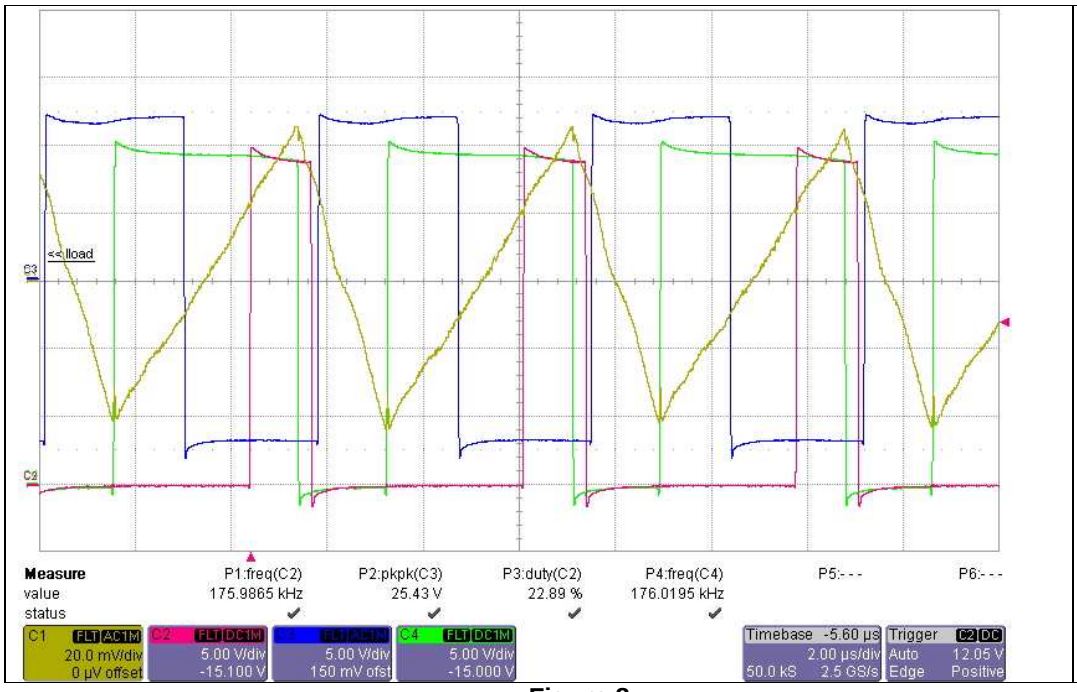


Figure 8

C1: Ouput Ripple 16V ouput, C2: Switch-node 5V ouput, C3: Switch-node 12V ouput (Slave Board), C4: Switch-node 16V ouput

The output ripple voltage at VOUT2=5V, with IOUT2=10A (IOUT2=12A), is shown in Figure 9.

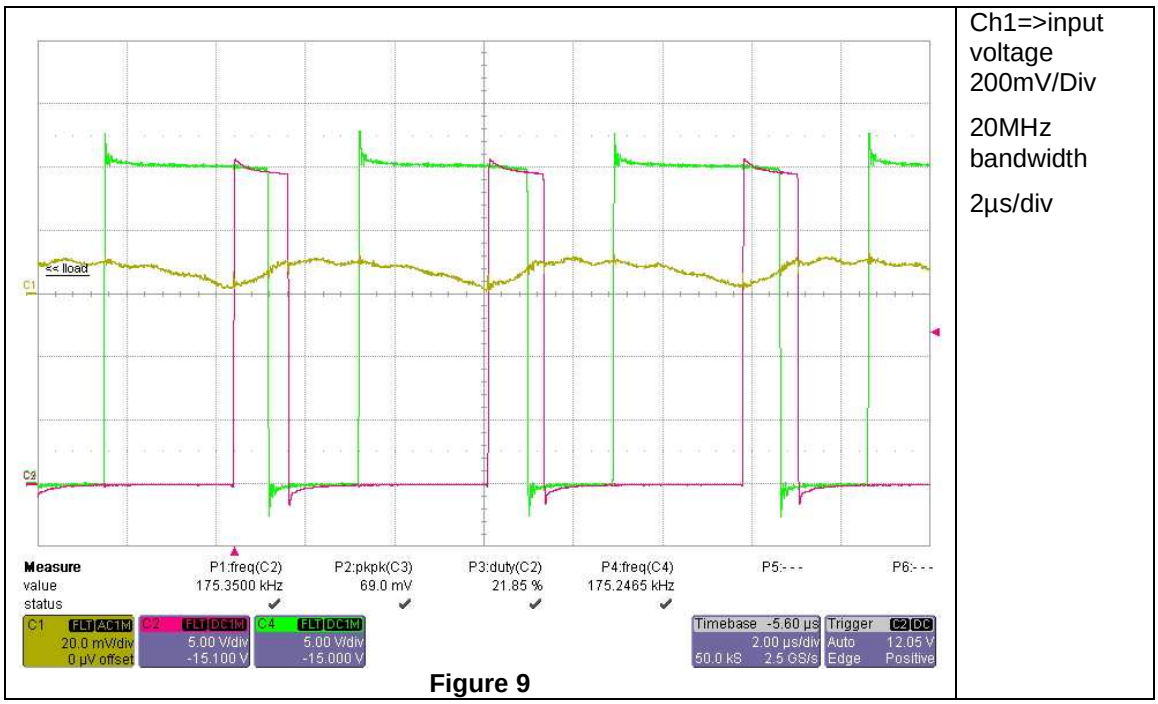


Figure 9

C1: Ouput Ripple 5V ouput C2: Switch-node 5V ouput, C4: Switch-node 16V ouput

6 Control Loop Frequency Response

Figure 10 shows the loop response of the output 16V@12A at full load on both outputs (16V@12A, 12V@4A)

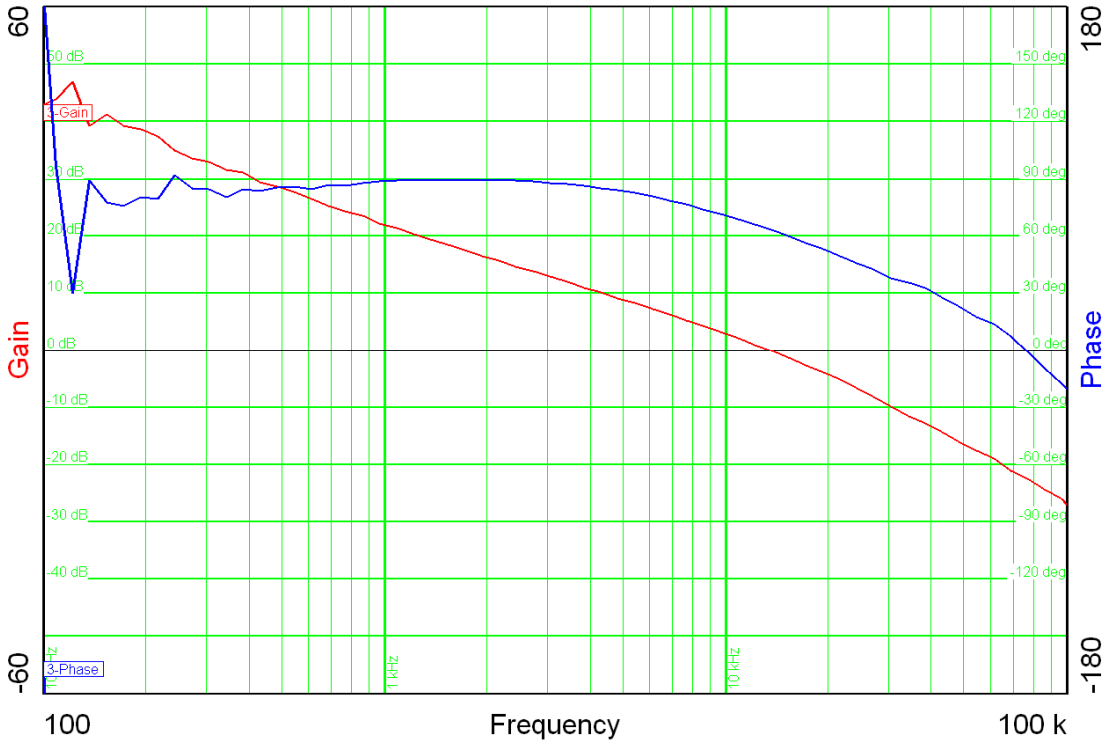


Figure 10

Table 44 summarizes the results from Figure 10

Bandwidth (kHz)	14
Phase margin	63°
slope (20dB/decade)	-1.517
gain margin (dB)	-22
slope (20dB/decade)	-1.36
freq (kHz)	77

Table 4

Figure 101 shows the loop response of the output 5V@10A at full load on both outputs (16V@12A, 12V@4A)

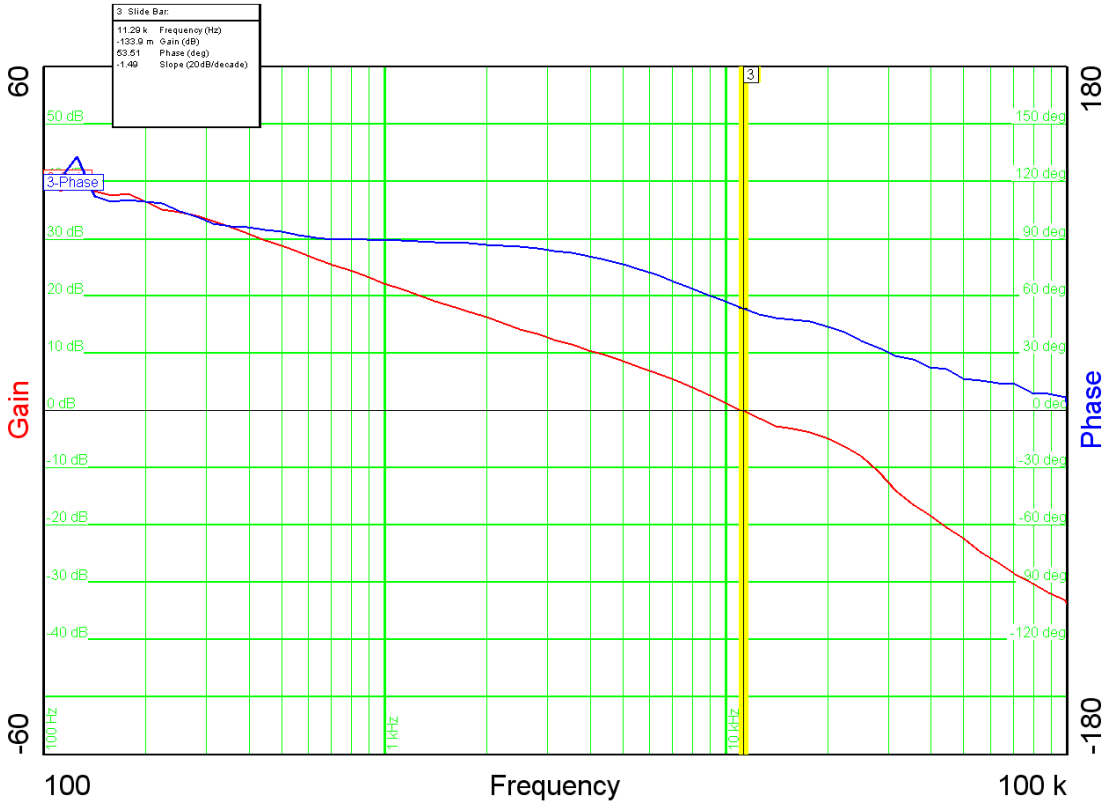


Figure 11

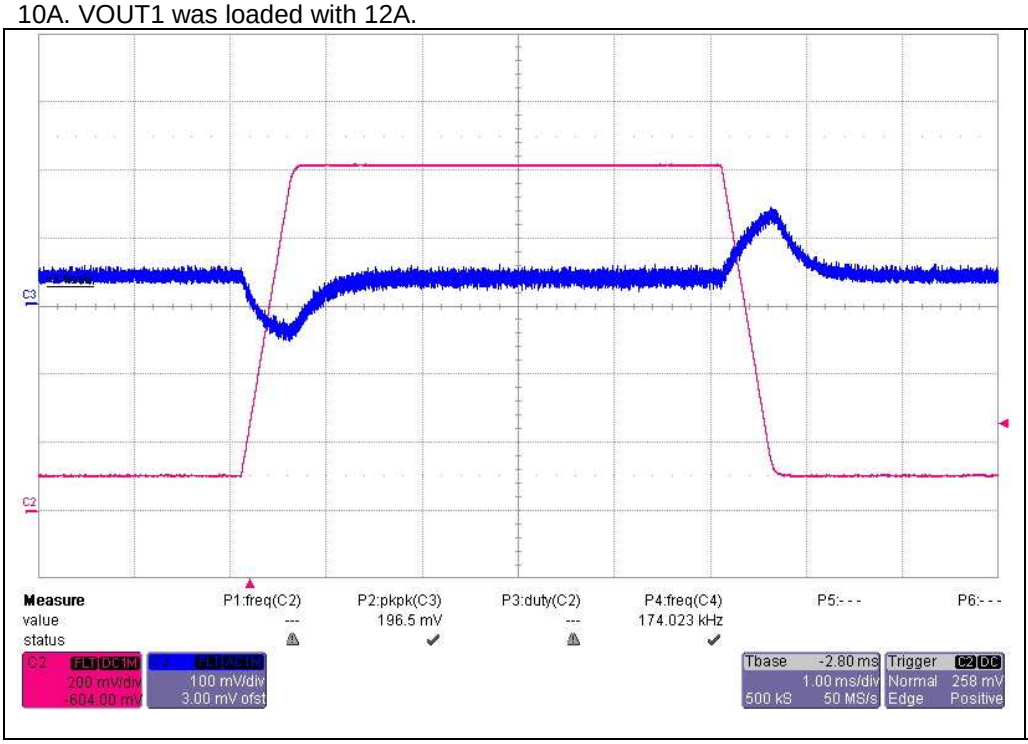
Table 45 summarizes the results from Figure 101

Bandwidth (kHz)	11
Phase margin	56°
slope (20dB/decade)	-1.17
gain margin (dB)	-33
slope (20dB/decade)	-1.2
freq (kHz)	100

Table 5

7 Load Transients

The Figure 12 shows the response to load transients. The load at OUT2 is switching from 1A to 10A. VOUT1 was loaded with 12A.



Ch4 => output voltage2 100mV/div

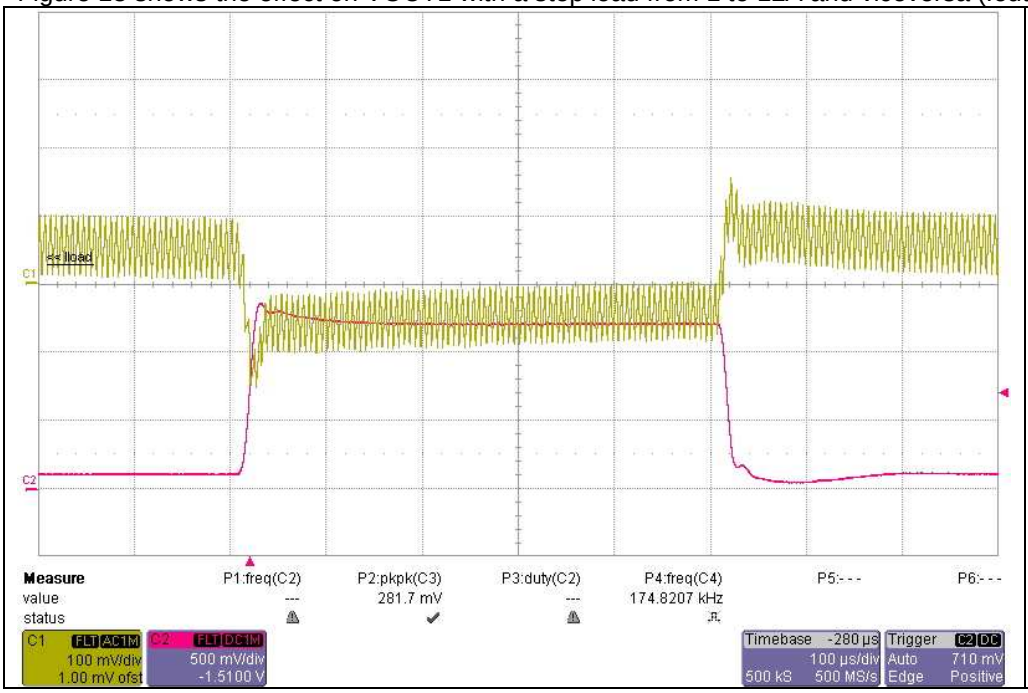
Ch3 => output current2 2A/div

20Mhz bandwidth setting

2ms/div

Figure 12

Figure 13 shows the effect on VOUT1 with a step load from 1 to 12A and viceversa (Iout2=10A).



Ch4 => output voltage1 100mV/div

Ch3 => output current2 2A/div

20Mhz bandwidth setting

2ms/div

Figure 13

8 Switch Node Waveforms, stand-alone Master and Master-Slave Operation

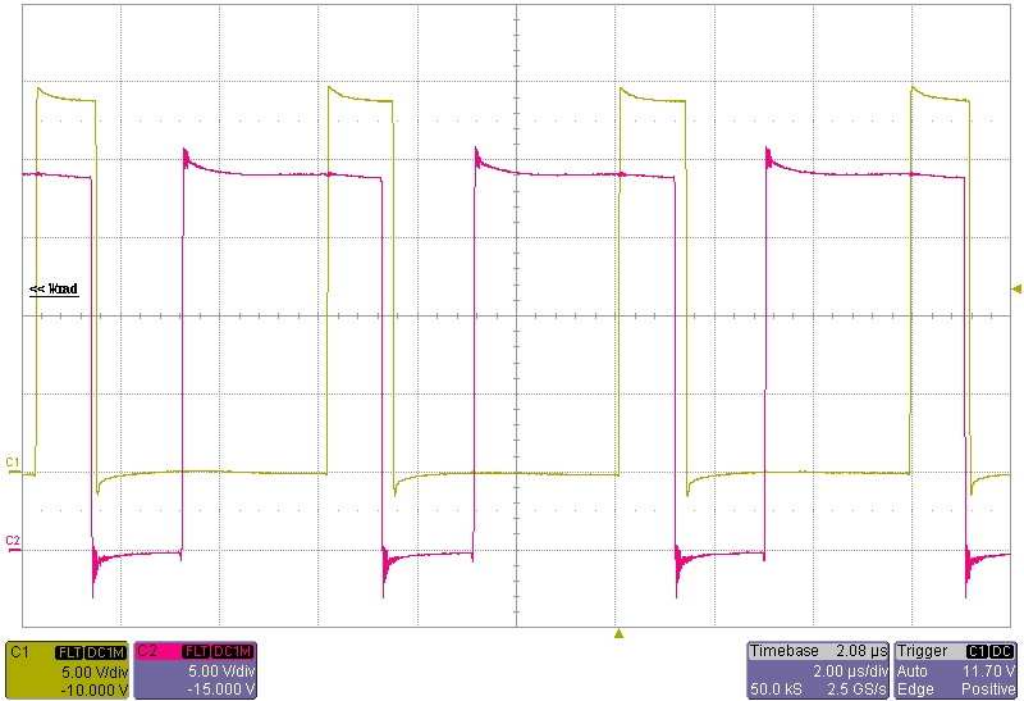


Figure 14 - C1: Switch-node 5V out, C2: Switch-node 16V out, full load on both outputs, stand-alone Master Operation

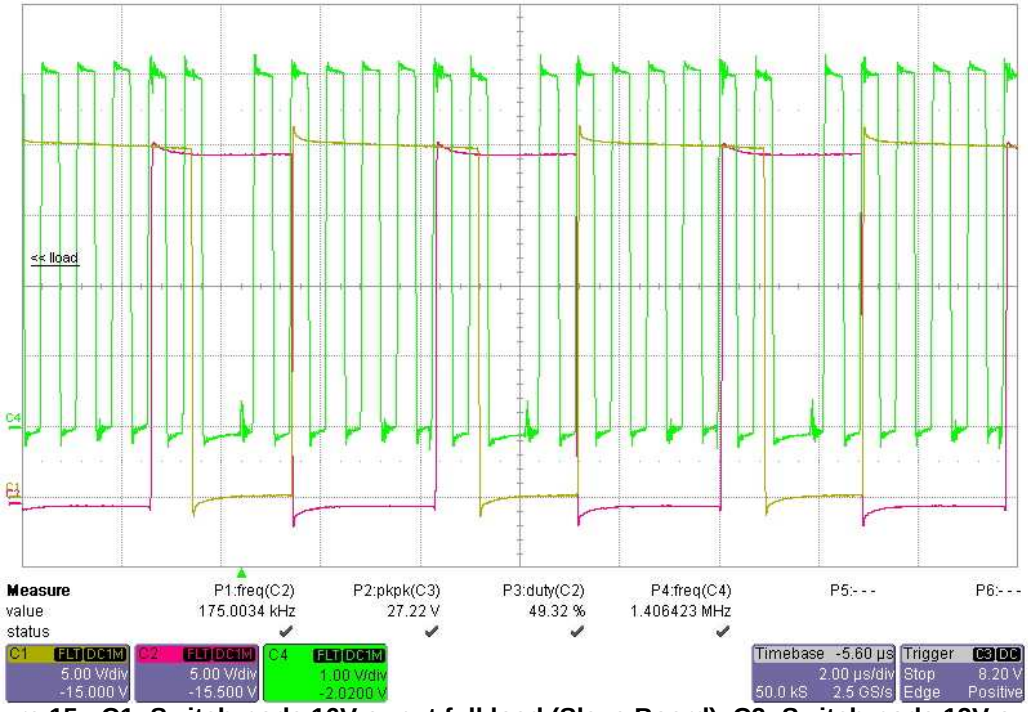


Figure 15 - C1: Switch-node 16V ouput full load (Slave Board), C2: Switch-node 12V ouput full load(Slave Board), C4: Synchronizing signal at J7 from the Master Board

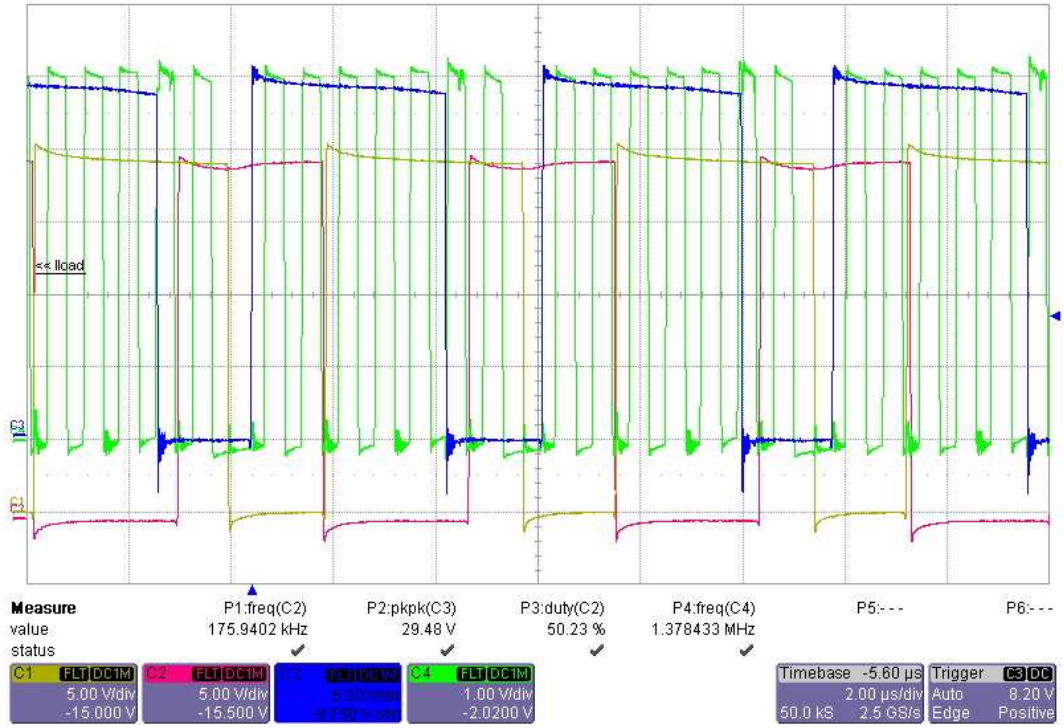


Figure 16 - C1: Switch-node 16V out full load (Slave), C2: Switch-node 12V out full load (Slave), C3: Switch-node 16V out (Master) C4: Synch. signal at J7 from the Master Board

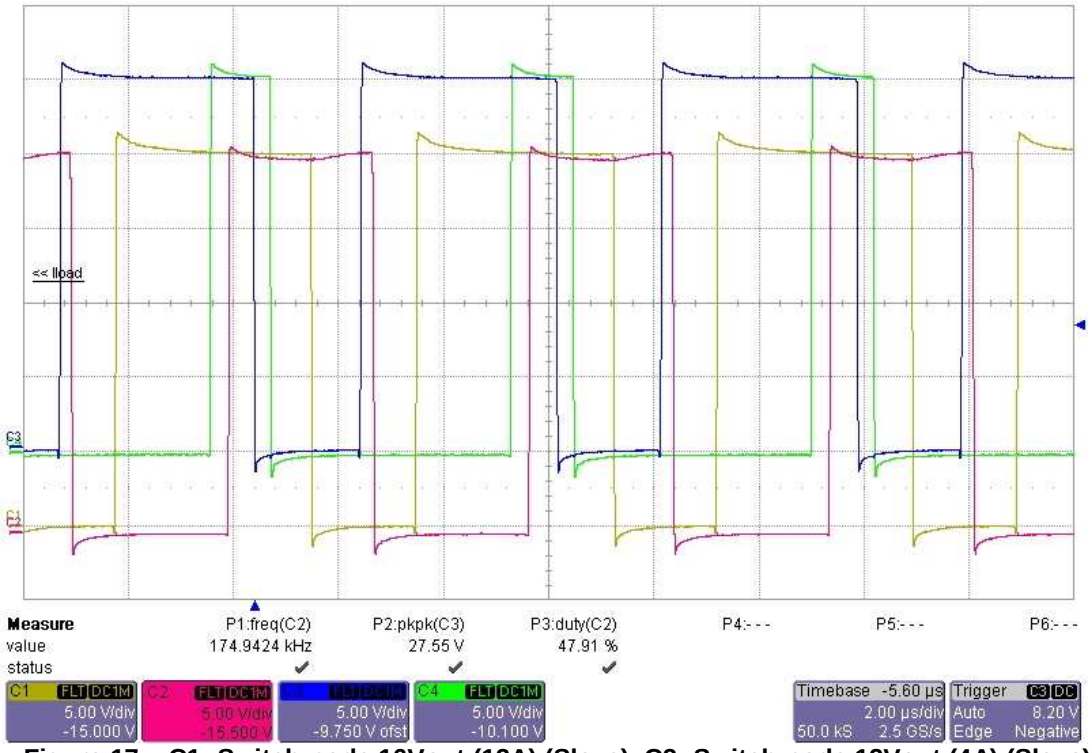


Figure 17 – C1: Switch-node 16Vout (12A) (Slave), C2: Switch-node 12Vout (4A) (Slave), C3: Switch-node 16Vout (12A) (Master), C4: Switch-node 5Vout (10A) (Master)

9 Short Circuit Operation

The operation has been tested putting through short condition on the output, removing, and pretending the system to reestablish the output power after soft-starting (Vtrk).
The transitory in turning off has been analyzed in detail according to the following time plots.
If the short circuit is removed, the IC restarts after 7 soft start-cycles (hiccup mode).

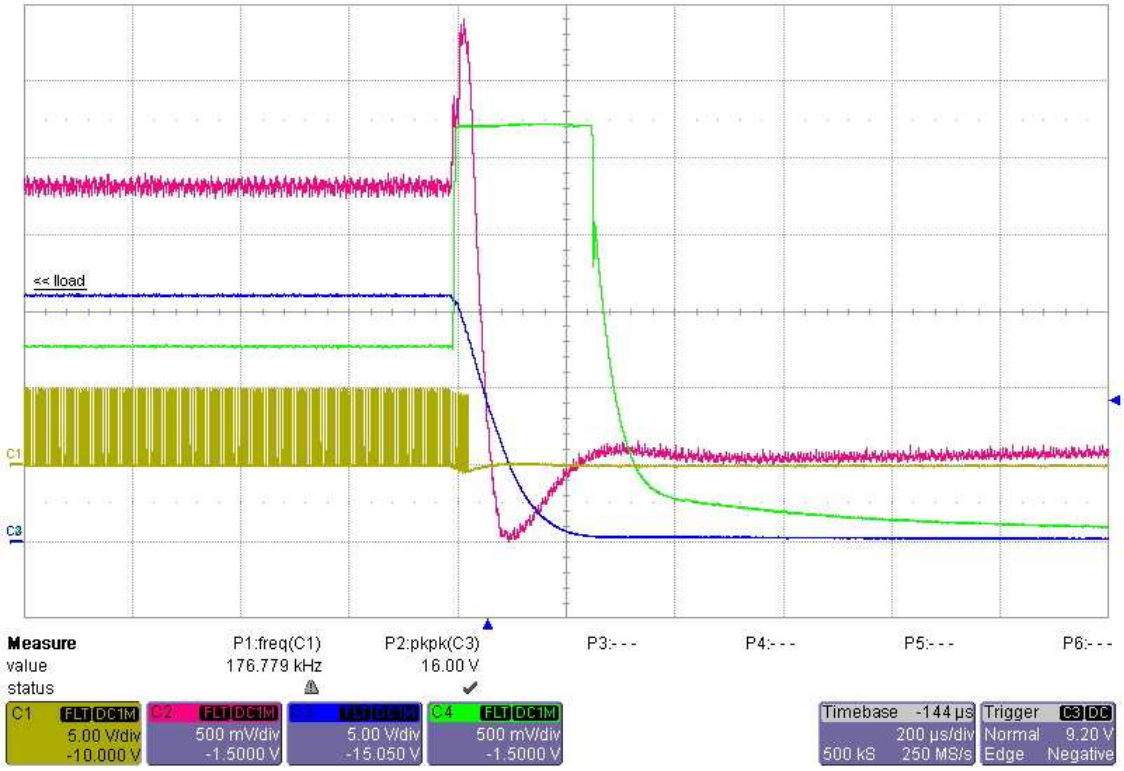


Figure 18: (Short Circuit on Vout=16V, Iout=12A) C4=Iout, C3=Vout, C2=TRK1 (TP3), C1=VLDRV1(drive)

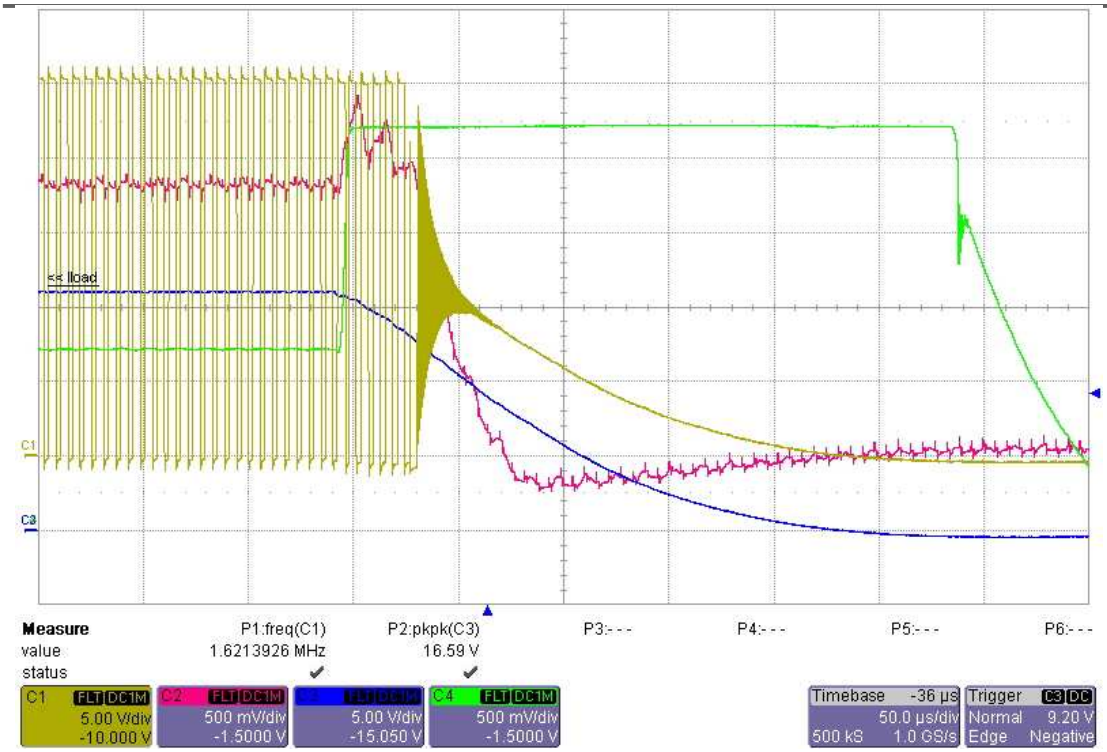


Figure 19: (Short Circuit on Vout=16V, Iout=12A) C4=Iout, C3=Vout, C2=TRK1 (TP3), C1=Vswitchnode (TP4)

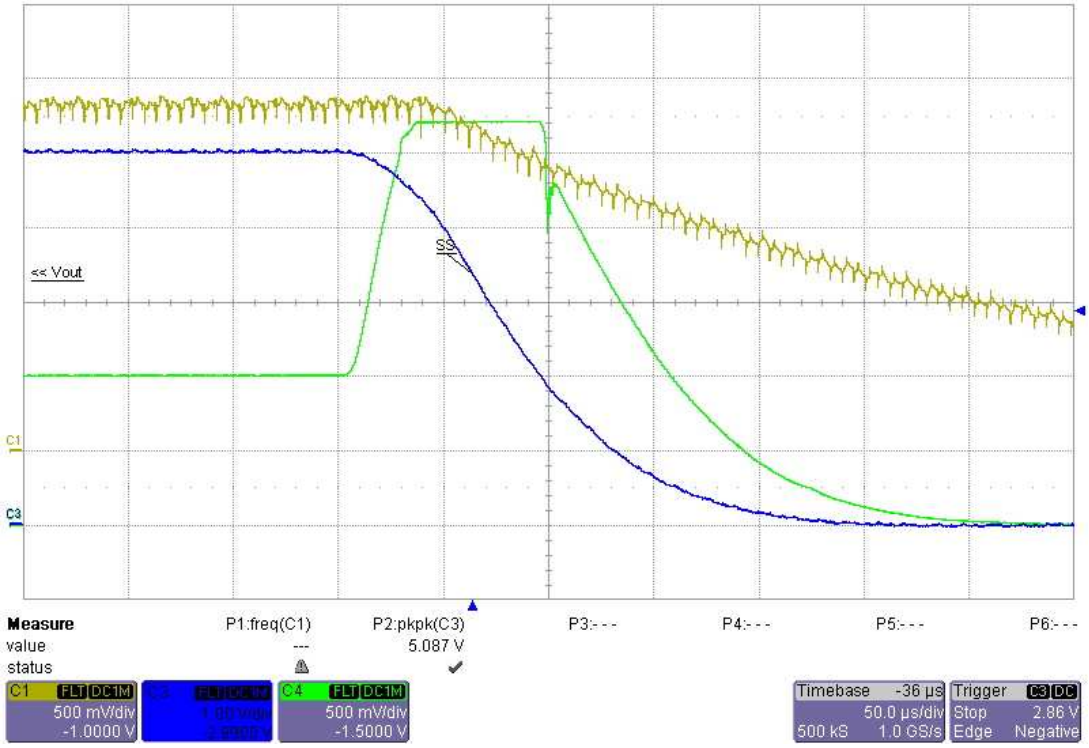


Figure 20: (Short Circuit on Vout=5V, Iout=10A) C4=Iout, C3=Vout, C1= Vtrack2 (TP17)

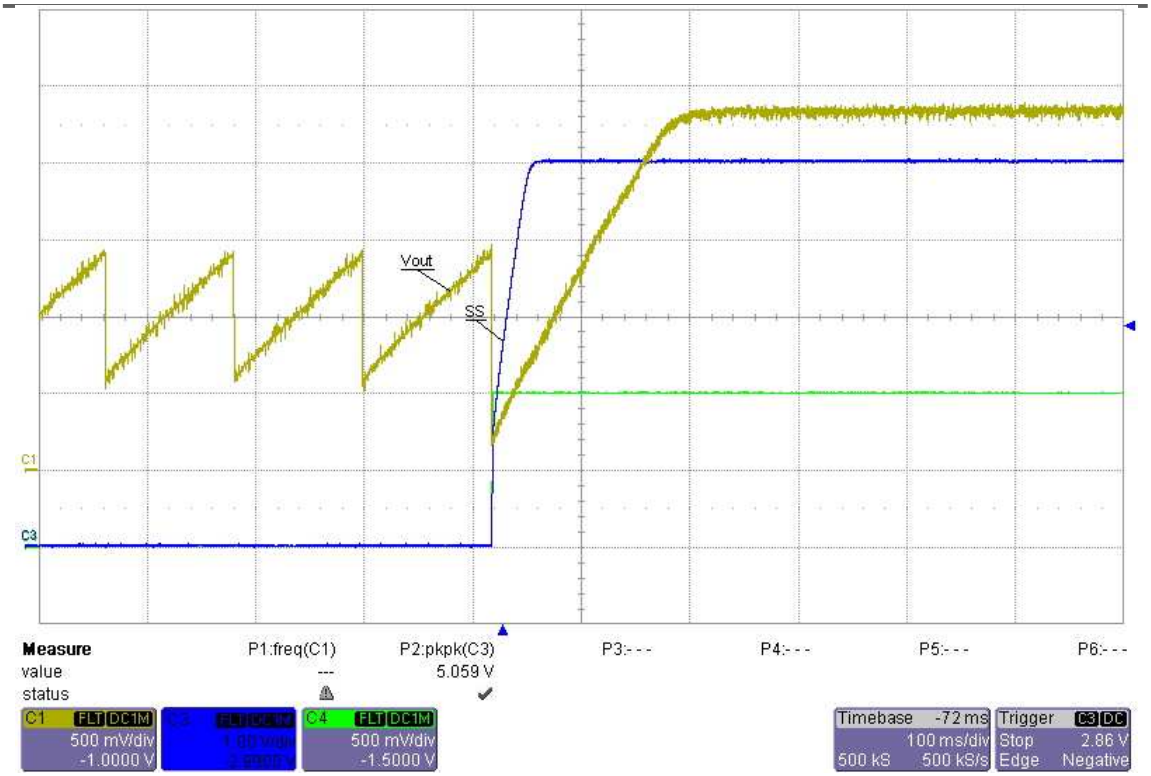


Figure 21: (Short Circuit removed on Vout=16V, Iout=12A) C4=Iout, C3=Vout, C1=Vtrack2 (TP17)

Values of current limitation for the two outputs are:

- **Vout=16V, Iout_lim=14.8A**
- **Vout=5V, Iout_lim=11.7A**

10 Thermal Pictures

Figure 106 shows the thermal picture of the board at full load on both outputs (16V@12A, 5V@10A) at ambient temperature Tamb=25°C.

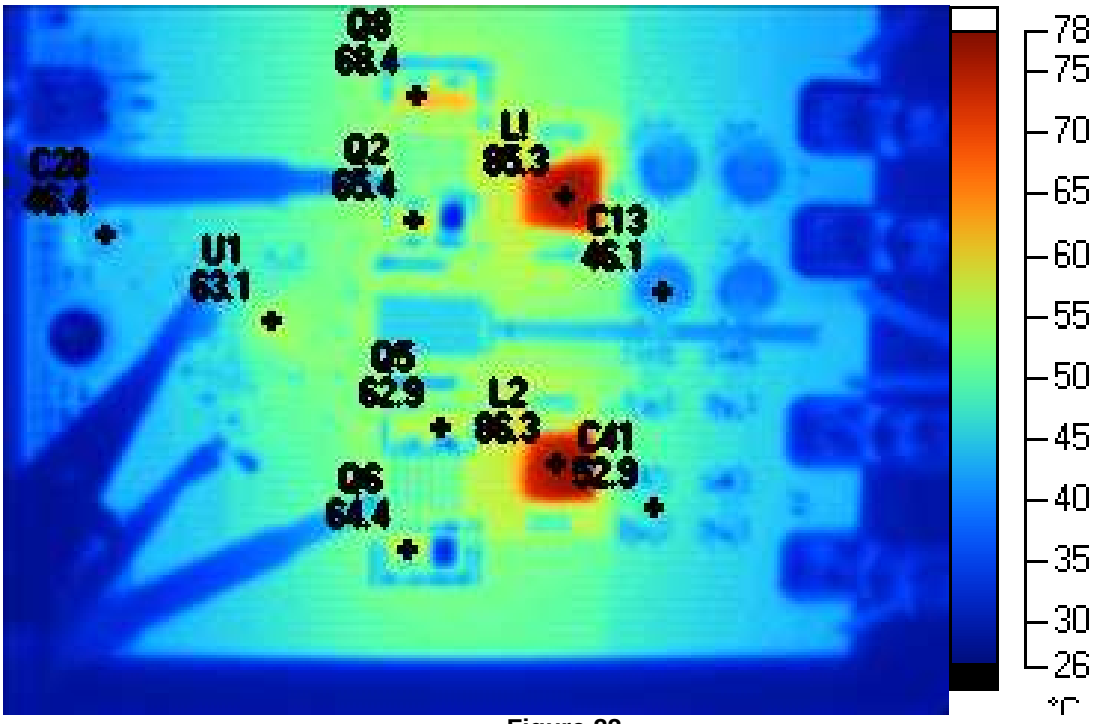


Figure 22

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