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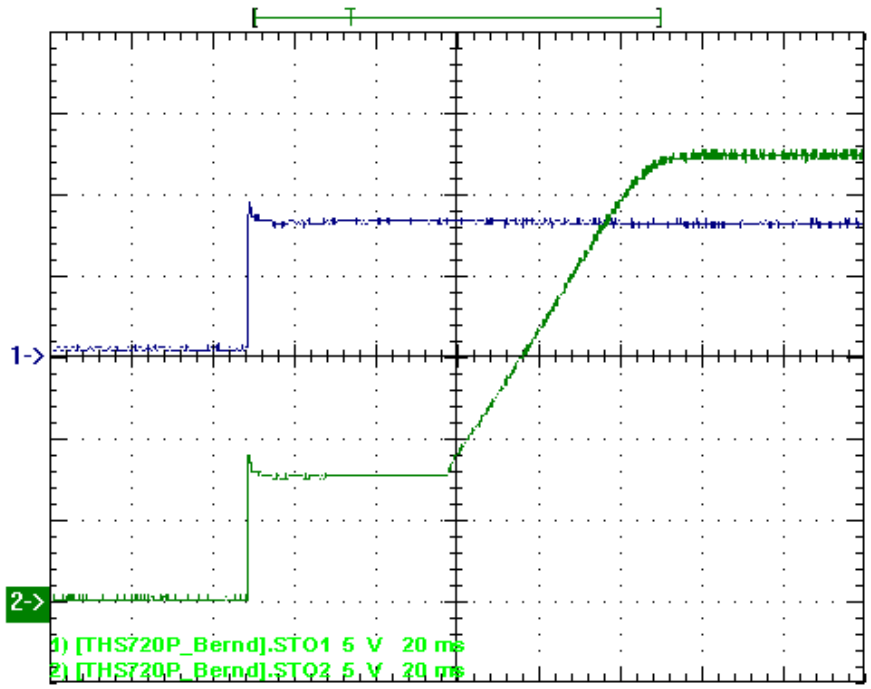
1. Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 8V, with 1A load on the output.

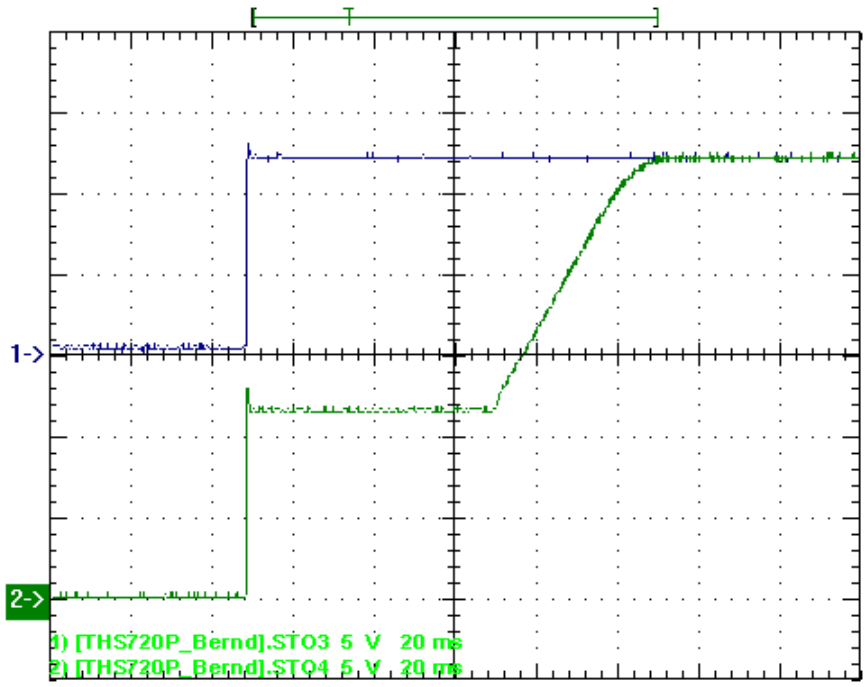


CH1=> input voltage 5V/div

CH2=> output voltage 5V/div 20ms/div

Figure 1 Startup 8Vin

The startup waveform is shown in the Figure 2. The input voltage was set at 12V, with 1A load on the output.



CH1=> input voltage 5V/div

CH2=> output voltage 5V/div 20ms/div

Figure 2 Startup 12Vin

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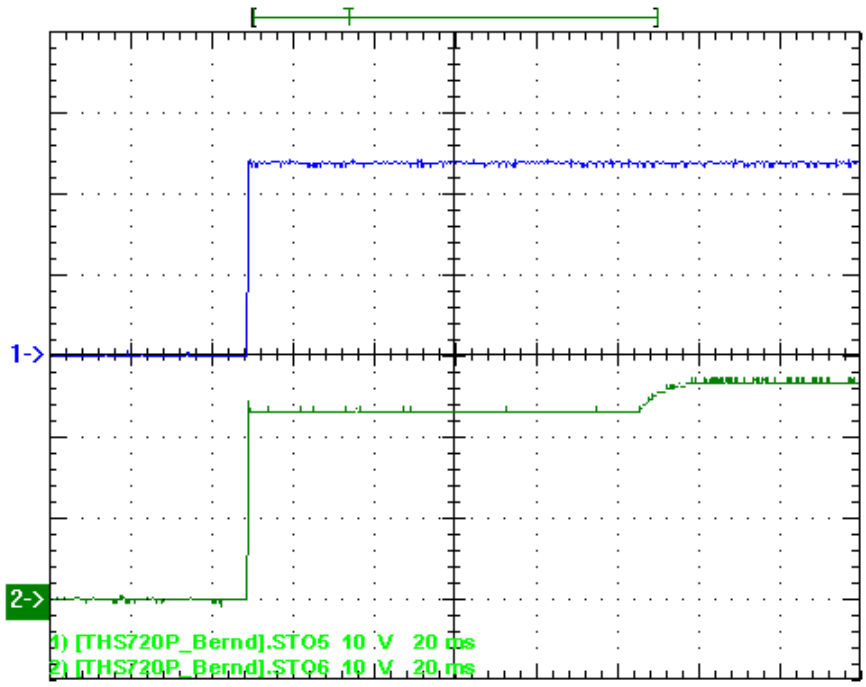
The startup waveform is shown in the Figure 3. The input voltage was set at 24V, with 1A load on the output.



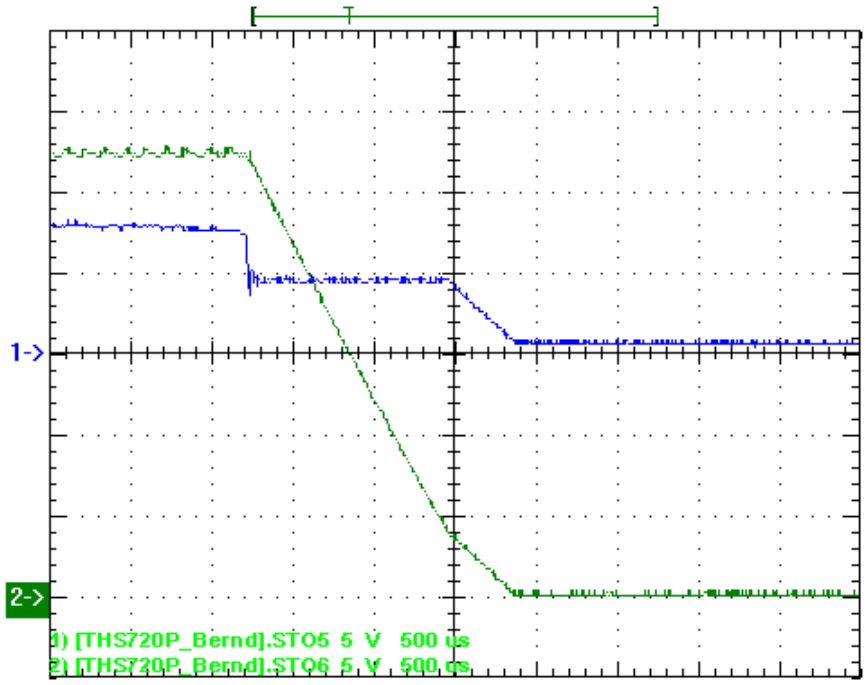
CH1=> input voltage 10V/div

CH2=> output voltage 10V/div 20ms/div

Figure 3 Startup 24Vin

2. Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set at 8V, with 1A load on the output.



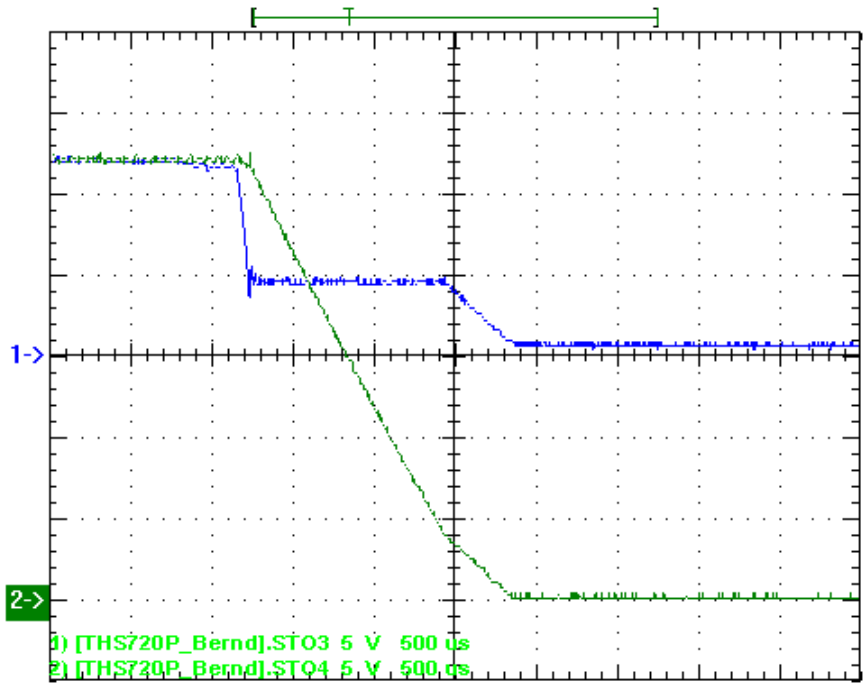
Ch1=> input voltage 5V/div

CH2=> output voltage 5V/div

500µs/div

Figure 4 shutdown 8Vin

The shutdown waveform is shown in the Figure 5. The input voltage was set at 12V, with 1A load on the output.



Ch1=> input voltage 5V/div

CH2=> output voltage 5V/div

500µs/div

Figure 5 shutdown 12Vin

The shutdown waveform is shown in the Figure 6. The input voltage was set at 8V, with 1A load on the output.

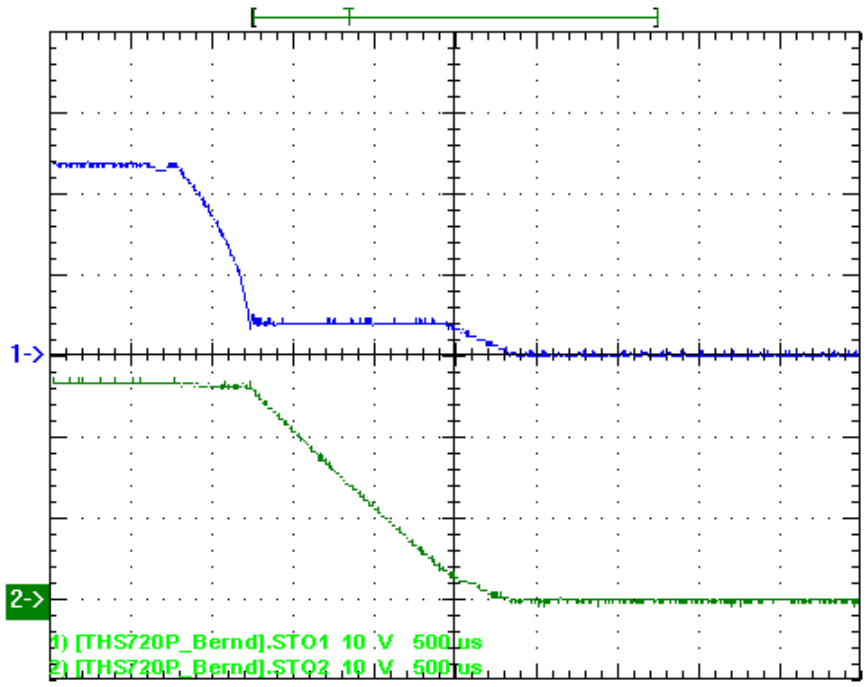


Figure 6 shutdown 24Vin

Ch1=> input voltage 10V/div

CH2=> output voltage 10V/div

500µs/div

3. Efficiency

The efficiency is shown in the Figure 7 below.

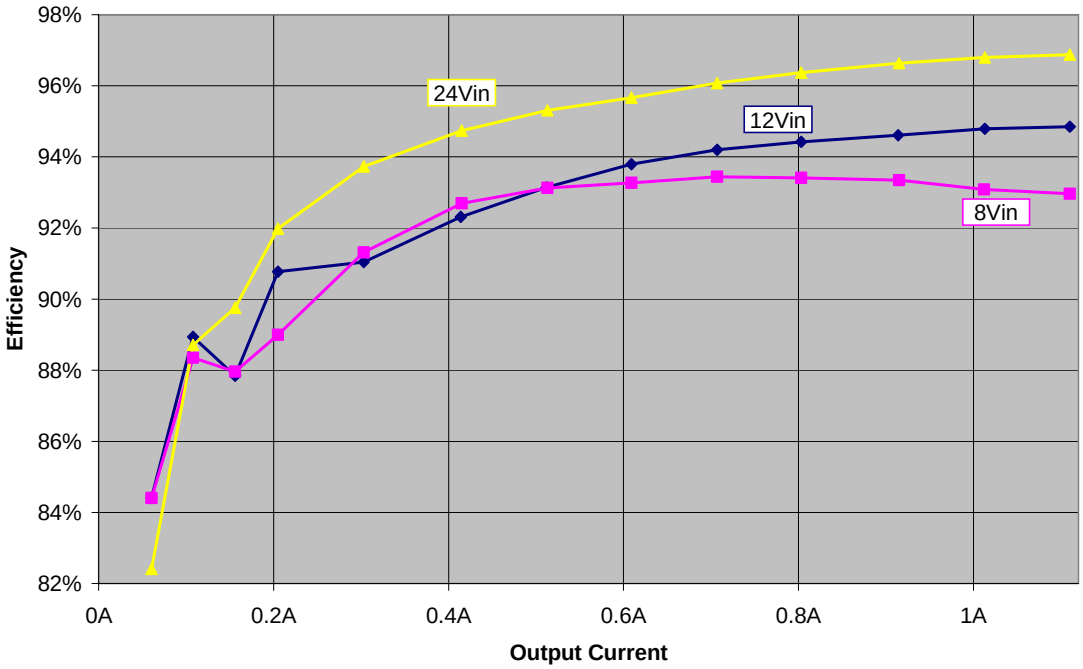


Figure 7

4. Load Regulation

The load regulation of the output is shown in the **Figure 8** below.

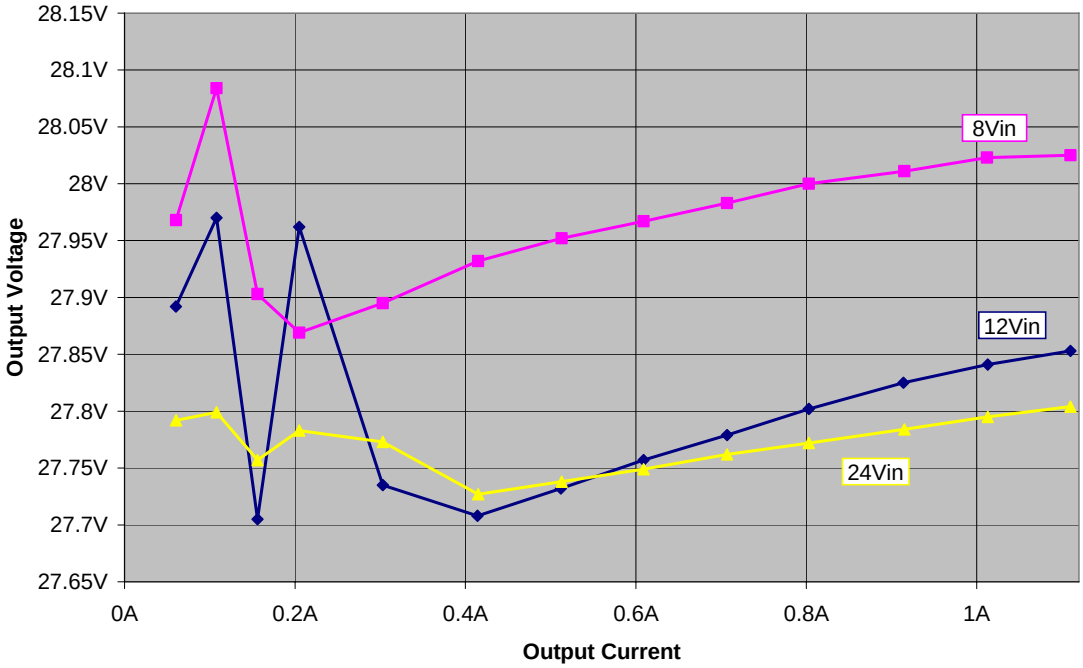


Figure 8

5. Line Regulation

The line regulation with 1A output current is shown in Figure 9.

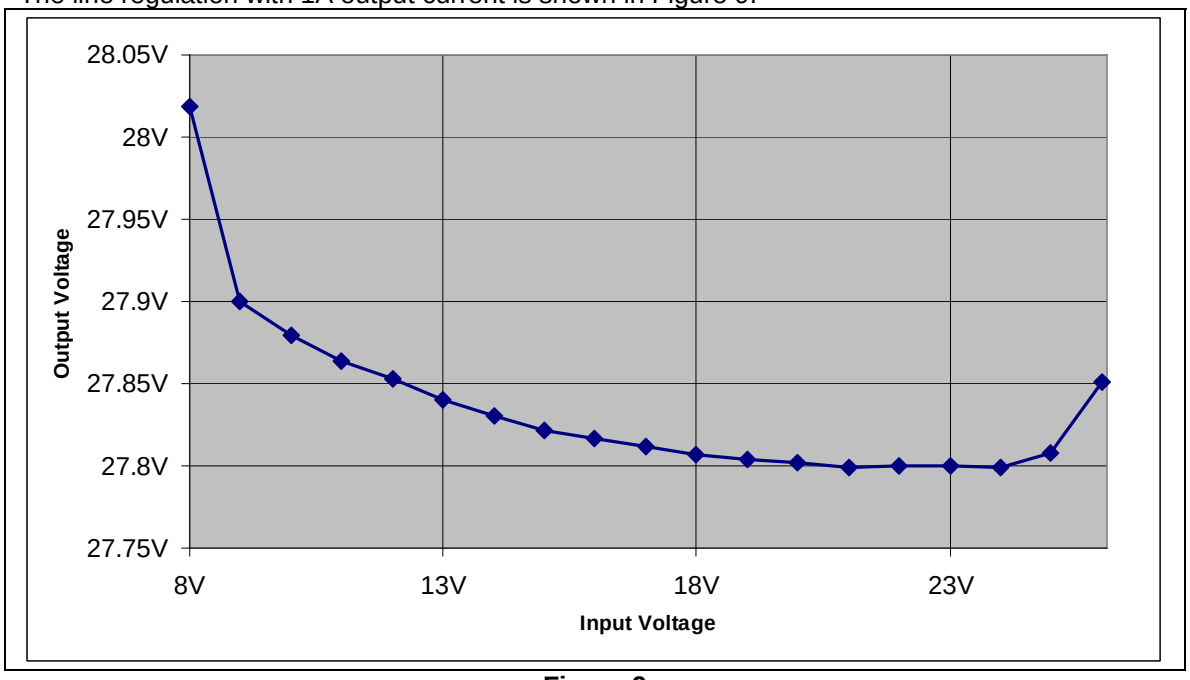


Figure 9

With the same measurement the corresponding efficiencies are shown in Figure 10.

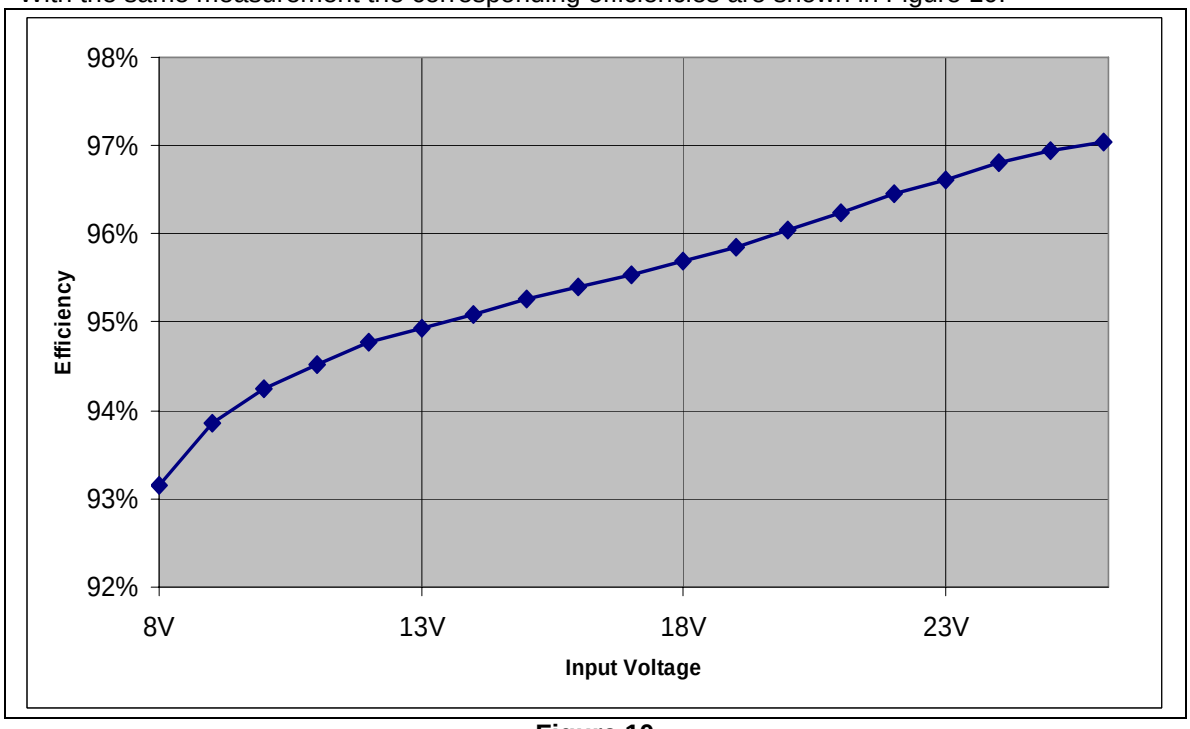
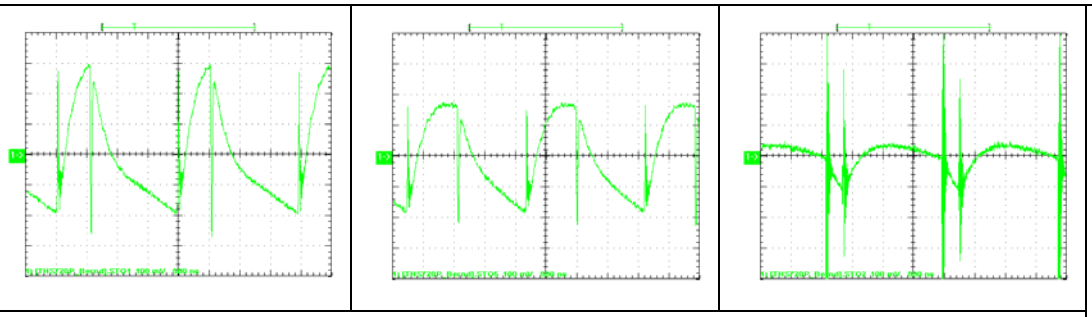


Figure 10

6. Ripple Voltage

The output ripple voltage is shown in Figure 11. The image was taken with a 1A load and 8V/12V/24V at the input.



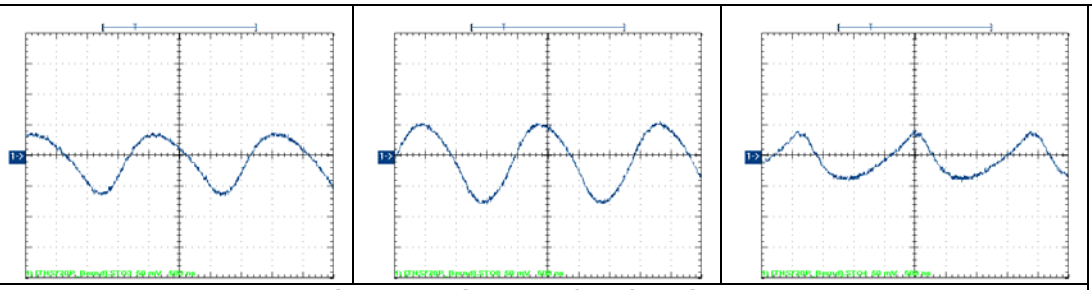
Ch1 => output voltage 100mV/Div

20MHz bandwidth setting

500ns/div

Figure 11 Vout AC 8V/12V/24V input

The input ripple voltage is shown in Figure 12. The image was taken with a 1A load and 8V/12V/24V at the input.



Ch1 => input voltage 50mV/Div

20MHz bandwidth setting

500ns/div

Figure 12 Vin AC 8V/12V/24V input

7. Load Transients

The Figure 13 shows the response to load transients. The load is switching from 0.5A to 1A with 8V at the input. Transient switching frequency was set to 100Hz

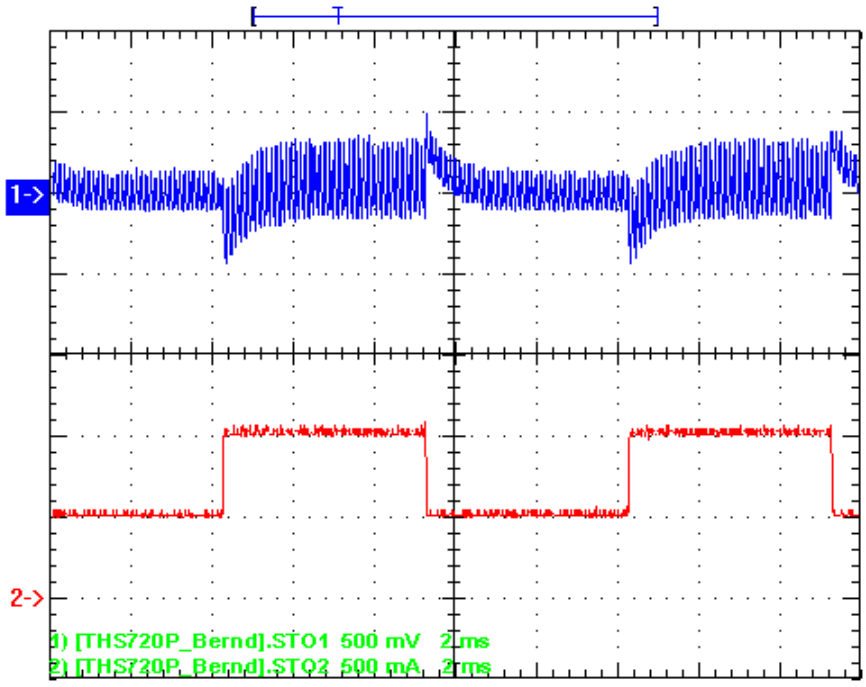


Figure 13

Ch1 => output voltage 500mV/div

Ch2 => load step: 500mA/div

20Mhz bandwidth setting

2ms/div

The same setup with the 24V applied at the input

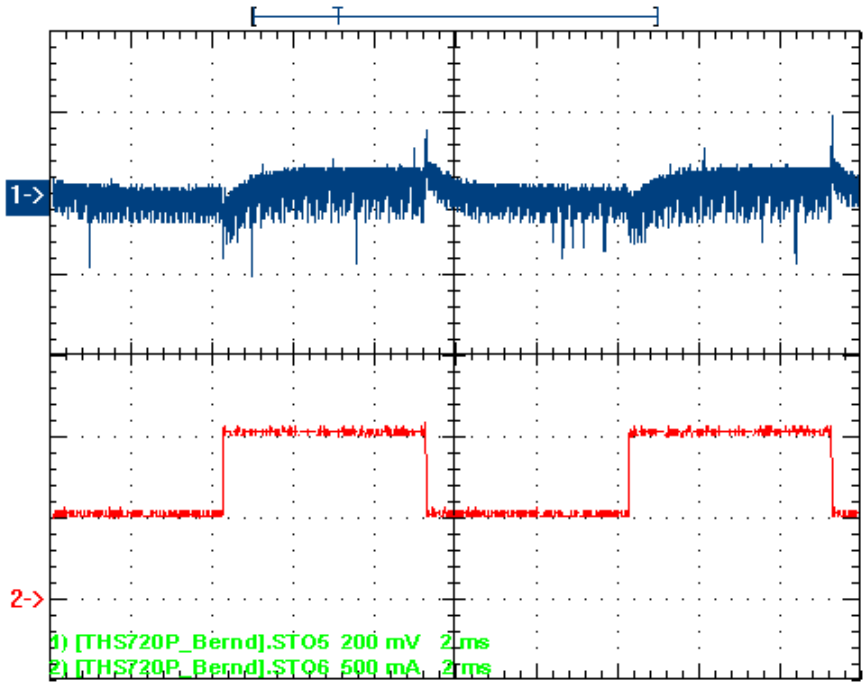


Figure 14

Ch1 => output voltage 200mV/div

Ch2 => load step: 2A/div

20Mhz bandwidth setting (CH1)

2ms/div

8. Switch Node Waveform

With input voltage set to 8V result in the waveform shown in Figure 15 and Figure 16. Output current was set to 1A.

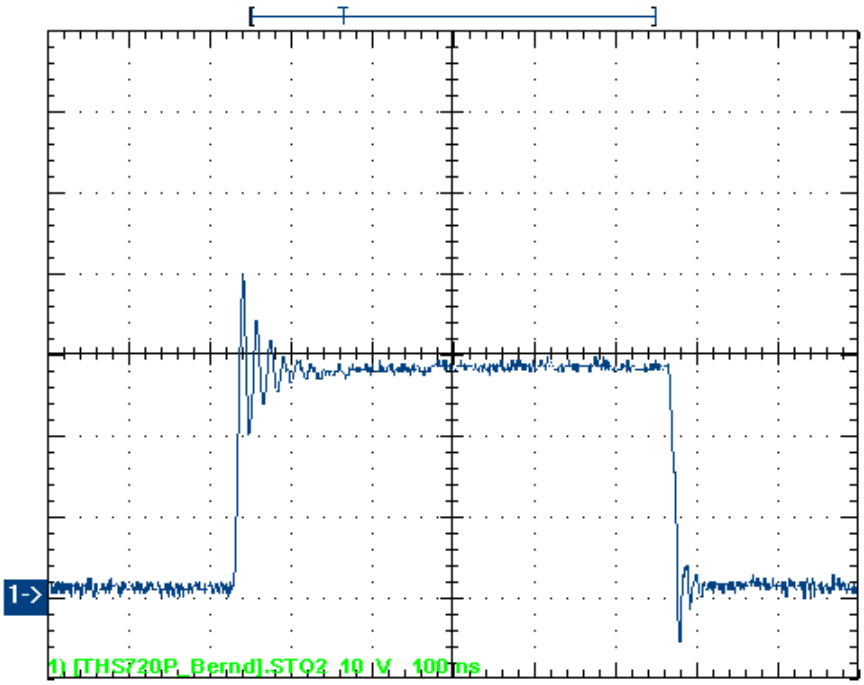
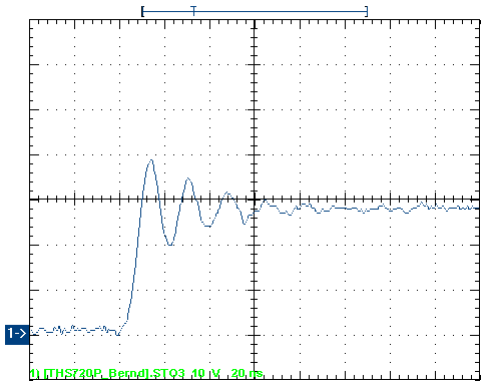


Figure 15

Ch1 => switch node
10V/div

100ns/div

full bandwidth



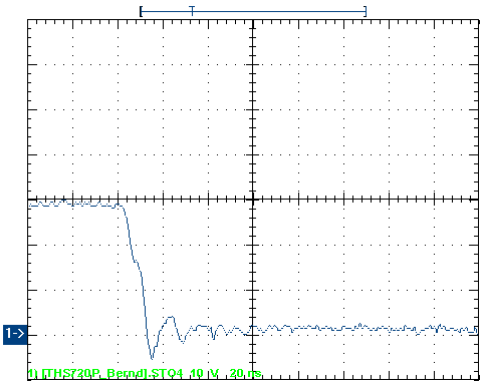


Figure 16

Ch1 => switchnode
10V/div

20ns/div

full bandwidth

With input voltage set to 12V result in the waveform shown in Figure 17 and Figure 18. Output current was set to 1A.

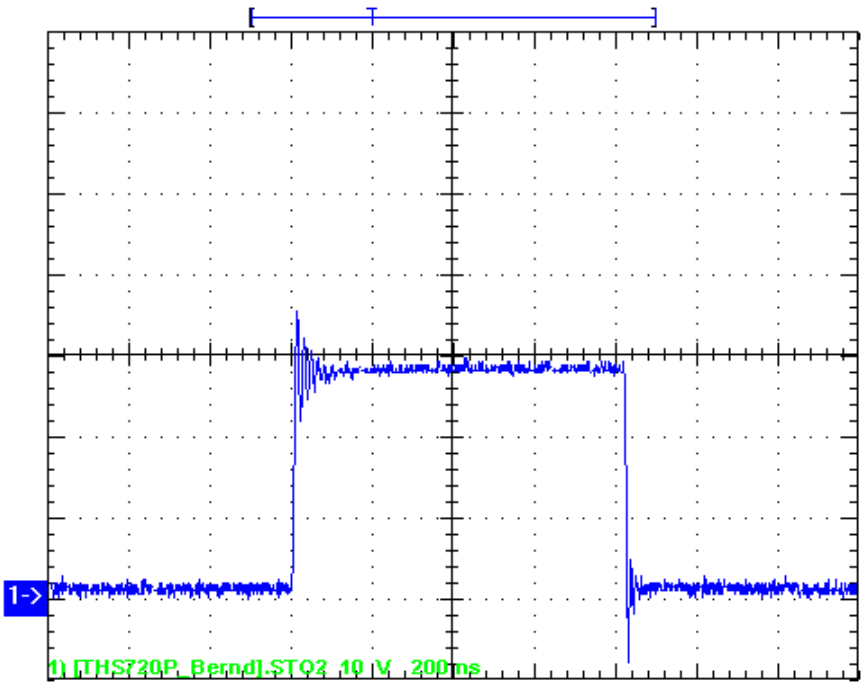
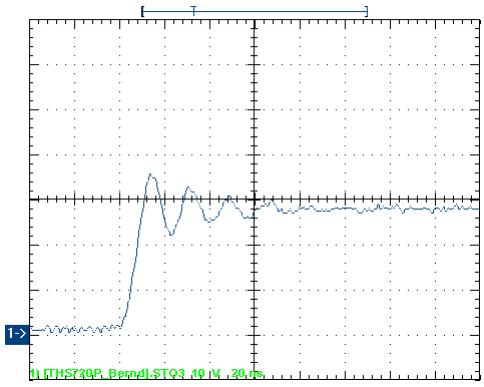


Figure 17

Ch1 => switch node
10V/div

200ns/div

full bandwidth



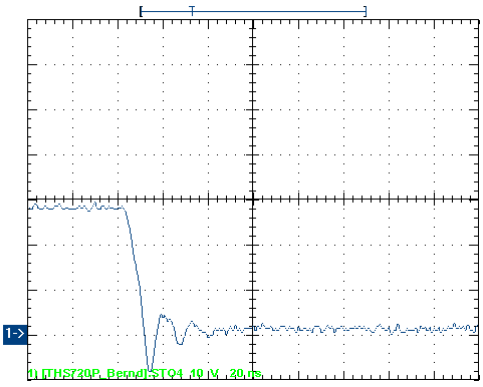


Figure 18

Ch1 => switchnode
10V/div

20ns/div

full bandwidth

With input voltage set to 24V result in the waveform shown in Figure 19 and Figure 20. Output current was set to 1A.

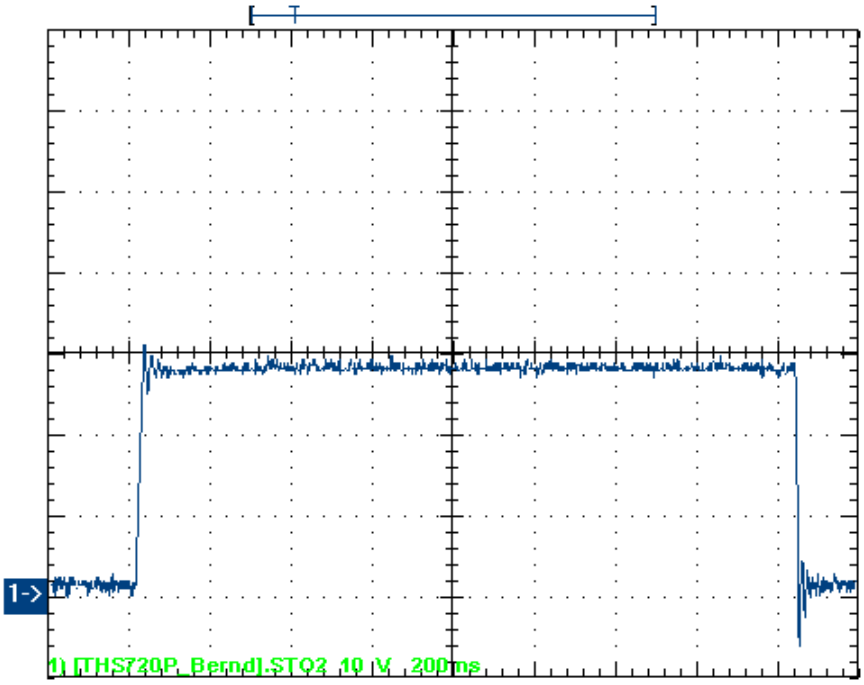


Figure 19

Ch1 => switch node
10V/div

200ns/div

full bandwidth

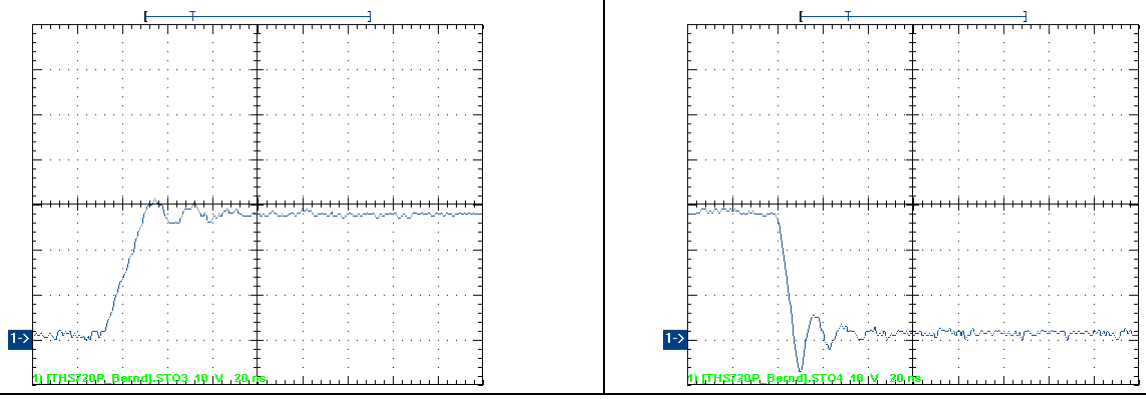


Figure 20

Ch1 => switchnode
10V/div

20ns/div

full bandwidth

9. Control Loop Frequency Response

Figure 21 shows the control loop frequency response and in Table 1 are the corresponding values for gain and phase margin. The output current was set to 1.1A and input voltage to 8V.

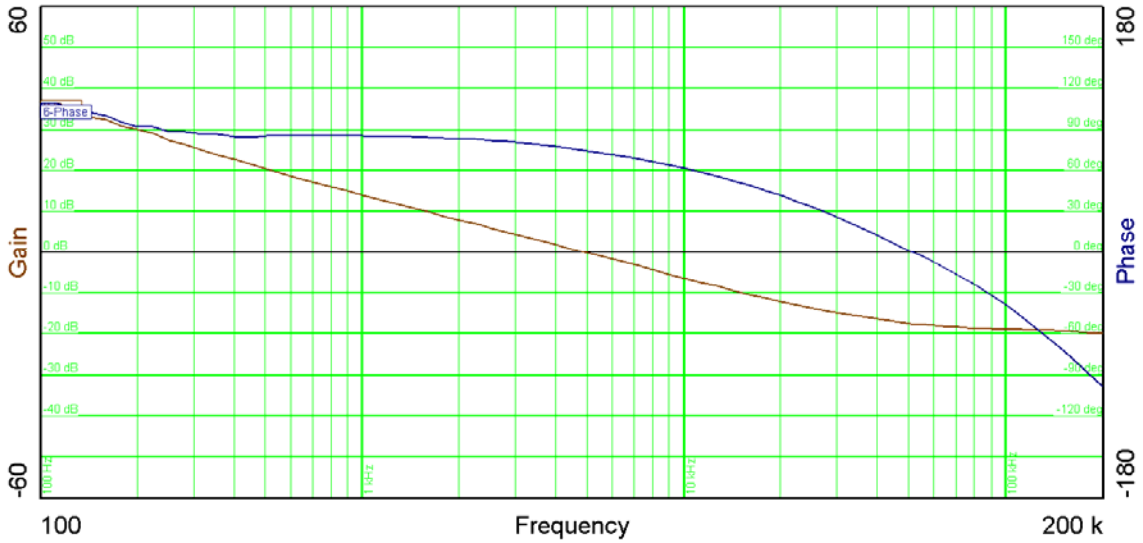


Figure 21

Bandwidth (kHz)	4.95
Phase margin	74.8°
slope (20dB/decade)	-1.04
gain margin (dB)	-17.5
at frequency (kHz)	51
slope (20dB/decade)	-0.393

Table 1

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