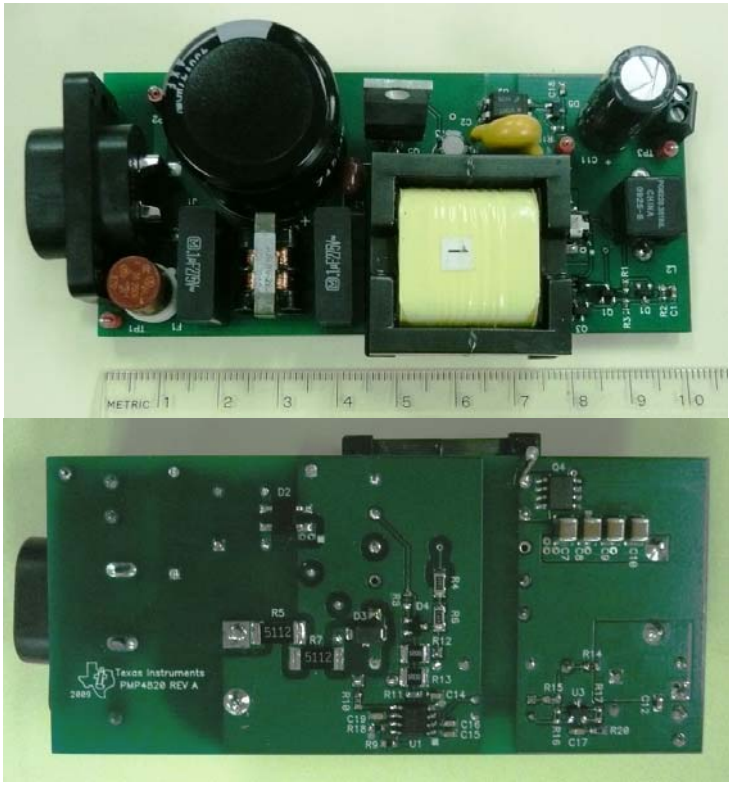
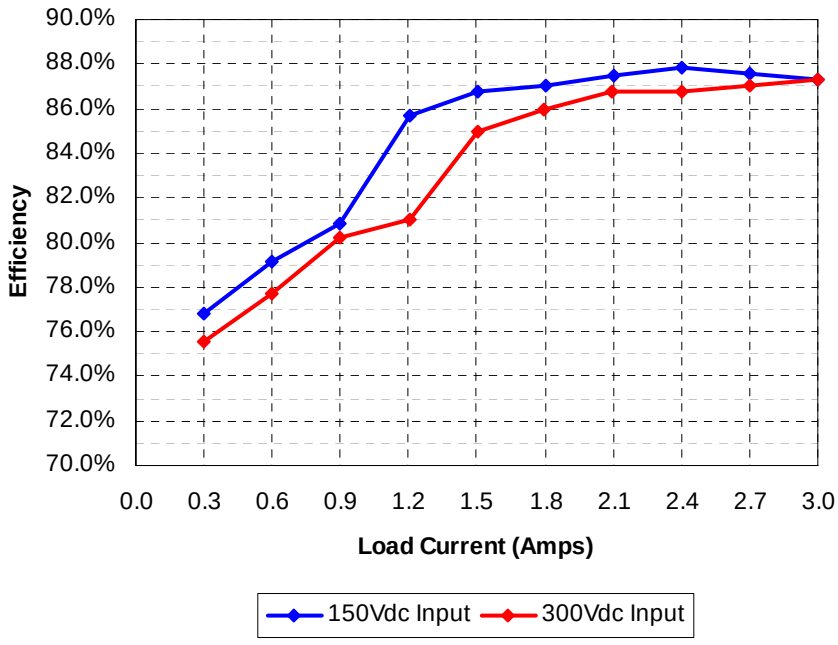
1 Photo

The photographs below show the top and bottom views of the PMP4820 Rev B demo board. The circuit is built on a PMP4820 Rev A PWB.



2 Efficiency

The efficiency data is shown in the tables and graph below.



150Vdc

Iout	Vout	Vin (Vdc)	Iin (mAdc)	Pin	Pout	Losses	Efficiency
0.301	12.04	152.2	31	4.72	3.62	1.09	76.8%
0.600	12.04	152.2	60	9.13	7.22	1.91	79.1%
0.899	12.04	152.2	88	13.39	10.82	2.57	80.8%
1.202	12.04	152.2	111	16.89	14.47	2.42	85.7%
1.503	12.04	152.2	137	20.85	18.10	2.76	86.8%
1.805	12.04	152.2	164	24.96	21.73	3.23	87.1%
2.100	12.04	152.1	190	28.90	25.28	3.62	87.5%
2.398	12.04	152.1	216	32.85	28.87	3.98	87.9%
2.699	12.04	152.1	244	37.11	32.50	4.62	87.6%
3.000	12.04	152.1	272	41.37	36.12	5.25	87.3%

300Vdc

Iout	Vout	Vin (Vdc)	Iin (mAdc)	Pin	Pout	Losses	Efficiency
0.301	12.05	300.0	16	4.80	3.63	1.17	75.6%
0.600	12.04	300.0	31	9.30	7.22	2.08	77.7%
0.900	12.04	300.0	45	13.50	10.84	2.66	80.3%
1.202	12.04	300.0	60	17.85	14.47	3.38	81.1%
1.504	12.04	300.0	71	21.30	18.11	3.19	85.0%
1.799	12.04	300.0	84	25.20	21.66	3.54	86.0%
2.098	12.04	300.0	97	29.10	25.26	3.84	86.8%
2.399	12.04	300.0	111	33.30	28.88	4.42	86.7%
2.700	12.04	300.0	125	37.35	32.51	4.84	87.0%
3.001	12.04	300.0	138	41.40	36.13	5.27	87.3%

3 Standby Mode Power Consumption

The tables below show the input power and efficiency during light load operation.

150Vdc

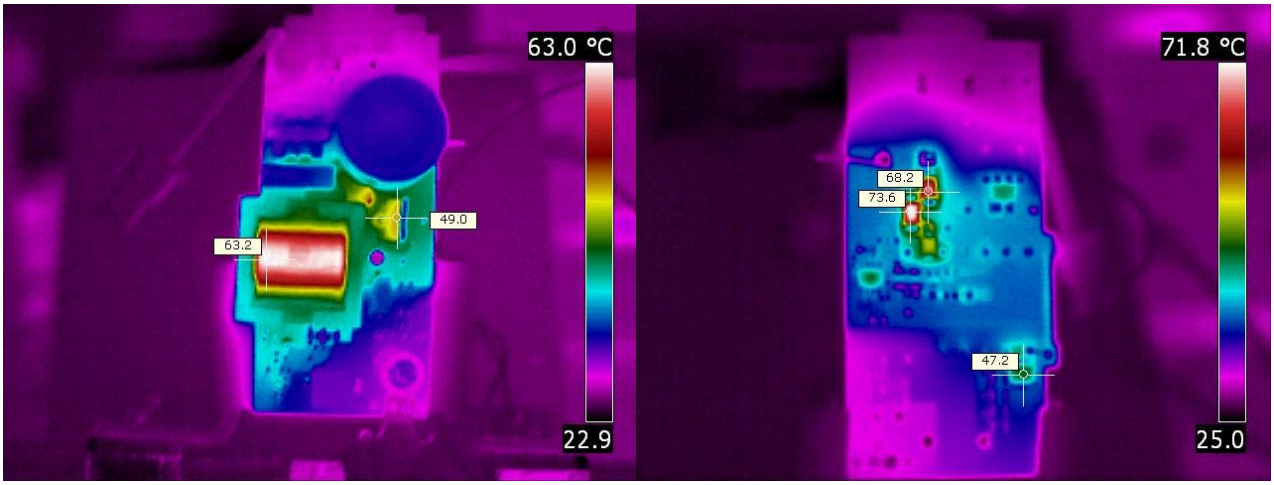
Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.05	154.2	0.42	65	0	65	0.0%
0.025	12.05	154.1	2.99	461	301	160	65.4%
0.050	12.05	154.1	5.64	869	603	267	69.3%
0.065	12.05	154.1	7.27	1120	783	337	69.9%

300Vdc

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.05	299.2	0.45	135	0	135	0.0%
0.025	12.05	299.2	1.80	539	301	237	55.9%
0.050	12.05	299.2	3.18	951	603	349	63.3%
0.065	12.05	299.2	4.03	1206	783	423	65.0%

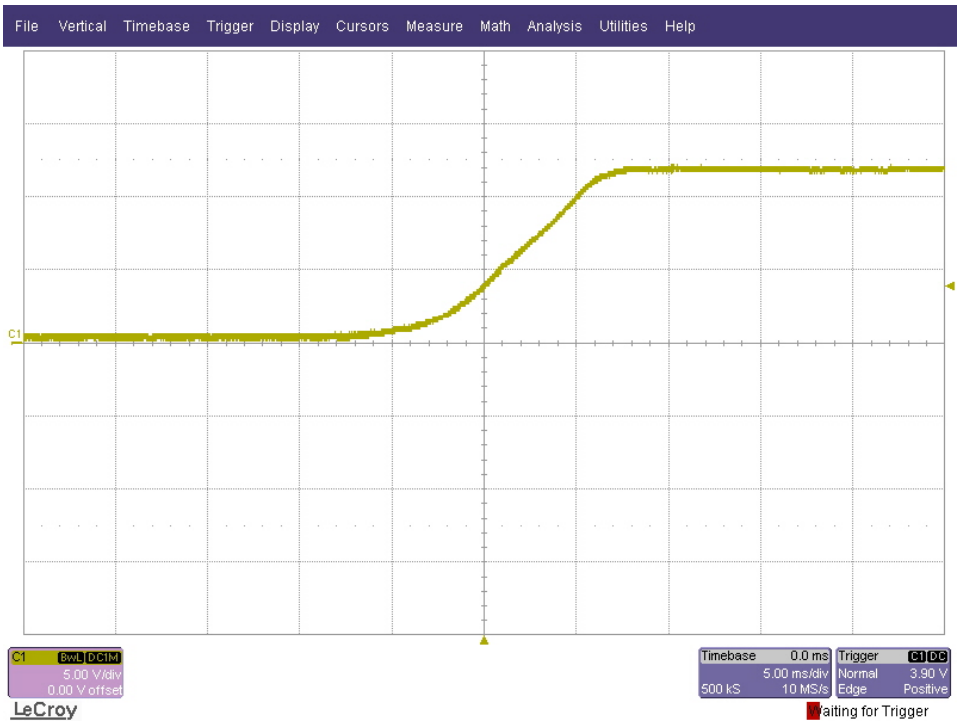
4 Thermal Image

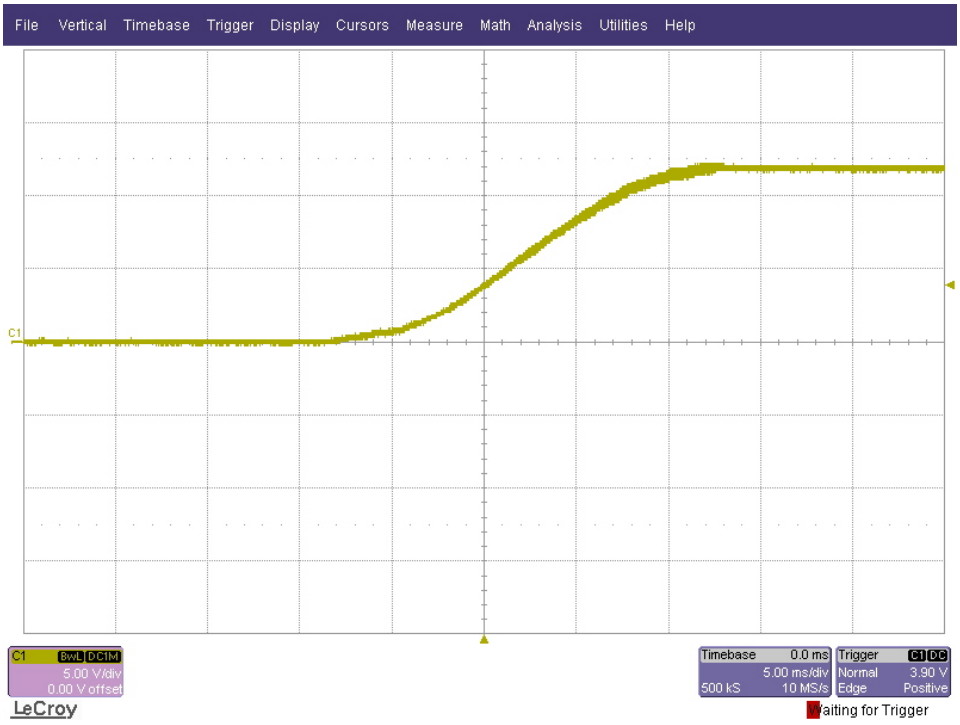
The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 26ºC with no forced air flow. The input was 300VDC, and the output was loaded with 3A.



5 Startup

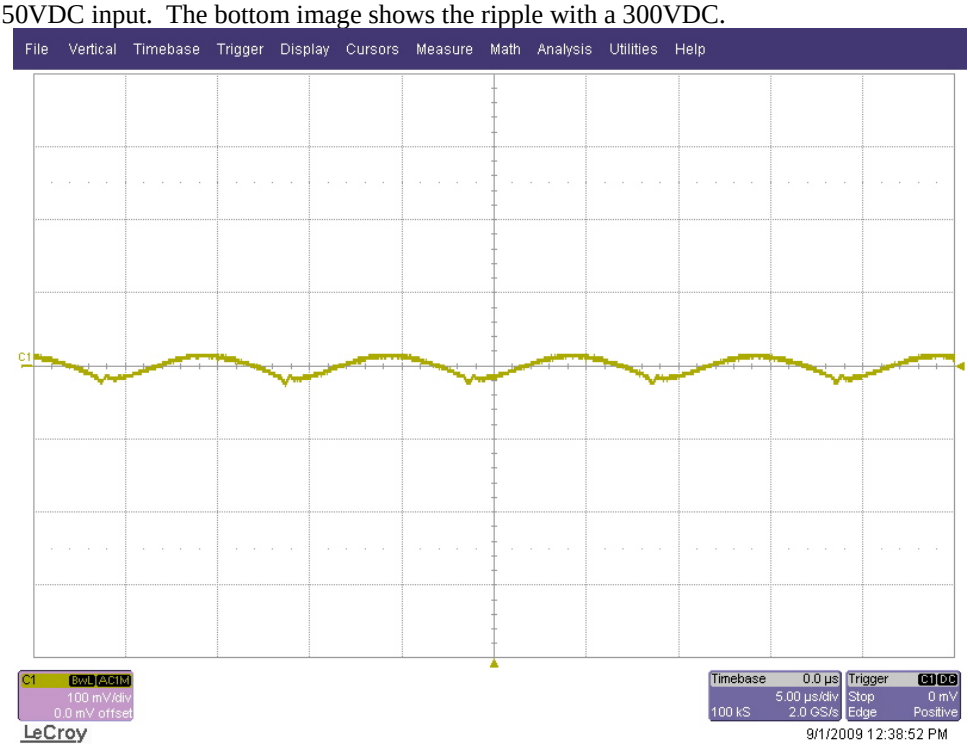
The output voltage at startup is shown in the images below. The input was 150VDC. For the top image, the output was unloaded. For the bottom image, the output was loaded with 3A.

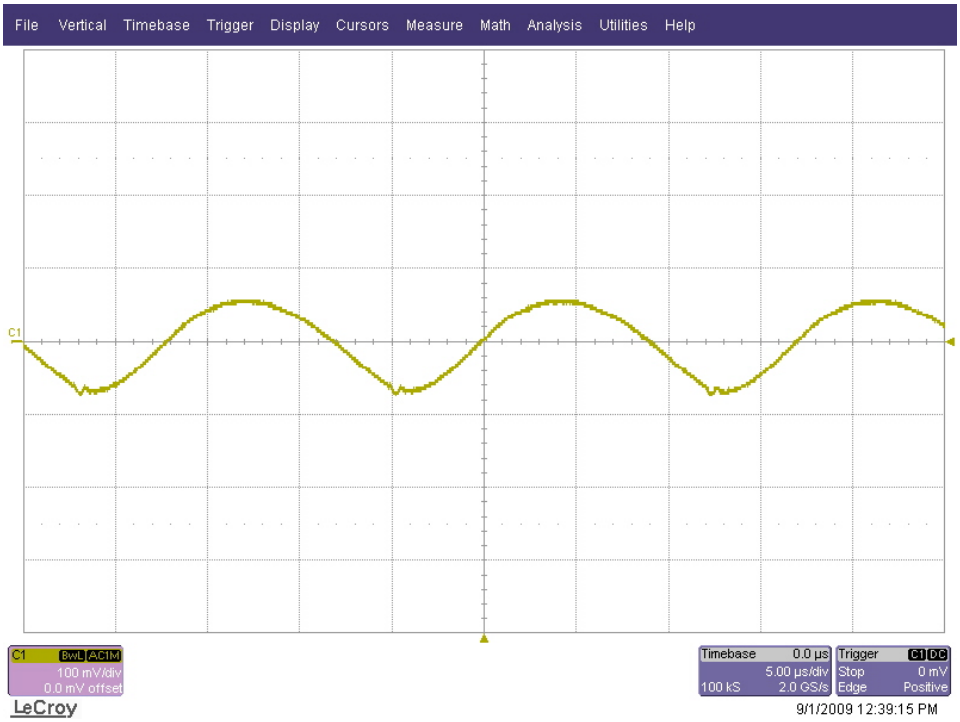




6 Output Ripple Voltage – Full Load

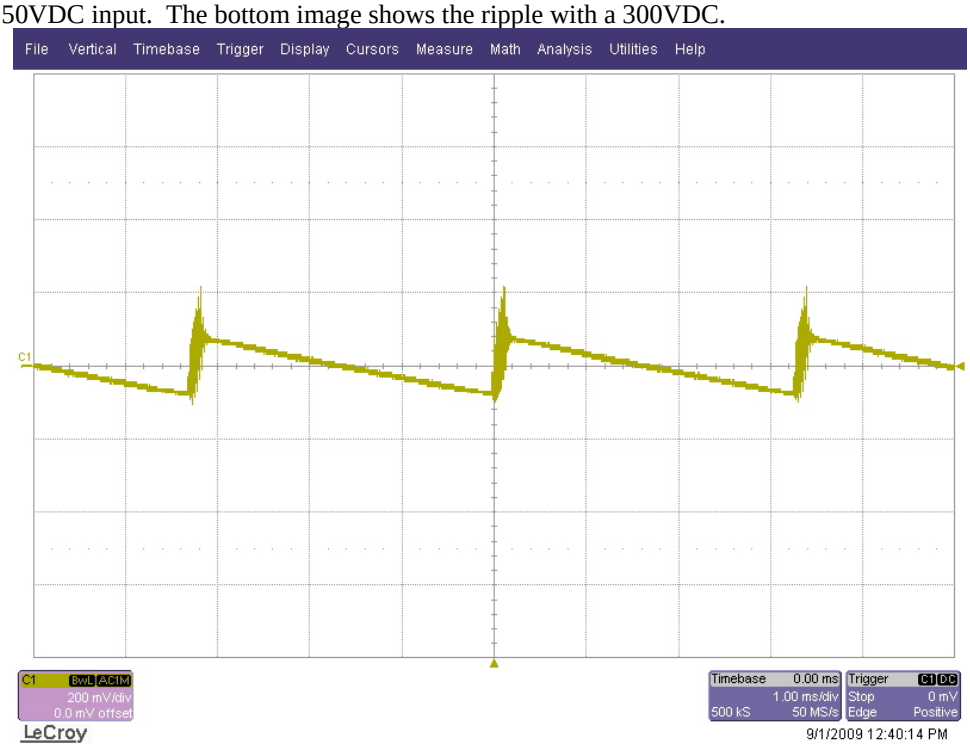
The output ripple voltage during full load operation (3A load) is shown in the plots below. The top image shows the ripple with a 150VDC input. The bottom image shows the ripple with a 300VDC.

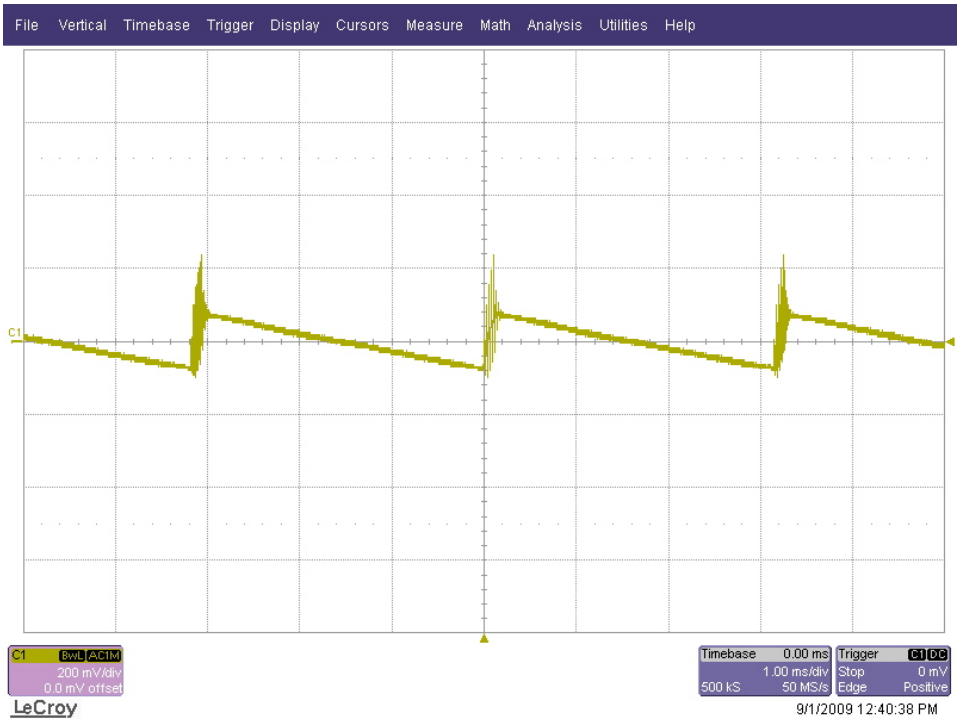




7 Output Ripple Voltage – Light Load

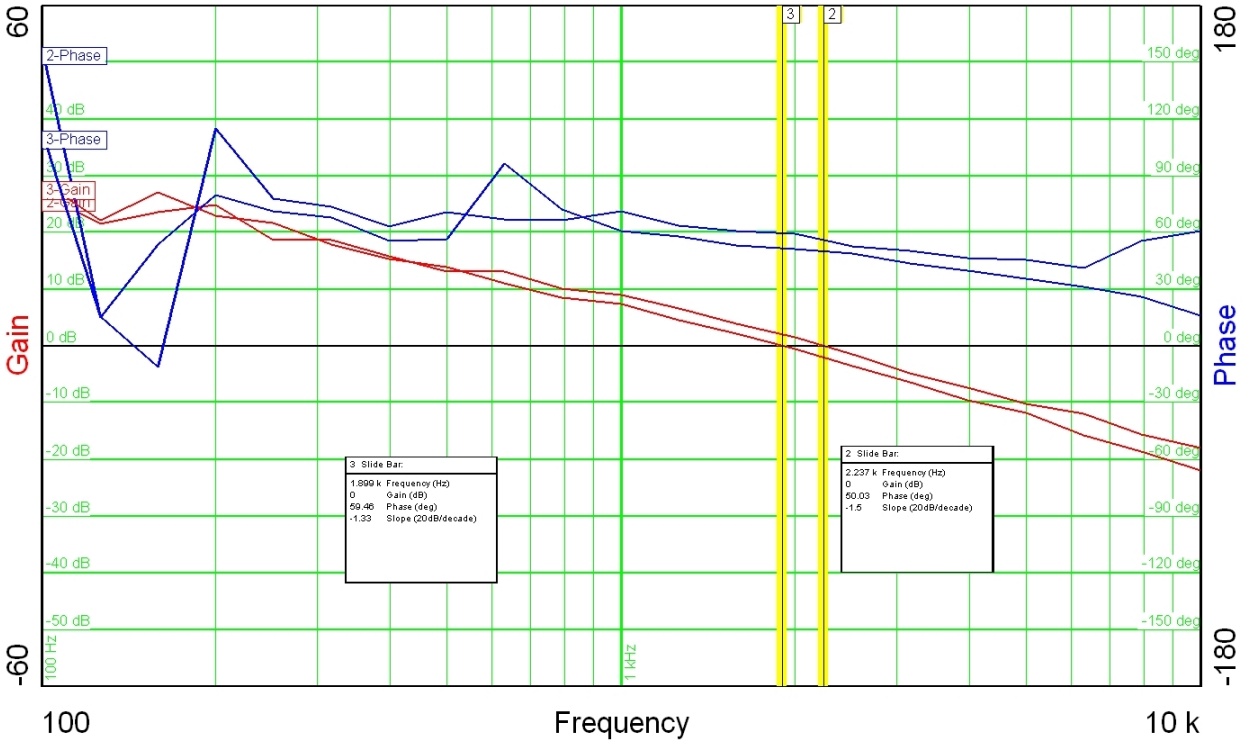
The output ripple voltage during light load operation (50ma load) is shown in the plots below. The top image shows the ripple with a 150VDC input. The bottom image shows the ripple with a 300VDC.





8 Loop Response

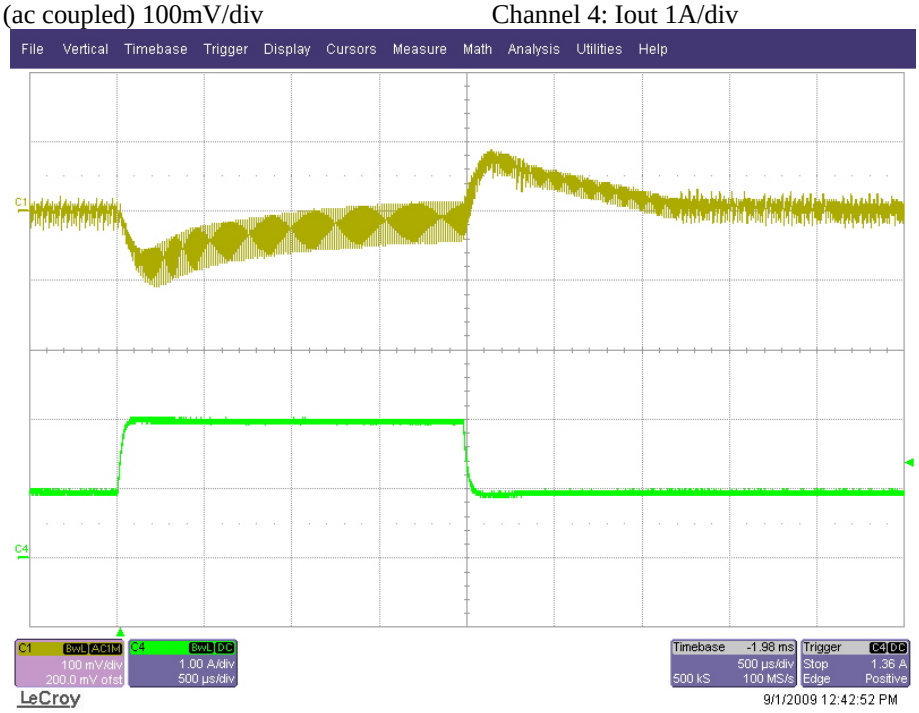
The image below shows the loop response of the converter. The upper gain/phase plot was measured with a 150Vdc input, and a 3A load. The lower gain/phase plot was measured with a 300Vdc input and a 3A load.



9 Load Transients

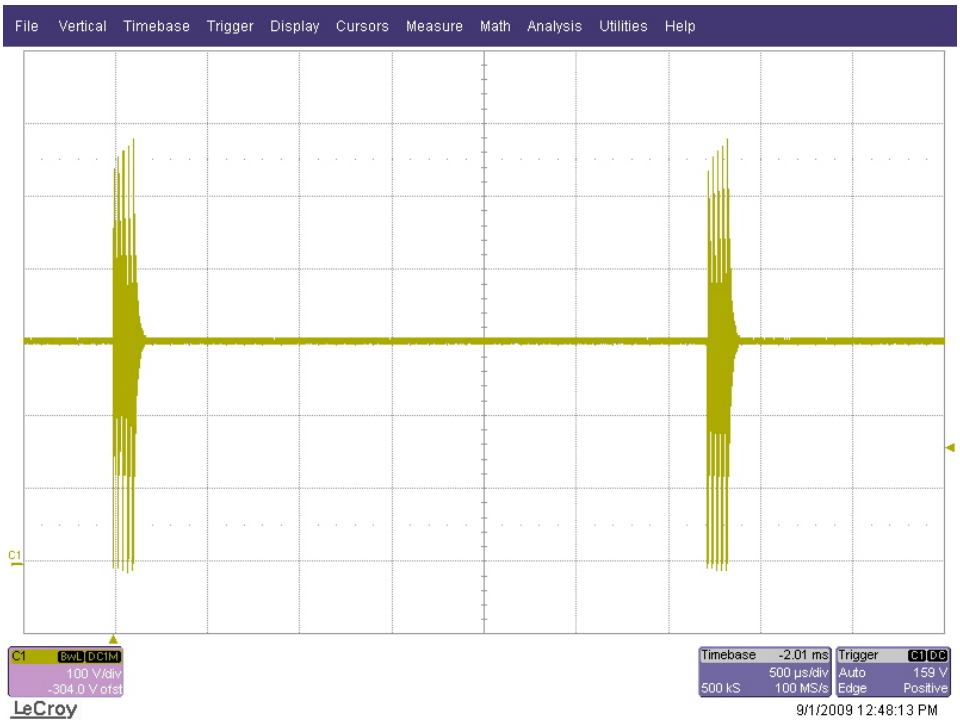
The images below show the response to a 1A to 2A load transient. For the top image, the input voltage was set to 150VDC. For the bottom image, the input was set to 300VDC.

Channel 1: Vout (ac coupled) 100mV/div Channel 4: Iout 1A/div



10 Switching Waveforms

The images below show the drain-to-source voltage waveform on the primary MOSFET (Q5). The top image demonstrates burst mode operation, where the load as 50mA and the input was set to 150VDC. In the bottom image, the load was 3A and the input was 150VDC.




File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C1
C1 BwL DC1M
100 V/div
-304.0 V ofst
LeCroy
Timebase 0.0 µs
5.00 µs/div
100 kS 2.0 GS/s
Trigger C1 DC
Auto 442 V
Edge Positive
9/1/2009 1:50:19 PM

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