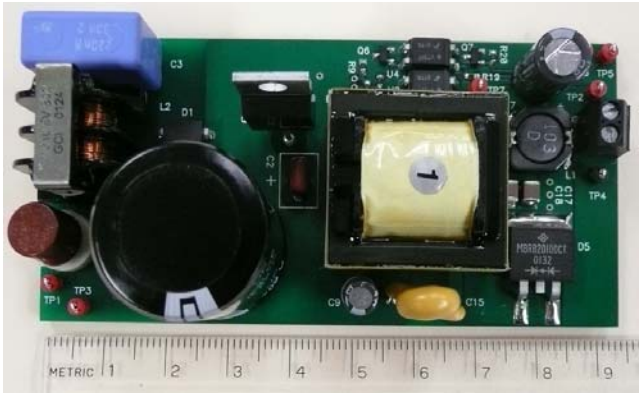
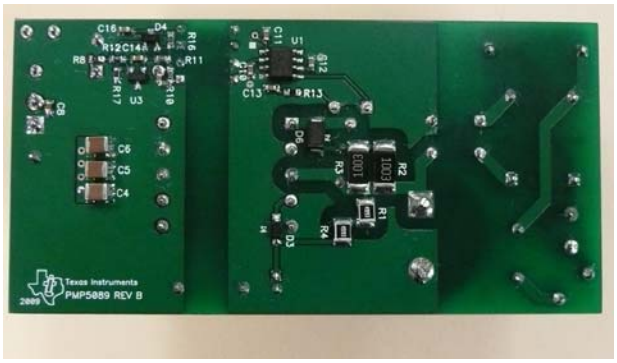
PMP5089 Rev C Test Results

1 Photo

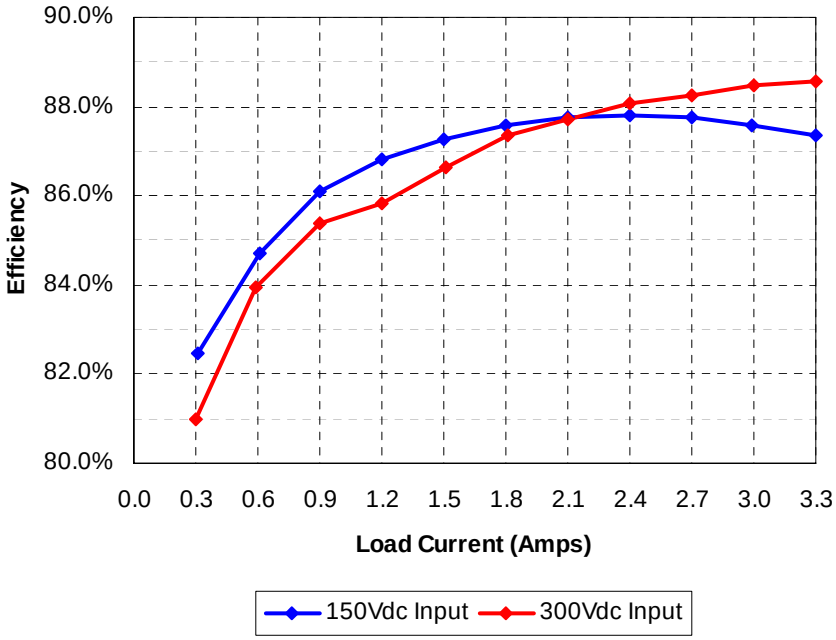
The photographs below show the top and bottom views of the PMP5089 Rev C demo board. The circuit is built on a PMP5089 Rev B PWB.





2 Efficiency

The efficiency data is shown in the tables and graph below.



150Vdc

Iout	Vout	Vin (Vdc)	Iin (mAdc)	Pin	Pout	Losses	Efficiency
0.305	12.00	150.5	29.49	4.44	3.66	0.78	82.5%
0.605	12.00	150.4	57.0	8.57	7.26	1.31	84.7%
0.904	11.99	150.4	83.7	12.59	10.84	1.75	86.1%
1.199	11.99	150.3	110.2	16.56	14.38	2.19	86.8%
1.500	11.99	150.2	137.2	20.61	17.99	2.62	87.3%
1.798	11.99	150.2	163.9	24.62	21.56	3.06	87.6%
2.096	11.99	150.1	190.8	28.64	25.13	3.51	87.8%
2.403	11.99	150.1	218.6	32.81	28.81	4.00	87.8%
2.704	11.99	150.0	246.3	36.95	32.42	4.52	87.8%
2.993	11.99	150.0	273.2	40.98	35.89	5.09	87.6%
3.299	11.99	149.9	302.1	45.28	39.56	5.73	87.3%

300Vdc

Iout	Vout	Vin (Vdc)	Iin (mAdc)	Pin	Pout	Losses	Efficiency
0.300	12.00	300.2	14.81	4.45	3.60	0.85	81.0%
0.595	12.00	300.2	28.34	8.51	7.14	1.37	83.9%
0.903	12.00	300.1	42.29	12.69	10.84	1.86	85.4%
1.198	11.99	300.1	55.76	16.73	14.36	2.37	85.8%
1.507	11.99	300.1	69.5	20.86	18.07	2.79	86.6%
1.806	11.99	300.1	82.6	24.79	21.65	3.13	87.4%
2.100	11.99	300.0	95.7	28.71	25.18	3.53	87.7%
2.402	11.99	300.0	109.0	32.70	28.80	3.90	88.1%
2.701	11.99	300.0	122.3	36.69	32.38	4.31	88.3%
2.999	11.99	300.0	135.5	40.65	35.96	4.69	88.5%
3.301	11.99	299.9	149.0	44.69	39.58	5.11	88.6%

3 Standby Mode Power Consumption

The tables below show the input power and efficiency during light load operation.

150Vdc

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.01	150.3	1.08	162	0	162	0.0%
0.025	12.00	150.3	3.26	490	300	190	61.2%
0.050	12.00	150.3	5.66	851	600	251	70.5%

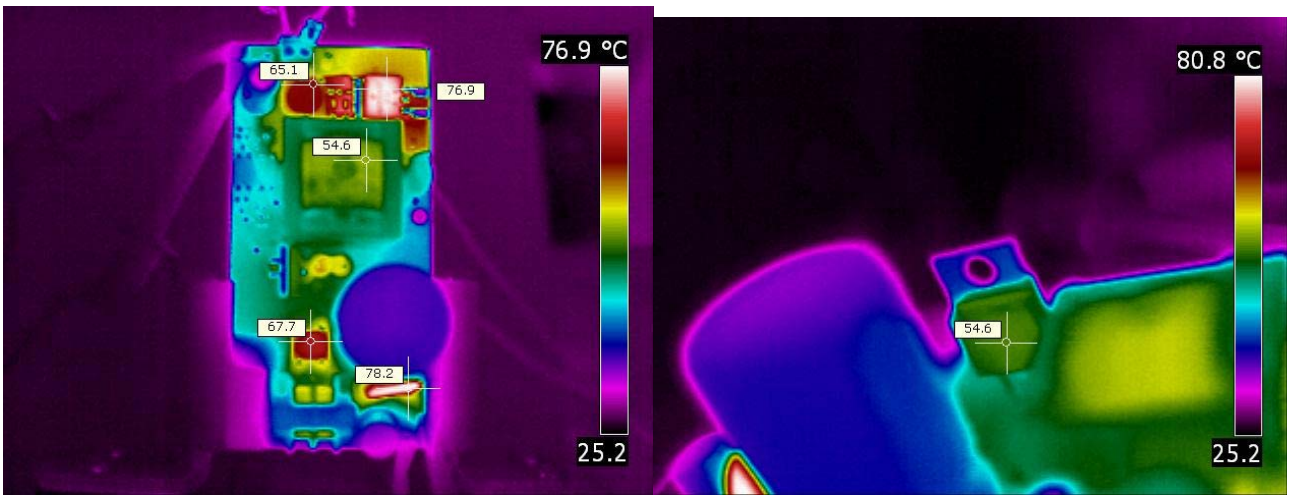
300Vdc

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.01	300.9	0.80	241	0	241	0.0%
0.025	12.00	300.9	1.90	572	300	272	52.5%
0.050	12.00	300.9	3.11	936	600	336	64.1%

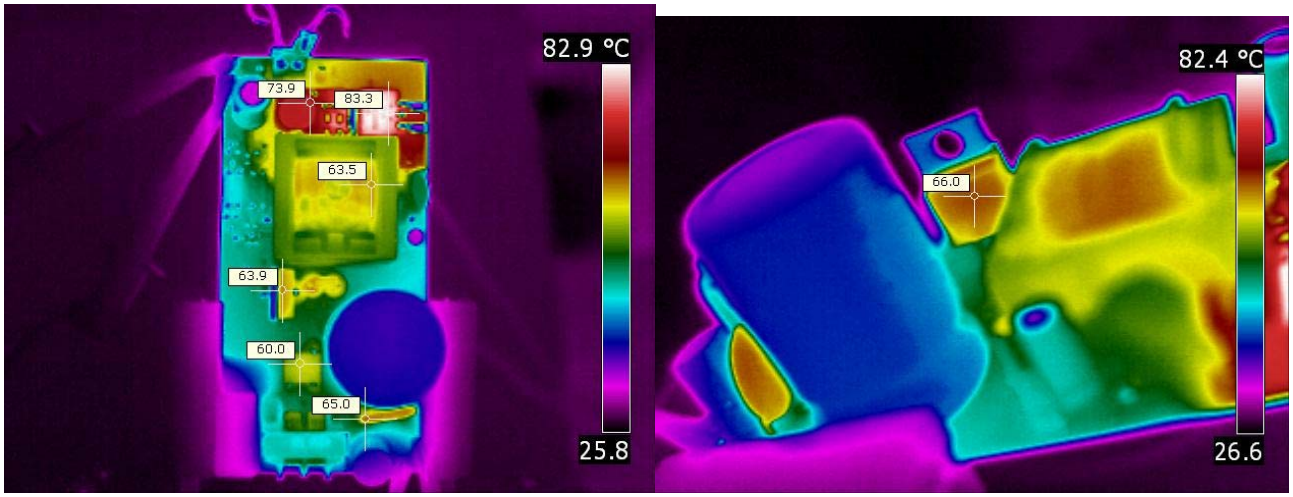
4 Thermal Images

The thermal images below show a top view (left) of the board and close up view (right) of the main FET (Q1). The ambient temperature was 26ºC with no forced air flow. The output was loaded with 3.3A.

4.1 115VAC, 60Hz

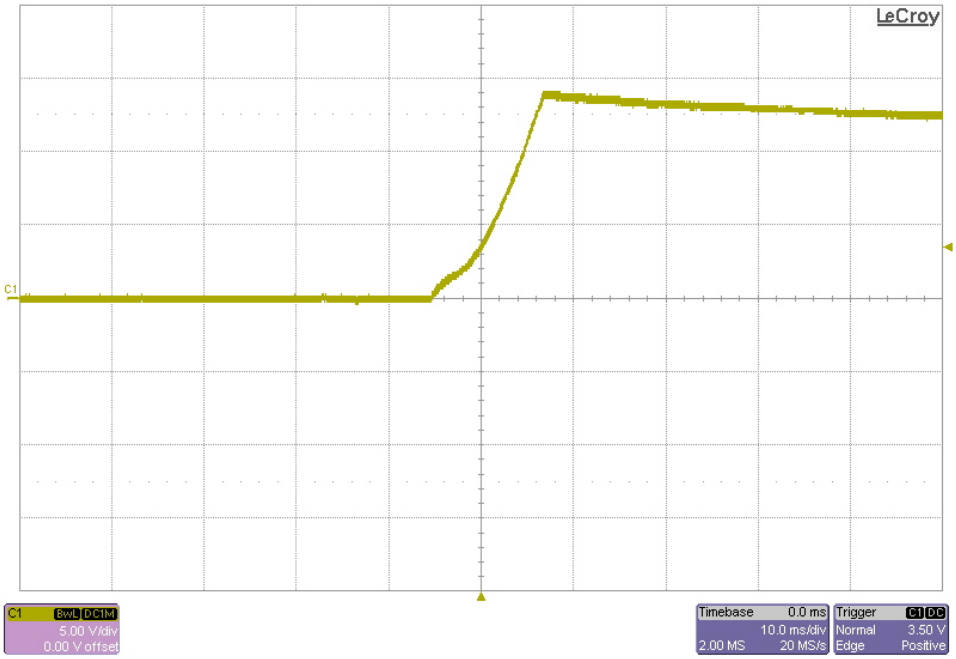


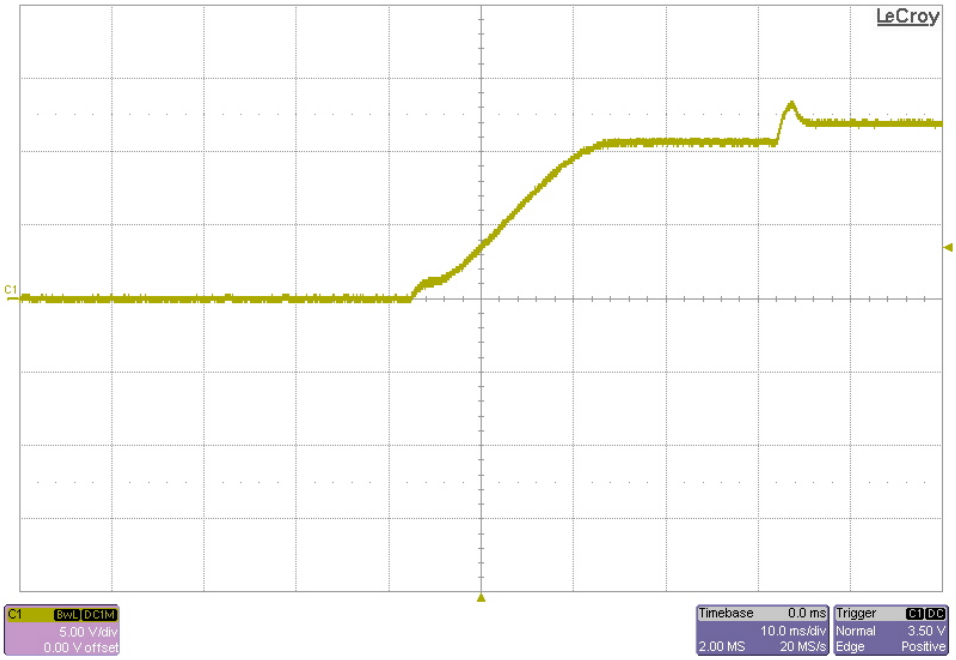
4.2 220VAC, 50Hz Input



5 Startup

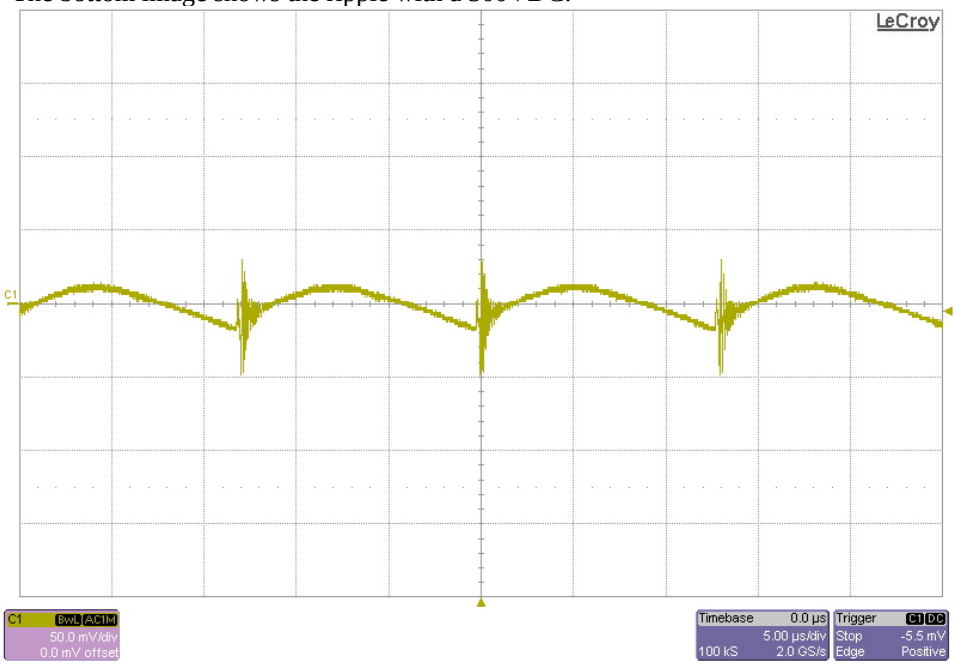
The output voltage at startup is shown in the images below. The input was 150VDC. For the top image, the output was unloaded. For the bottom image, the output was loaded with 3.3A.

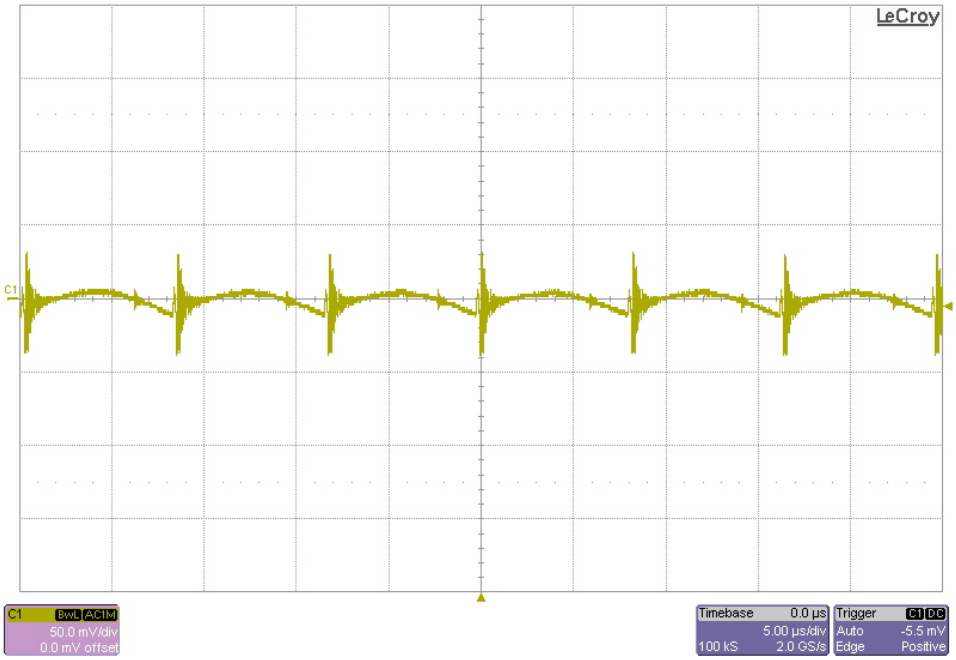




6 Output Ripple Voltage – Full Load

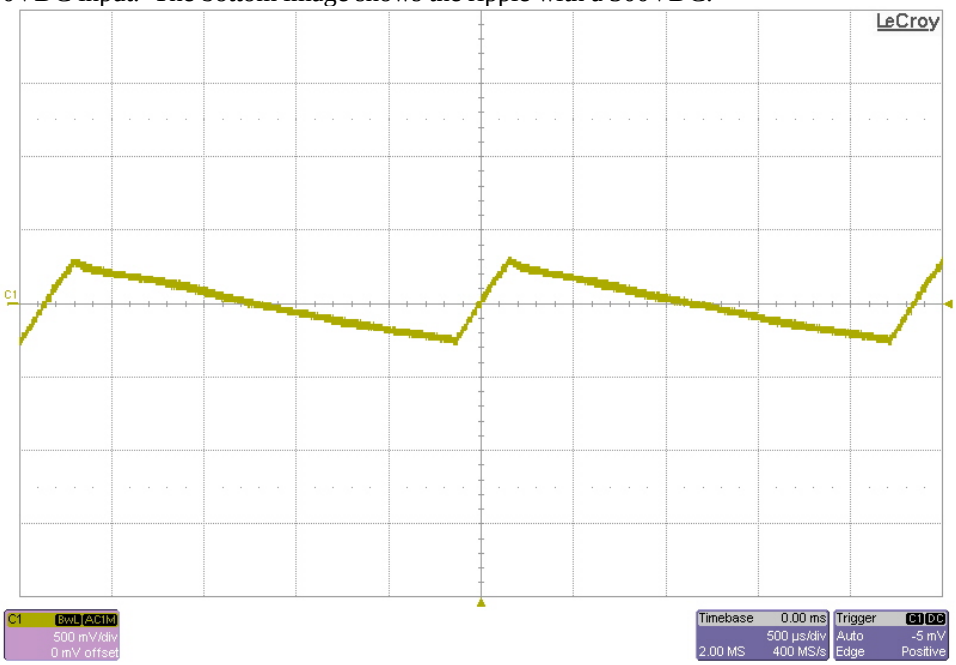
The output ripple voltage during full load operation is shown in the plots below. The top image shows the ripple with a 150VDC input. The bottom image shows the ripple with a 300VDC.

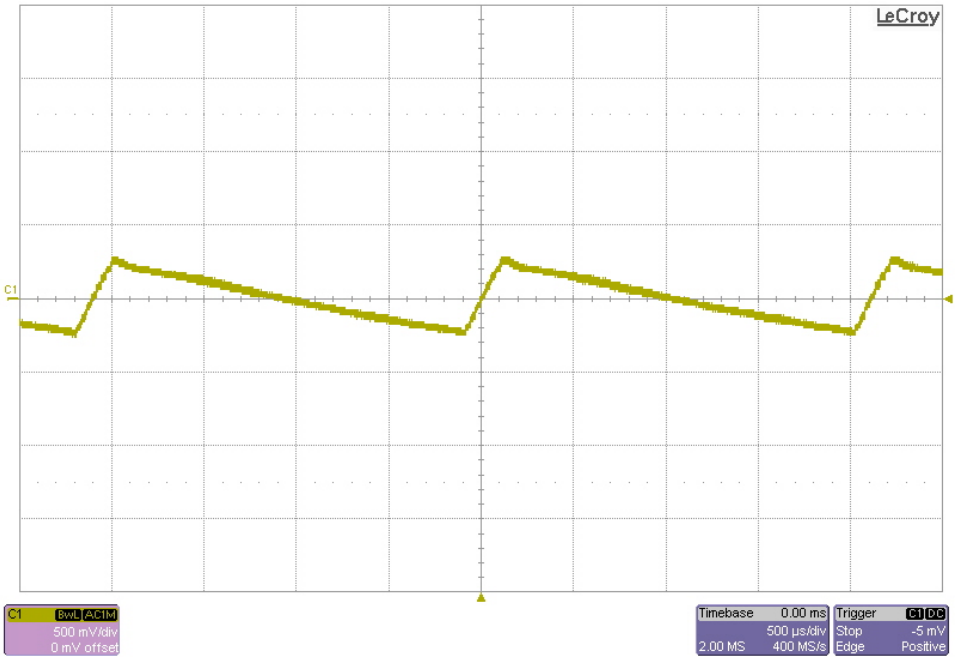




7 Output Ripple Voltage – Light Load

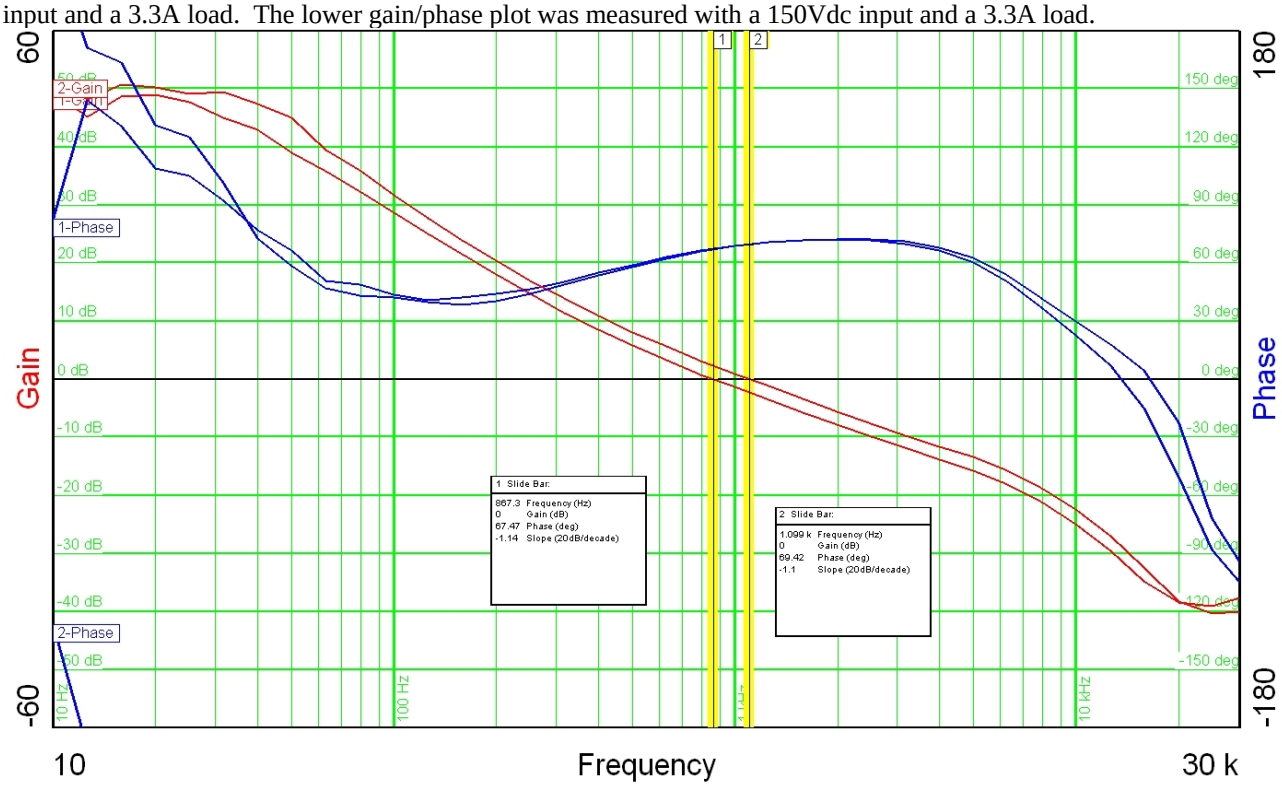
The output ripple voltage during light load operation (100mA) is shown in the plots below. The top image shows the ripple with a 150VDC input. The bottom image shows the ripple with a 300VDC.





8 Loop Response

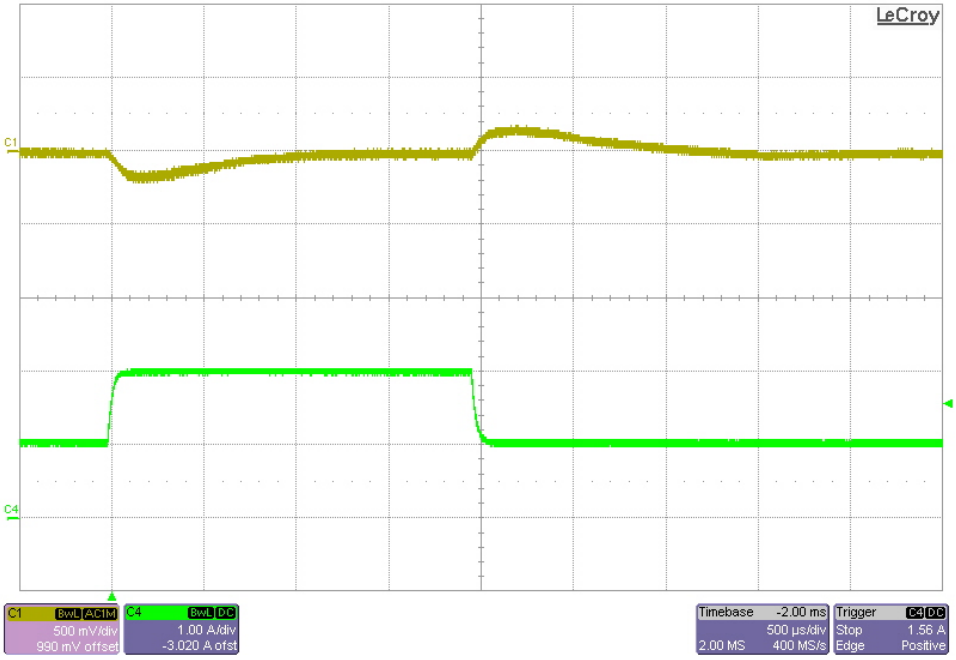
The image below shows the loop response of the converter. The upper gain/phase plot was measured with a 300Vdc input and a 3.3A load. The lower gain/phase plot was measured with a 150Vdc input and a 3.3A load.

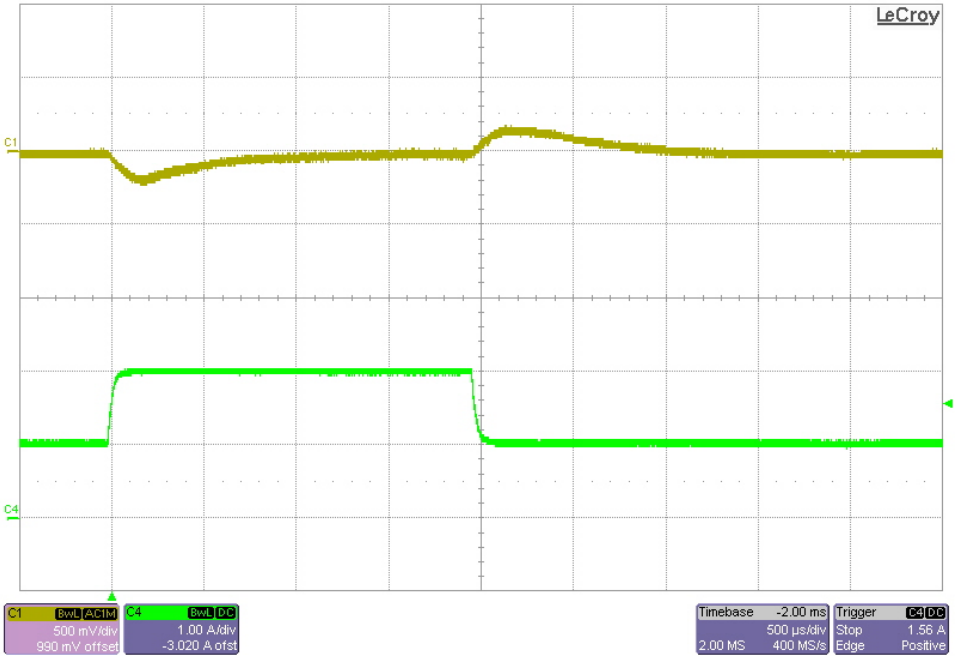


9 Load Transients

The images below show the response to a 1A to 2A load transient. For the top image, the input voltage was set to 150VDC. For the bottom image, the input was set to 300VDC.

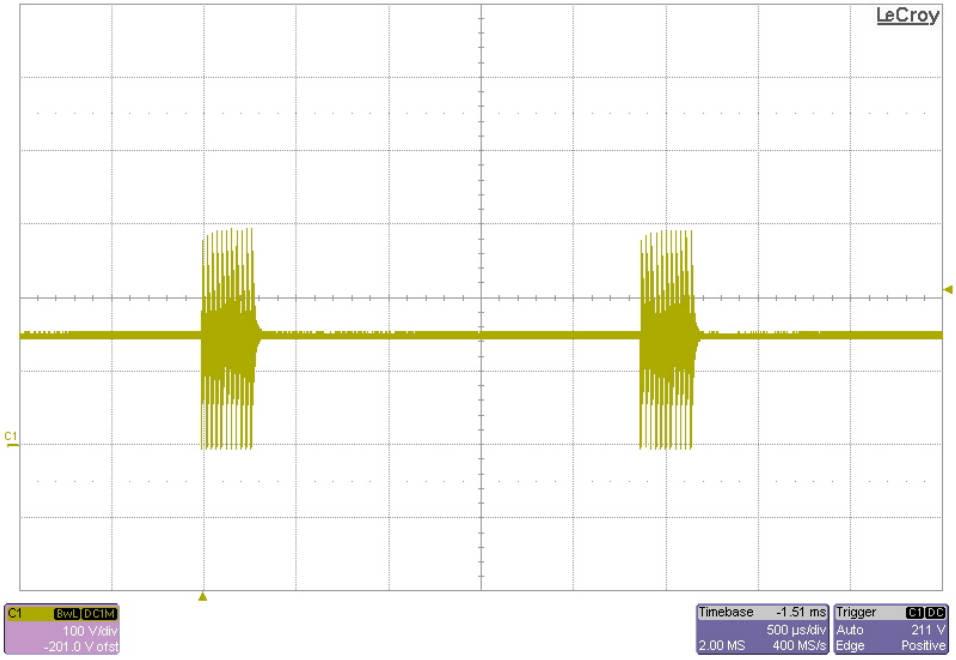
Channel 1: Vout (ac coupled) 500mV/div Channel 4: Iout 1A/div

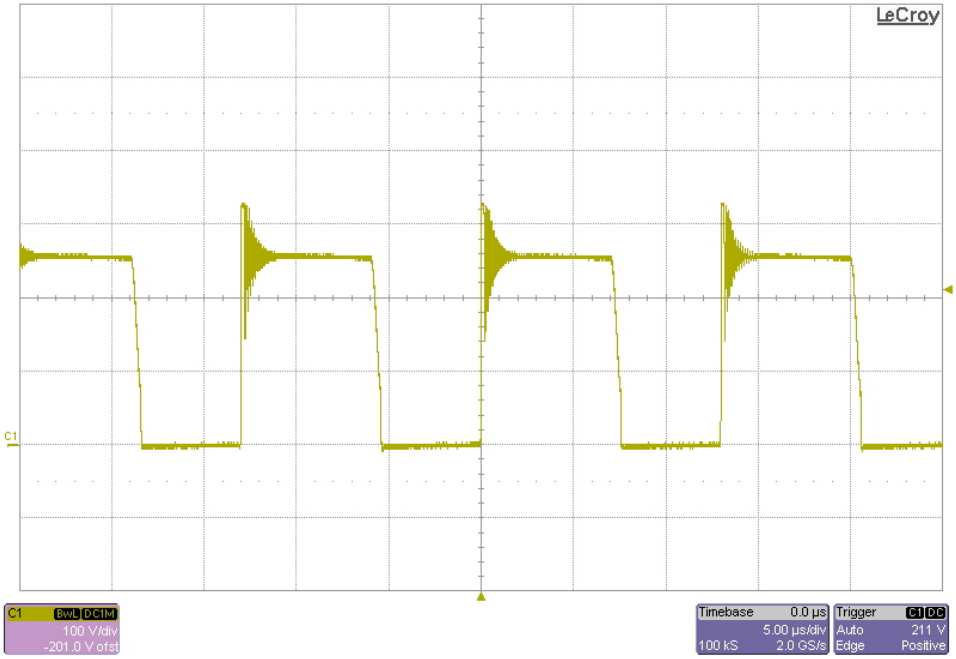




10 Switching Waveforms

The images below show the drain-to-source voltage waveform on the primary MOSFET (Q1). The top image demonstrates burst mode operation, where the load was 100mA and the input was set to 150VDC. In the bottom image, the load was 3.3A and the input was 150VDC.





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