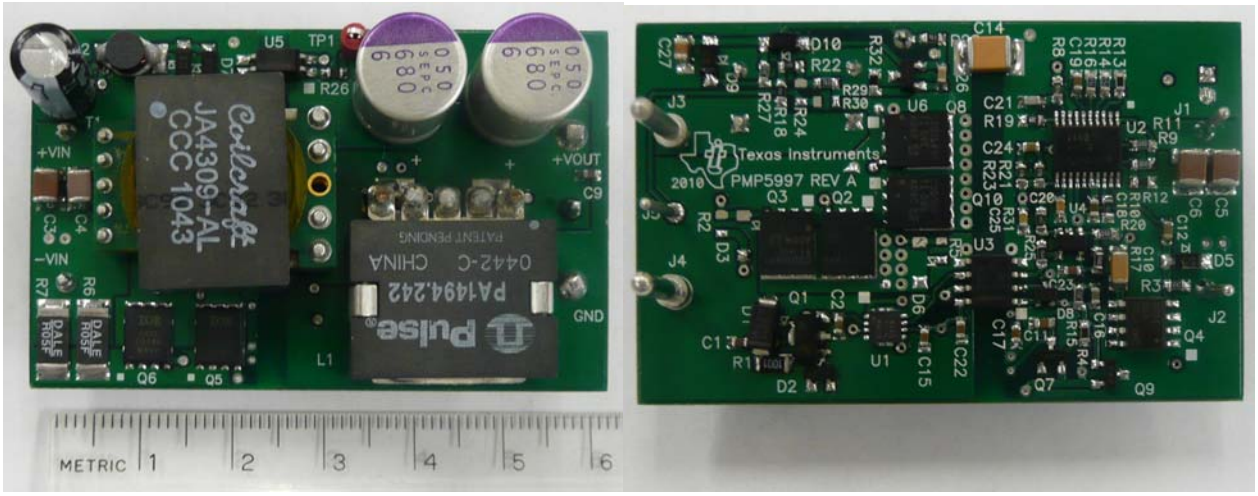
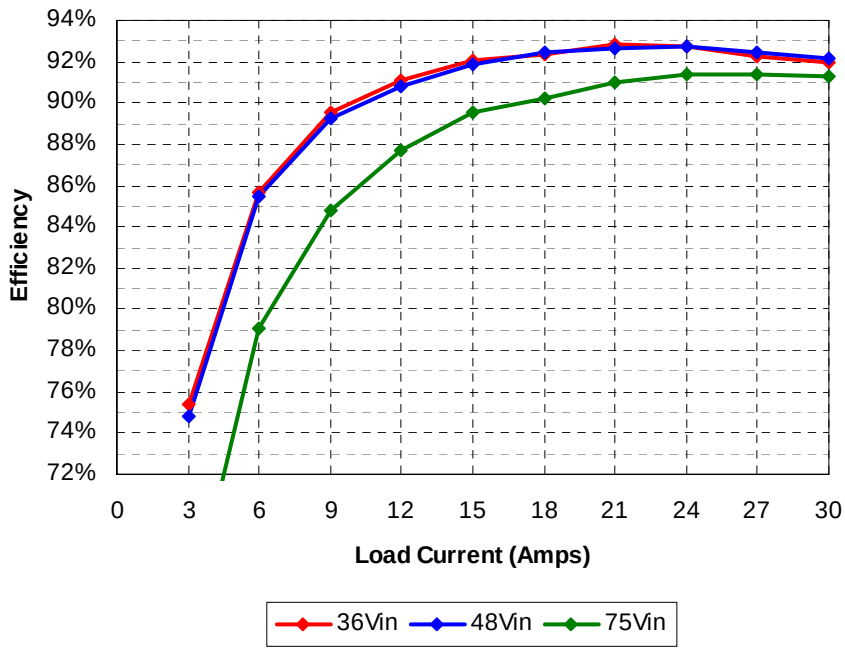
1 Photo

The photo below shows the PMP5997 Rev B demo board. This circuit was built on a PMP5997_REVA PCB.



2 Efficiency

The efficiency data is shown in the tables and graph below.



Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
36.0	0.092	0.000	3.28	0.00	3.312	0.0%
36.0	0.361	2.993	3.27	9.80	3.198	75.4%
36.0	0.635	5.99	3.27	19.59	3.270	85.7%
36.0	0.913	9.00	3.27	29.43	3.434	89.6%
36.0	1.196	11.99	3.27	39.21	3.843	91.1%
36.0	1.480	15.0	3.27	49.05	4.223	92.1%
36.0	1.770	18.0	3.27	58.86	4.860	92.4%
36.0	2.054	21.0	3.27	68.67	5.264	92.9%
36.0	2.351	24.0	3.27	78.48	6.145	92.7%
36.0	2.658	27.0	3.27	88.29	7.385	92.3%
36.0	2.963	30.0	3.27	98.10	8.568	92.0%

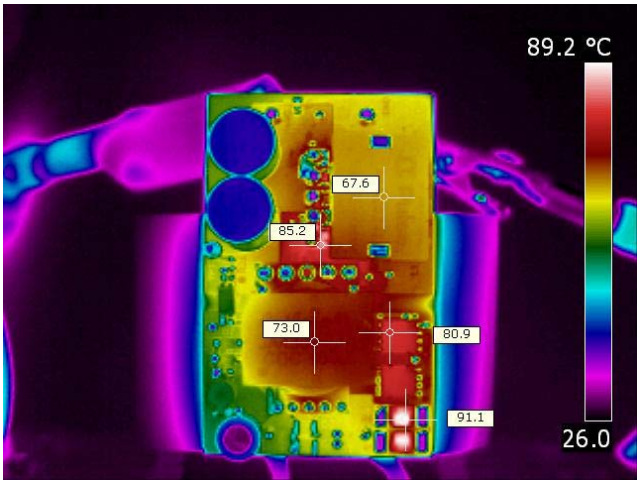
Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
48.0	0.072	0.000	3.28	0.00	3.456	0.0%
48.0	0.274	3.000	3.28	9.84	3.310	74.8%
48.0	0.478	5.98	3.28	19.62	3.323	85.5%
48.0	0.689	9.00	3.28	29.52	3.547	89.3%
48.0	0.900	12.00	3.27	39.24	3.954	90.8%
48.0	1.113	15.0	3.27	49.05	4.366	91.8%
48.0	1.328	18.0	3.27	58.89	4.842	92.4%
48.0	1.544	21.0	3.27	68.67	5.431	92.7%
48.0	1.764	24.0	3.27	78.48	6.179	92.7%
48.0	1.990	27.0	3.27	88.29	7.214	92.4%
48.0	2.219	30.0	3.27	98.10	8.394	92.1%

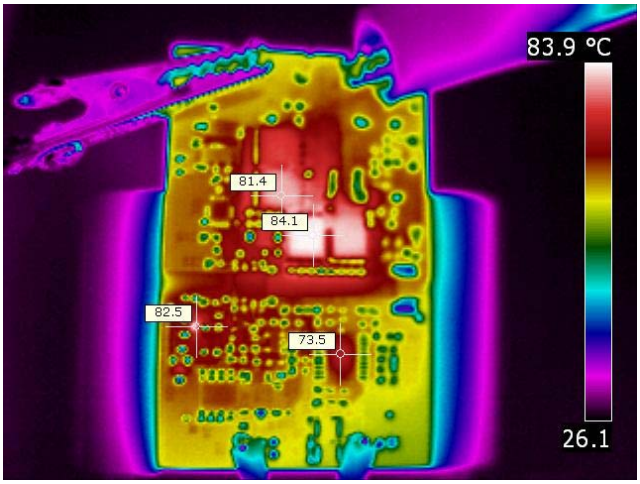
Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
75.0	0.076	0.000	3.28	0.00	5.700	0.0%
75.0	0.202	2.999	3.28	9.84	5.313	64.9%
75.0	0.332	6.00	3.28	19.68	5.220	79.0%
75.0	0.464	9.00	3.28	29.52	5.280	84.8%
75.0	0.598	11.99	3.28	39.33	5.523	87.7%
75.0	0.733	15.0	3.28	49.20	5.775	89.5%
75.0	0.870	18.0	3.27	58.89	6.357	90.3%
75.0	1.006	21.0	3.27	68.67	6.780	91.0%
75.0	1.145	24.0	3.27	78.48	7.395	91.4%
75.0	1.288	27.0	3.27	88.29	8.310	91.4%
75.0	1.433	30.0	3.27	98.10	9.375	91.3%

3 Thermal Images

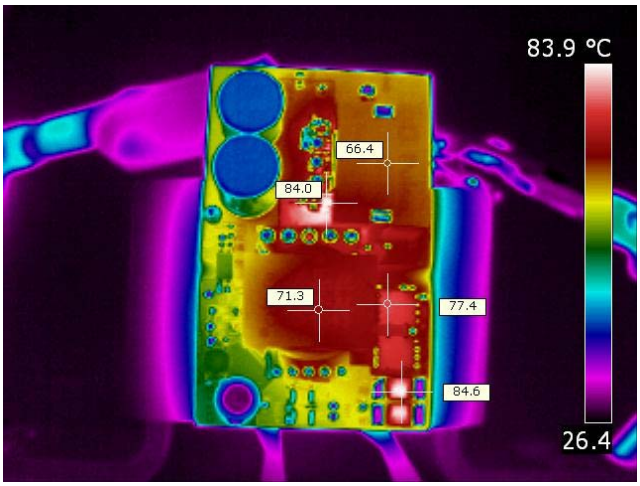
The thermal images below show a top and bottom view of the board with a 30A load and 300LFM of forced air flow. The ambient temperature was 26ºC.

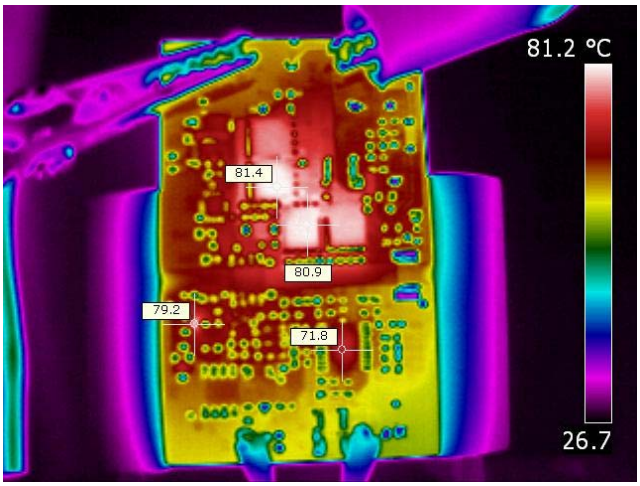
3.1 36Vin



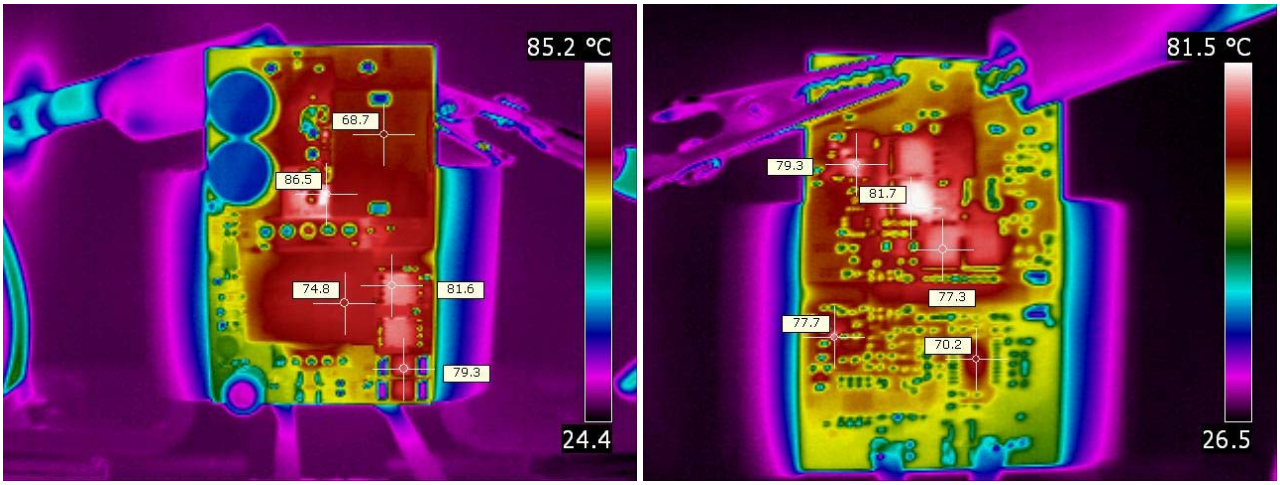


3.2 48Vin





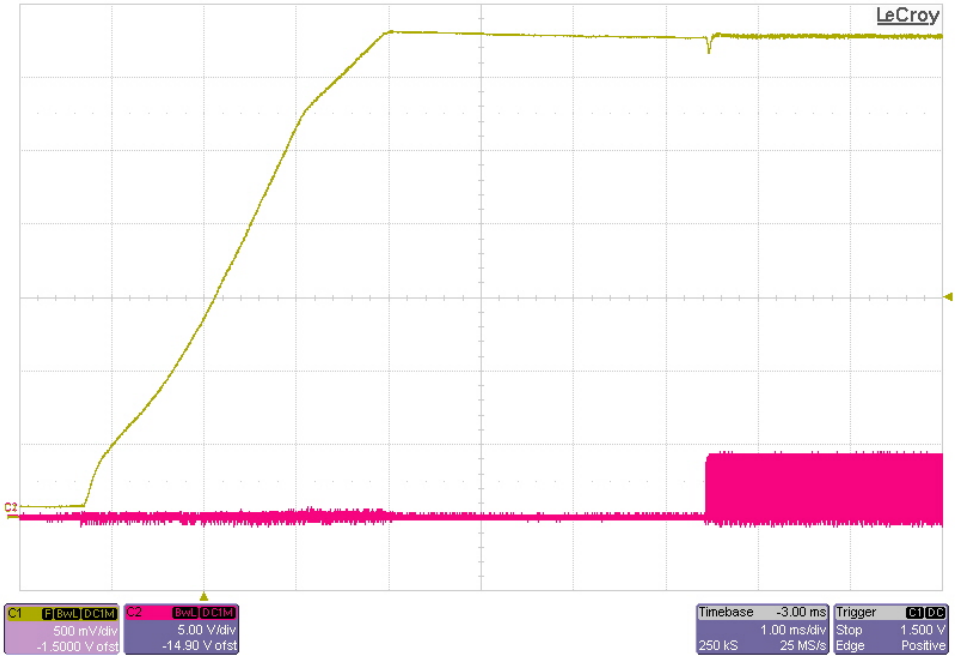
3.3 75Vin



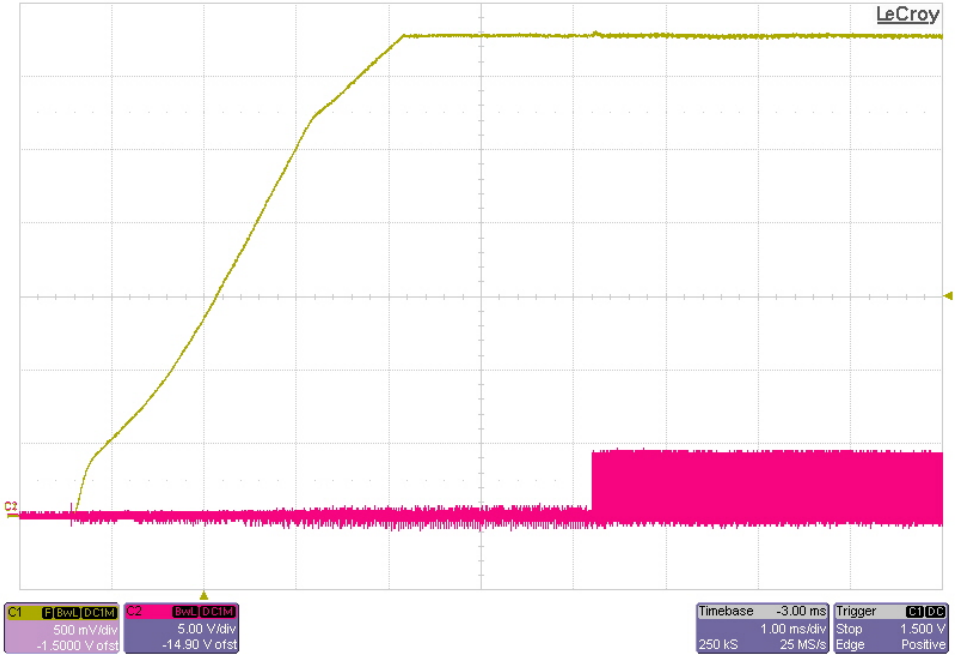
4 Startup

The output voltage at startup is shown in the images below. Channel 1 shows the output voltage, and channel 2 shows the voltage on the gates of Q8 and Q10.

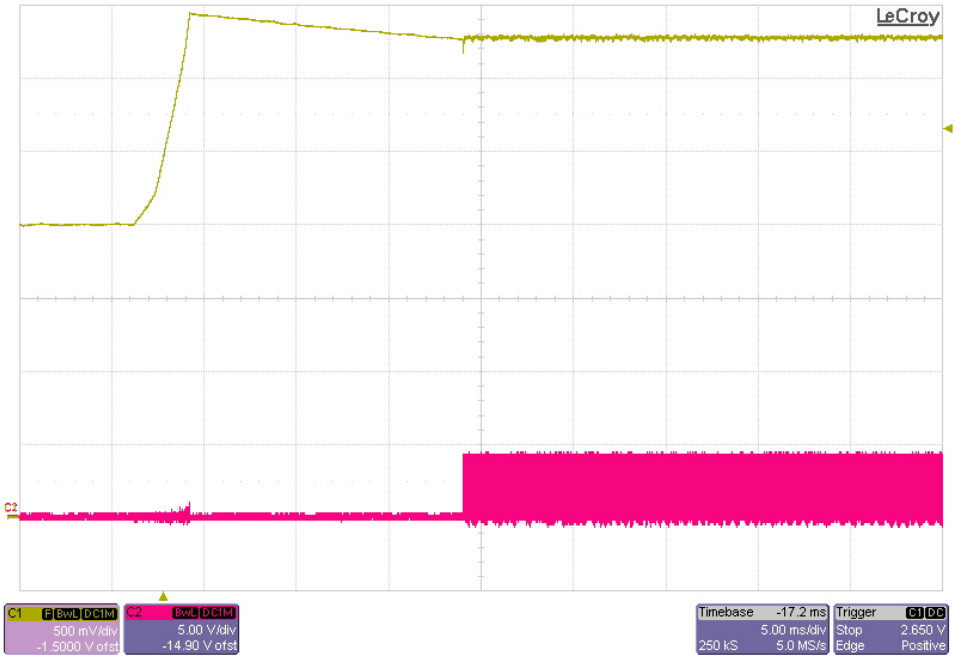
4.1 36V Input, No Load, No Pre-bias



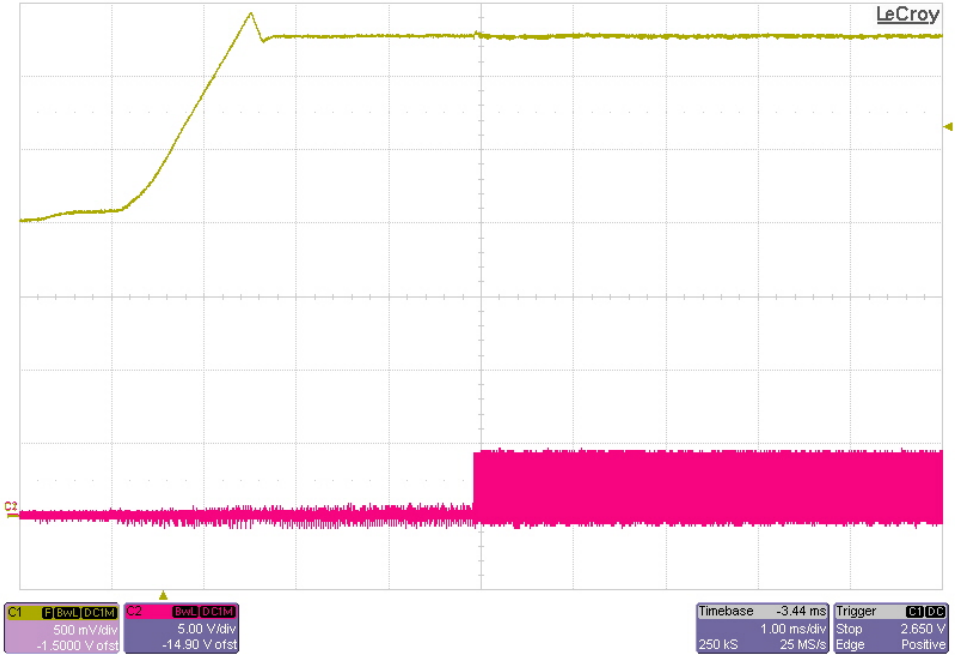
4.2 36V Input, 1 Ohm Load, No Pre-bias



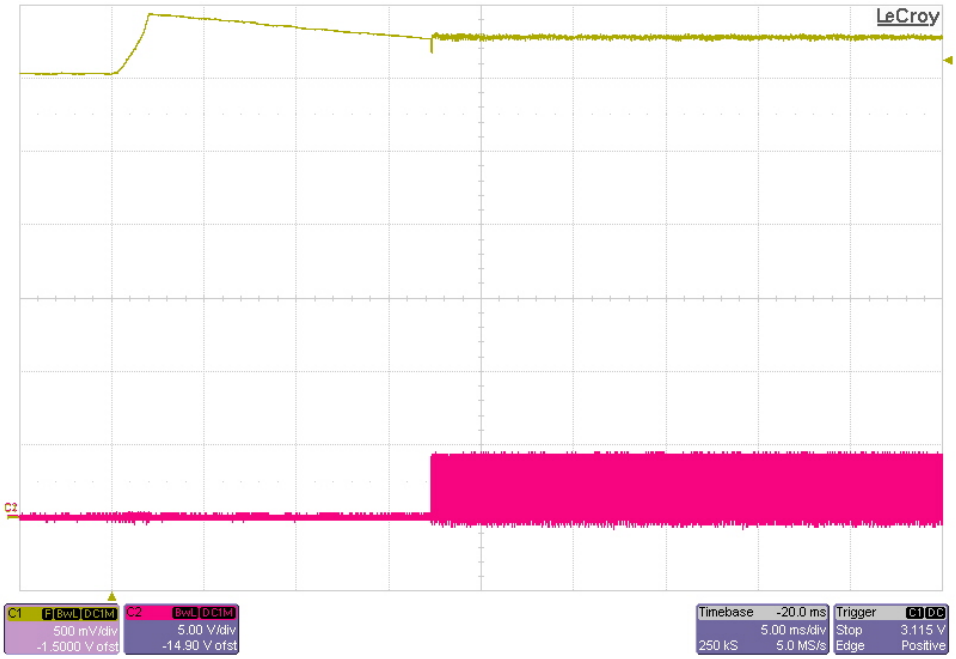
4.3 36V Input, No Load, 2V Pre-bias



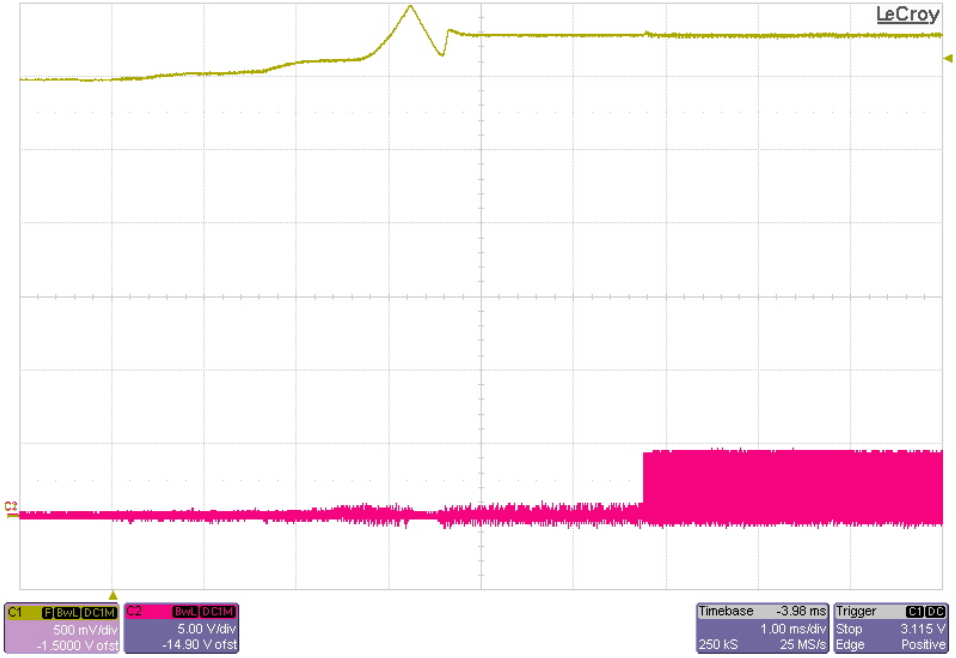
4.4 36V Input, 1 Ohm Load, 2V Pre-bias



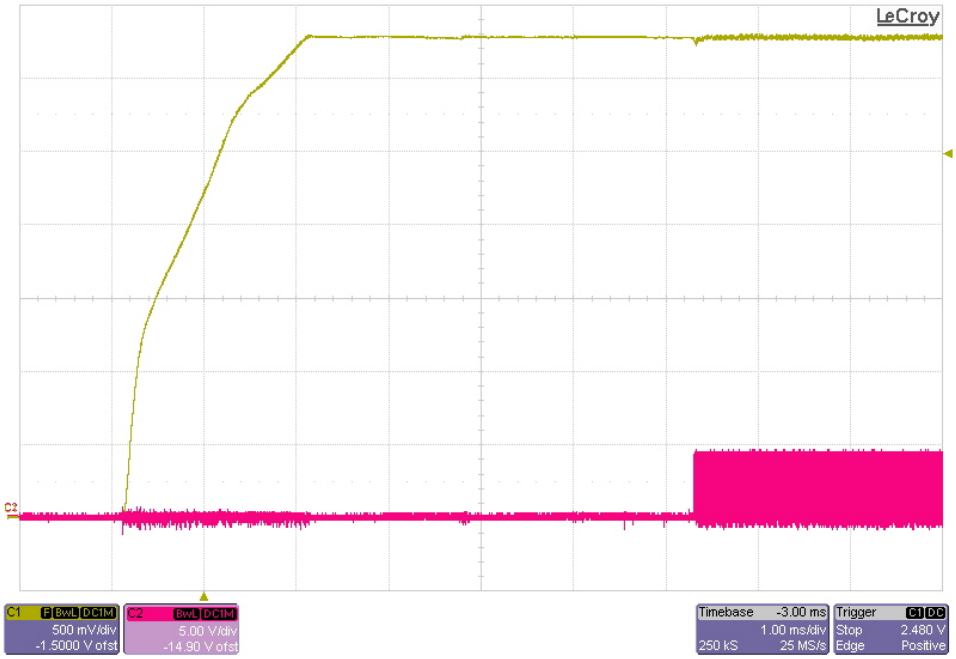
4.5 36V Input, No Load, 3V Pre-bias



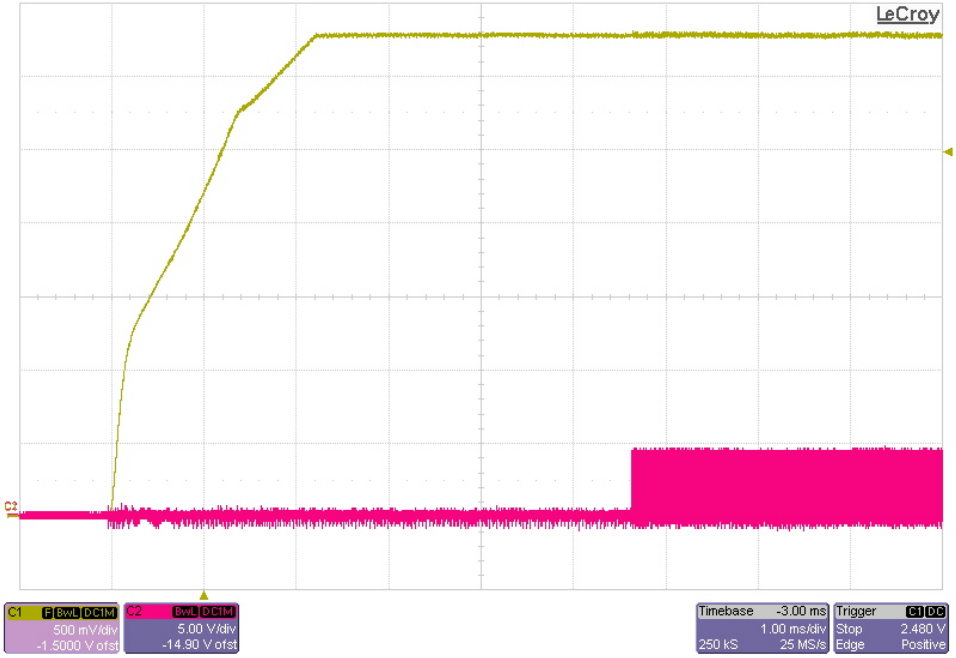
4.6 36V Input, 1 Ohm Load, 3V Pre-bias



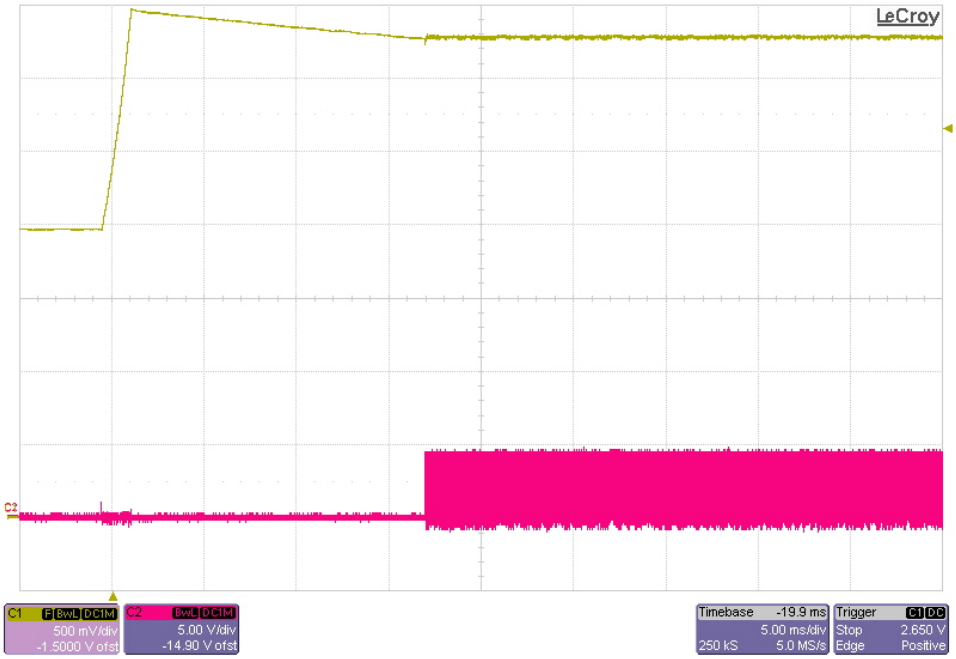
4.7 75V Input, No Load, No Pre-bias



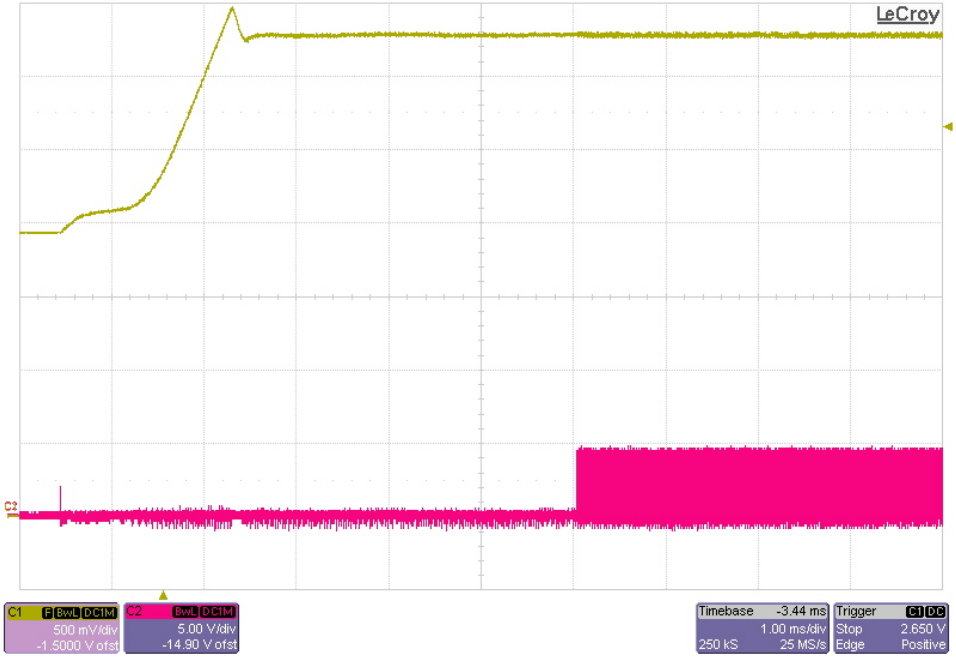
4.8 75V Input, 1 Ohm Load, No Pre-bias



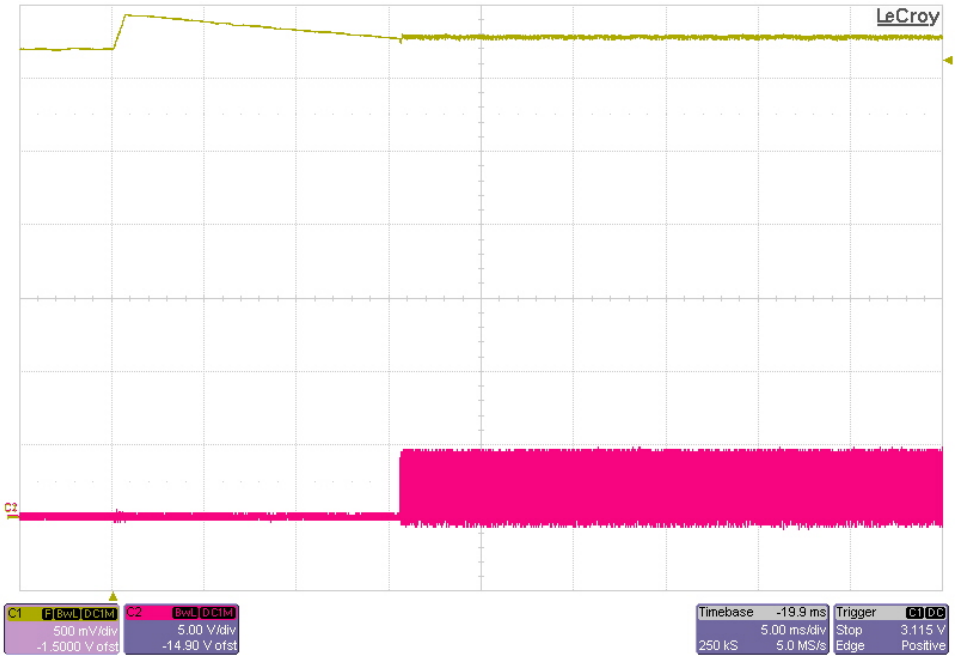
4.9 75V Input, No Load, 2V Pre-bias



4.10 75V Input, 1 Ohm Load, 2V Pre-bias



4.11 75V Input, No Load, 3V Pre-bias

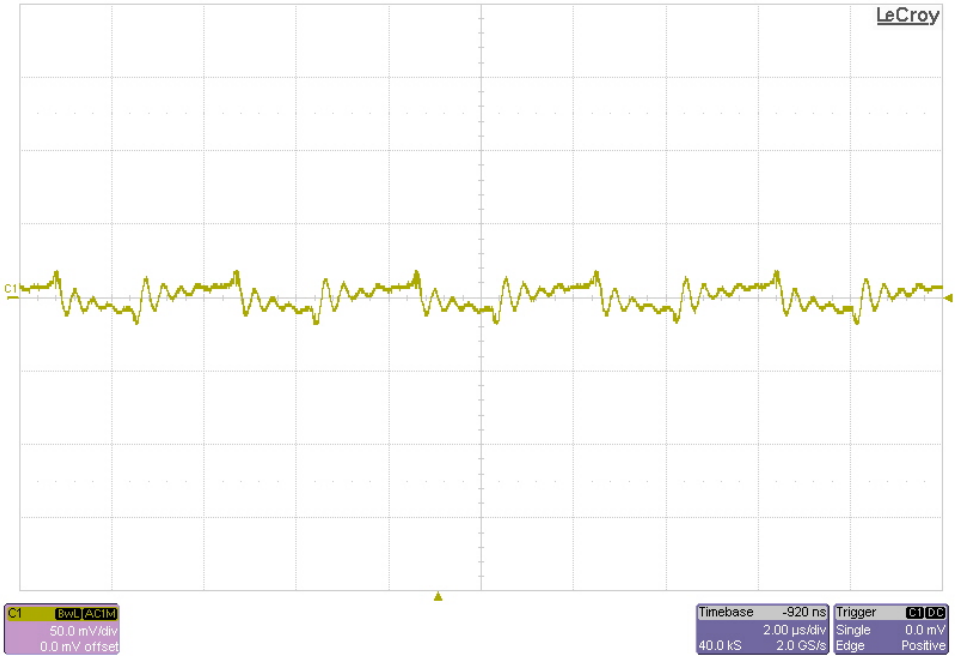


4.12 75V Input, 1 Ohm Load, 3V Pre-bias

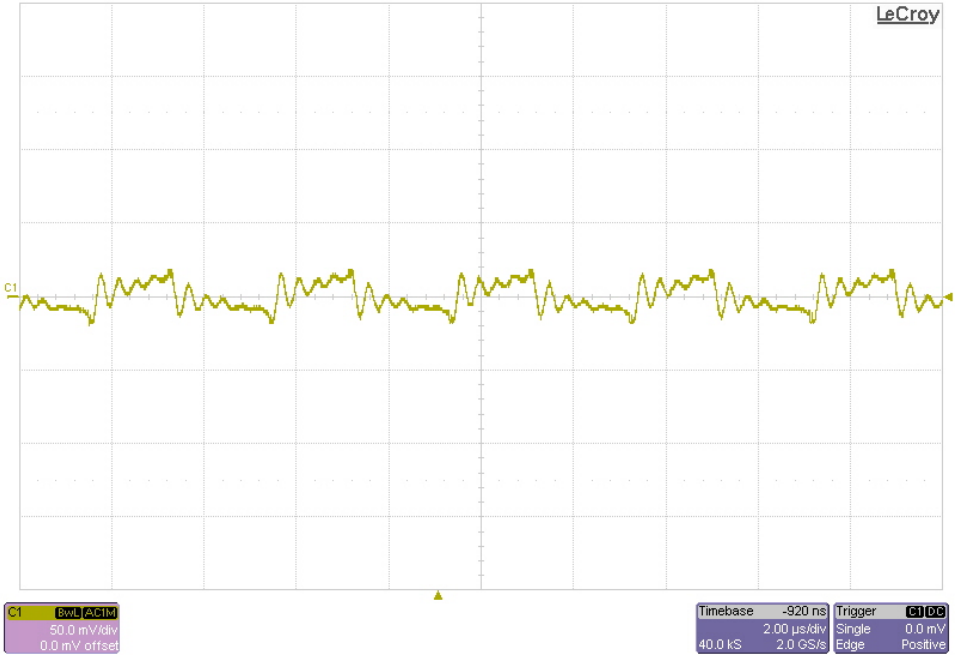
5 Output Ripple Voltage

The output ripple voltage during full load operation (30A load) is shown in the images below.

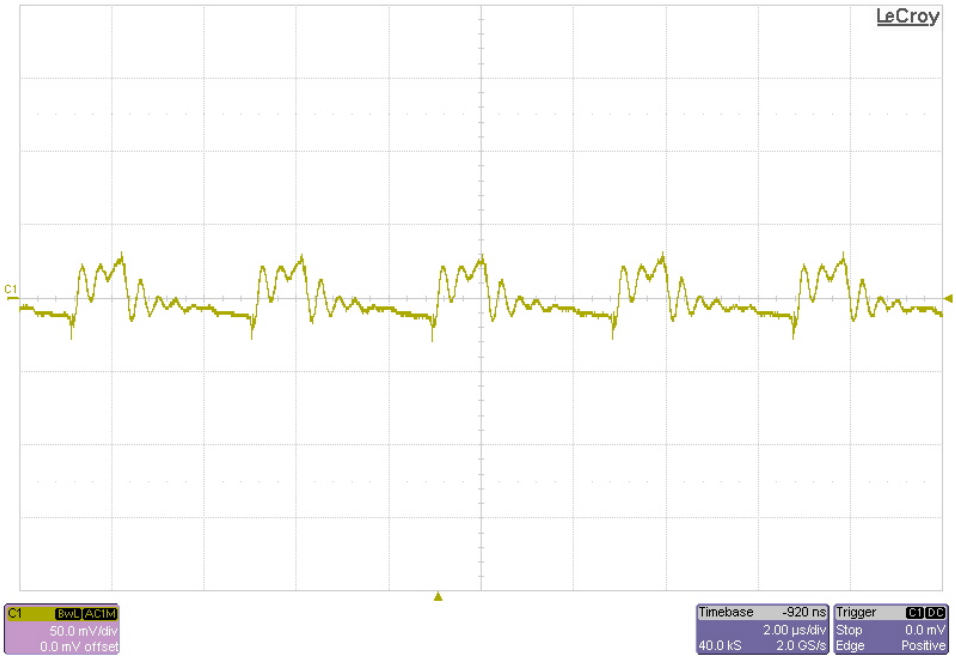
5.1 36V Input



5.2 48V Input

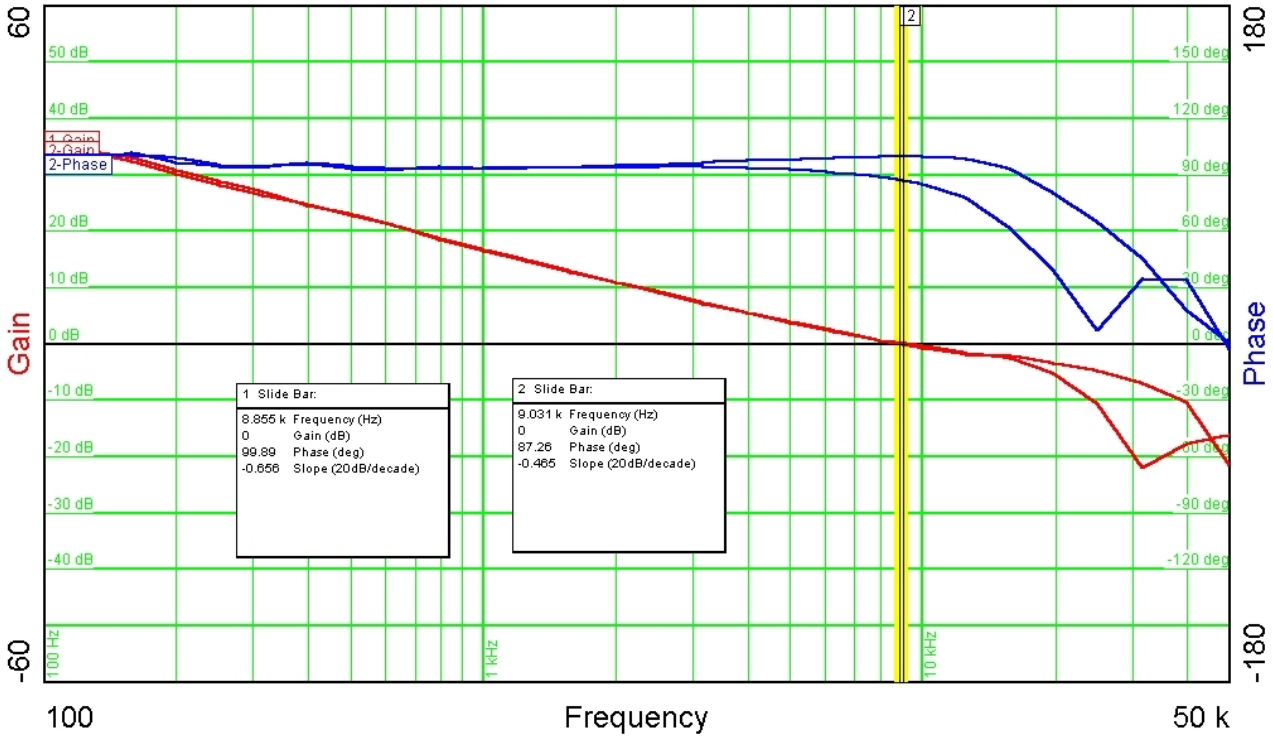


5.3 75V Input



6 Loop Response

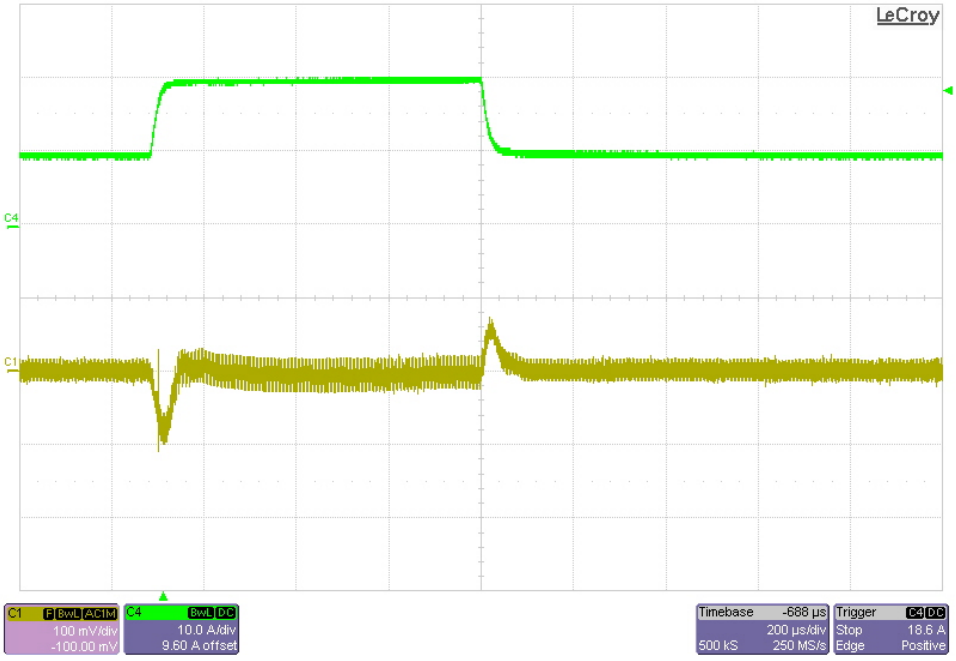
The image below shows the loop response of the converter. For plot #1, the input was 36Vdc. For plot #2, the input was 75Vdc. The output was loaded with 30A.

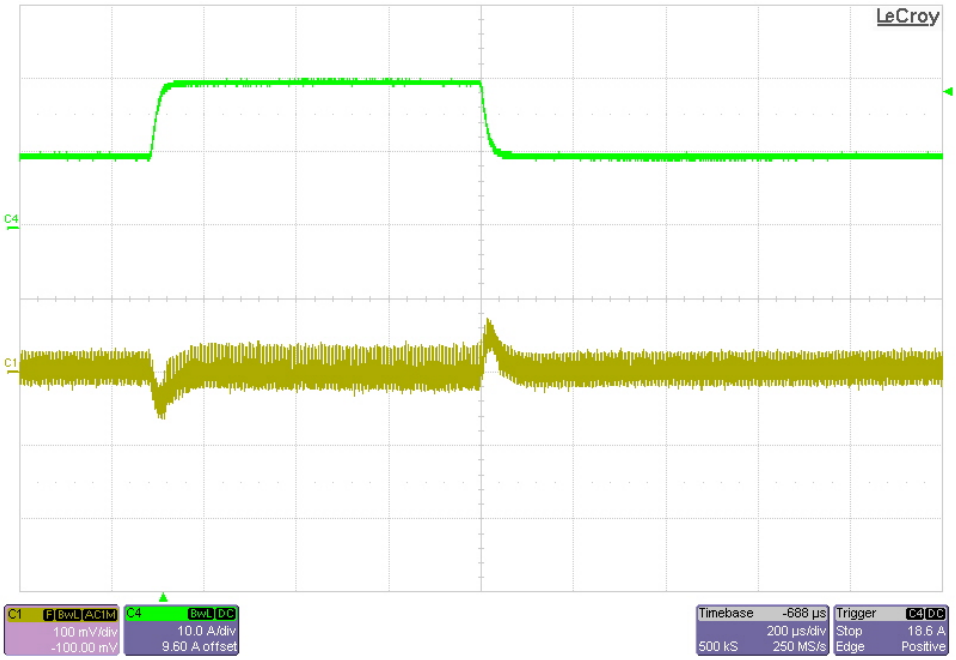


7 Load Transients

The images below show the response to a 10A to 20A load transient. For the top image, the input voltage was set to 36VDC. For the bottom image, the input voltage was set to 75VDC.

Channel 1: Vout (ac coupled) 100mV/div Channel 4: Iout 10A/div

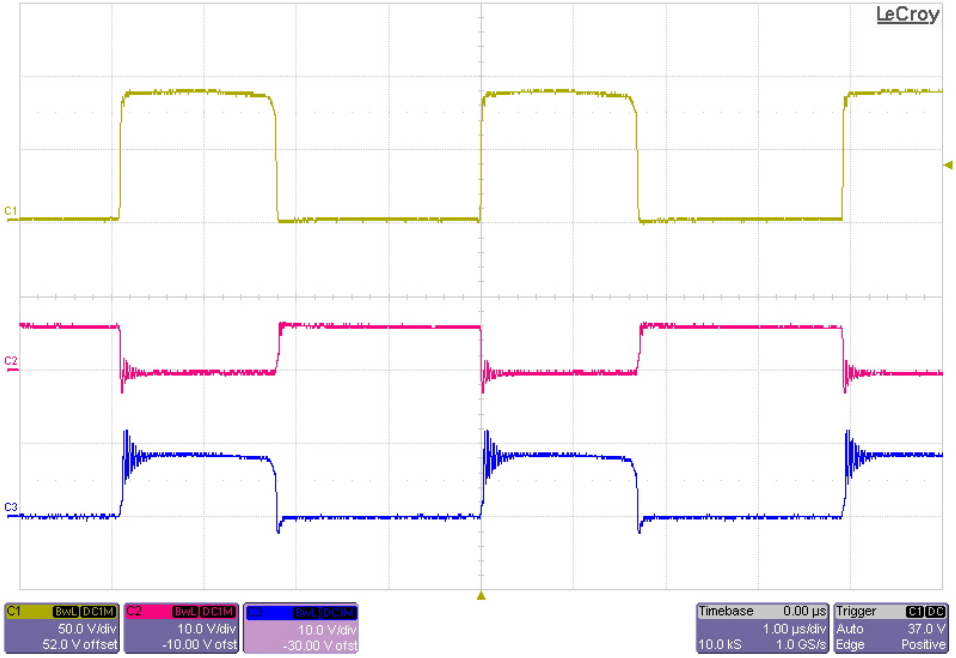


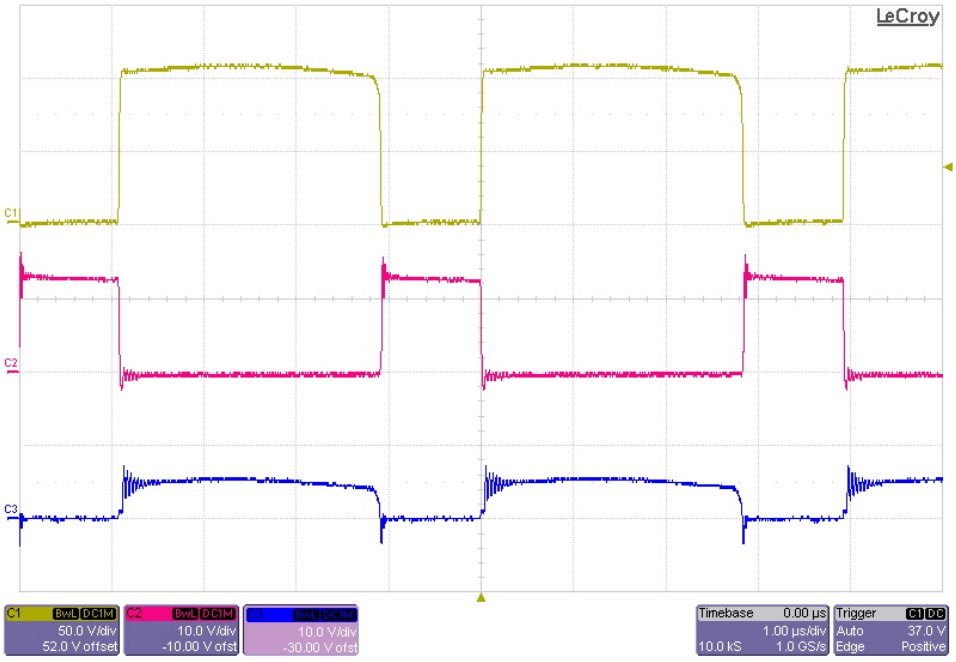


8 Switching Waveforms

The images below show the drain-to-source voltage waveforms on the switching MOSFETs. The output was loaded with 30A. For the top image, the input was set to 36V. For the bottom image, the input was set to 75V.

Channel 1: Q5 & Q6 Vds Channel 2: Q2 & Q3 Vds
Channel 3: Q8 & Q10 Vds




LeCroy
C1
C2
C3
C1 BwL DC1M
50.0 V/div
52.0 V offset
C2 BwL DC1M
10.0 V/div
-10.00 V ofst
C3 BwL DC1M
10.0 V/div
-30.00 V ofst
Timebase 0.00 µs
1.00 µs/div
10.0 kS 1.0 GS/s
Trigger C1 DC
Auto 37.0 V
Edge Positive

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