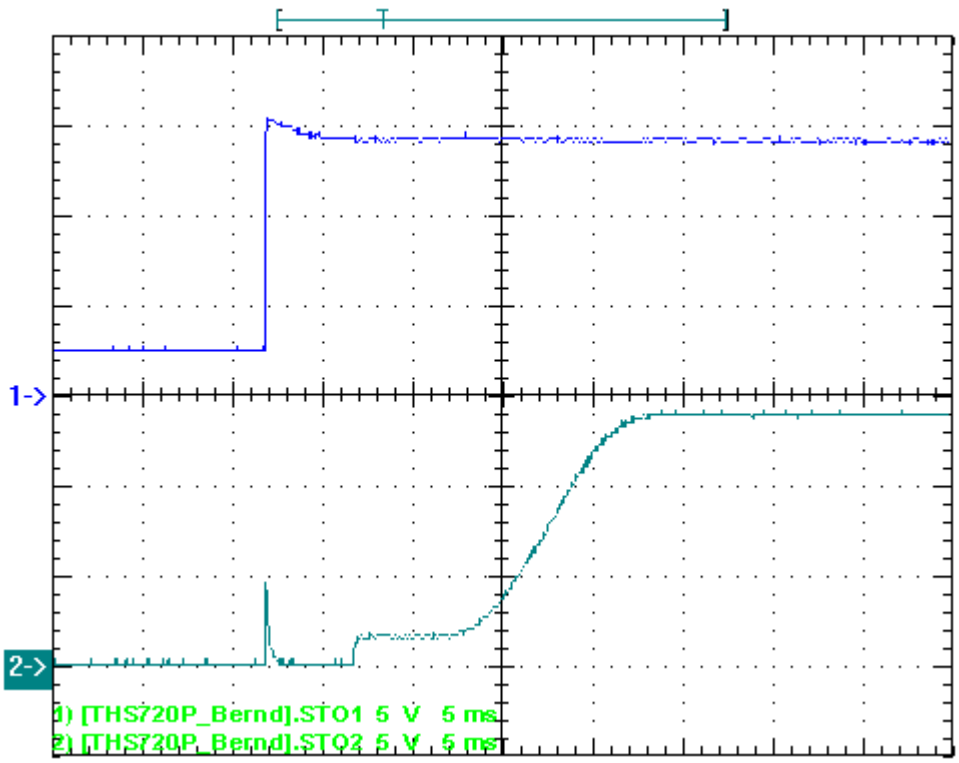
PMP4531RevB Test Results

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at ~14.4V, with resistive load on the output adjusted to get about 14.4V out.



Ch1=> input voltage 5V/div

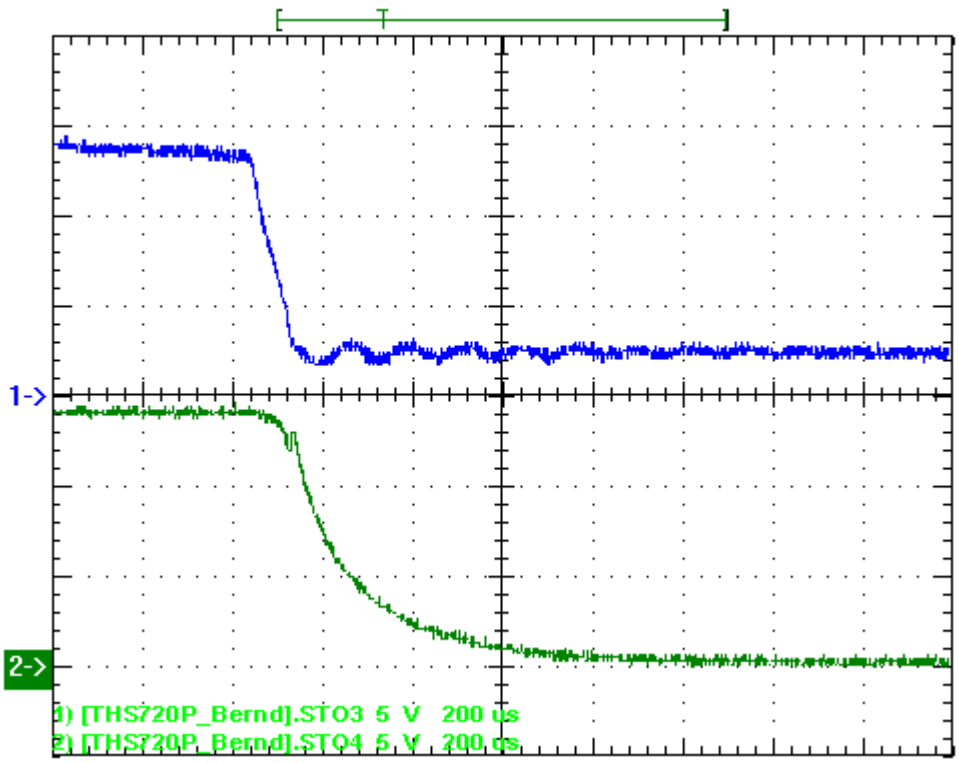
CH2=> output voltage 5V/div

5ms/div

Figure 1

2 Shutdown

The startup waveform is shown in the Figure 1. The input voltage was set at ~14.4V, with resistive load on the output adjusted to get about 14.4V out..



Ch1=> input voltage 5V/div

CH2=> output voltage 5V/div

200µs/div

Figure 2

3 Efficiency

The efficiency with varied input voltage is shown on Figure 3. Output voltage was adjusted to ~14.4V.

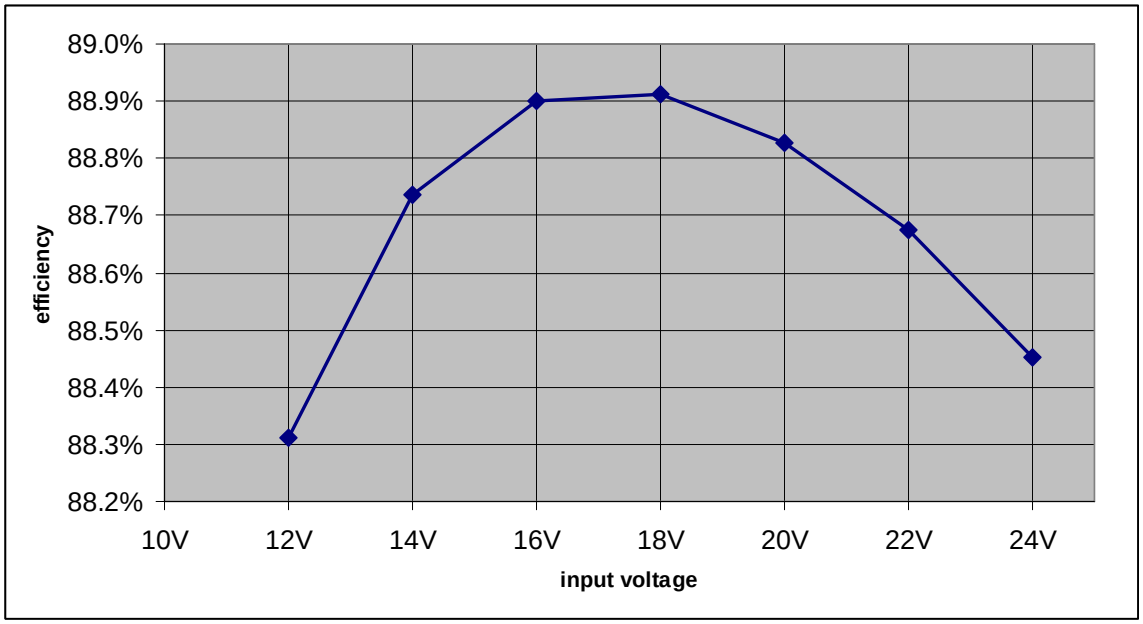


Figure 3

4 Line regulation

Figure 4 shows the output voltage dependency to the input voltage. Output voltage was adjusted to ~14.4V.

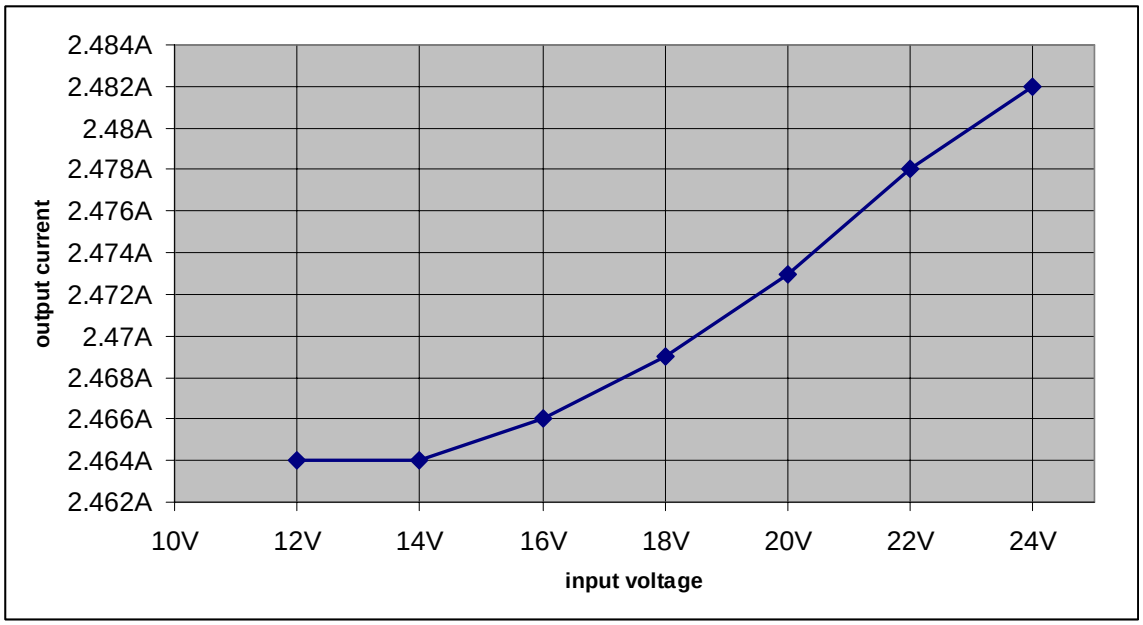
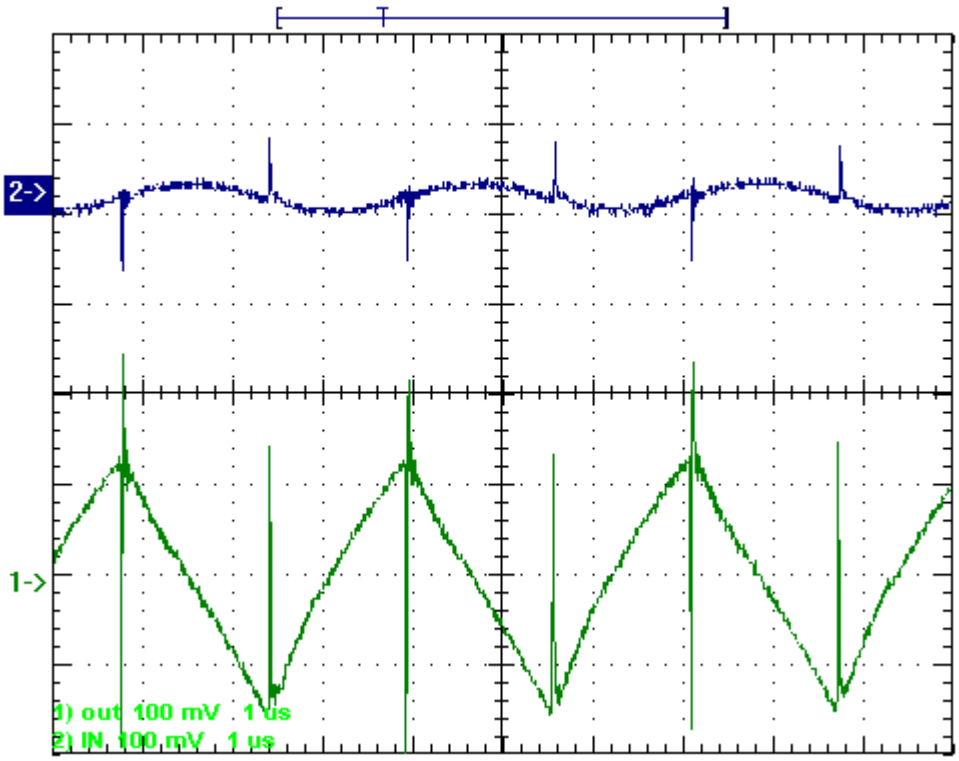


Figure 4

5 Ripple Voltage

The ripple voltage is shown in Figure 5. . Output voltage was adjusted to ~14.4V.



Ch2 =>input voltage 100mV/Div

Ch1 => output voltage 100mV/Div

20MHz bandwidth

1µs/div

curves captured separately with triggered to switch node

Figure 5

6 Control Loop Frequency Response

Figure 6 shows the loop response. The electronic load was switched to resistive mode.

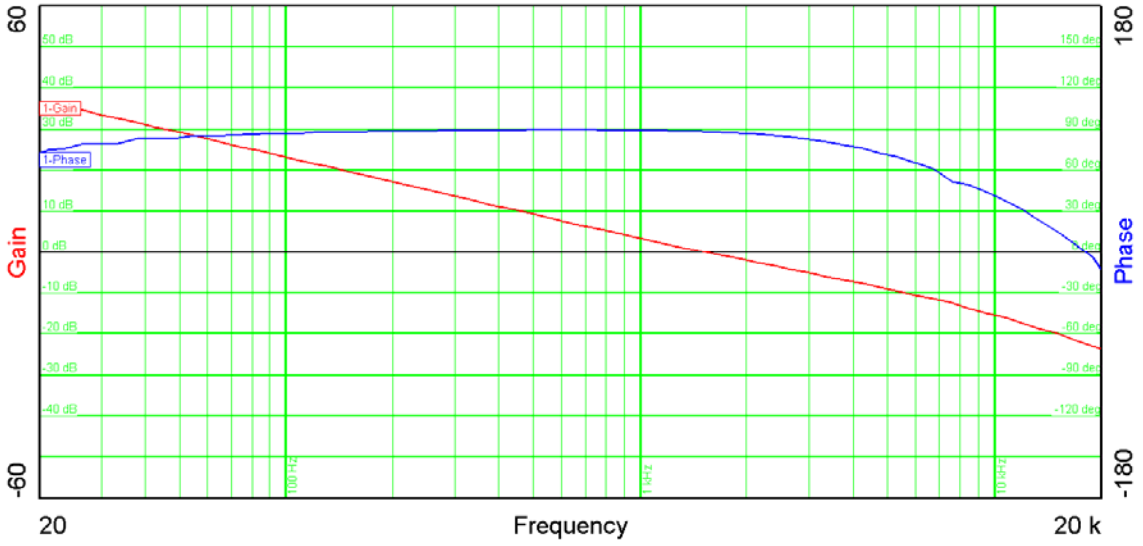


Figure 6

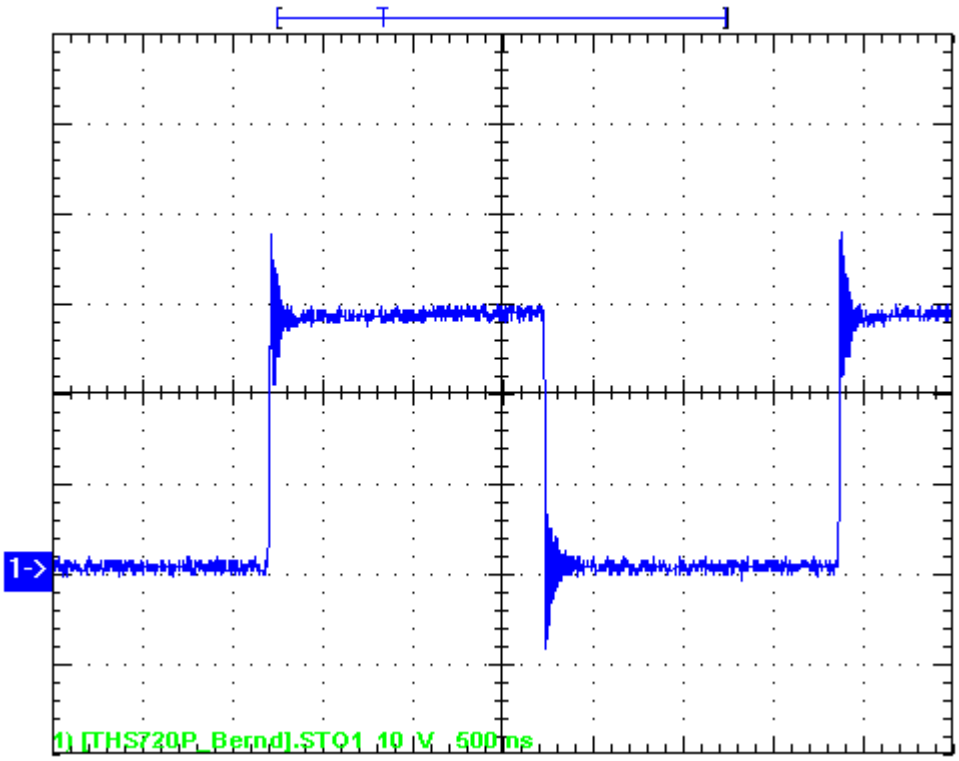
Table 1 summarizes the results from Figure 6

Bandwidth (kHz)	1.52
Phase margin	88.2°
slope (20dB/decade)	-0.916
gain margin (dB)	-22.27°
slope (20dB/decade)	-1.63
freq (kHz)	18

Table 1

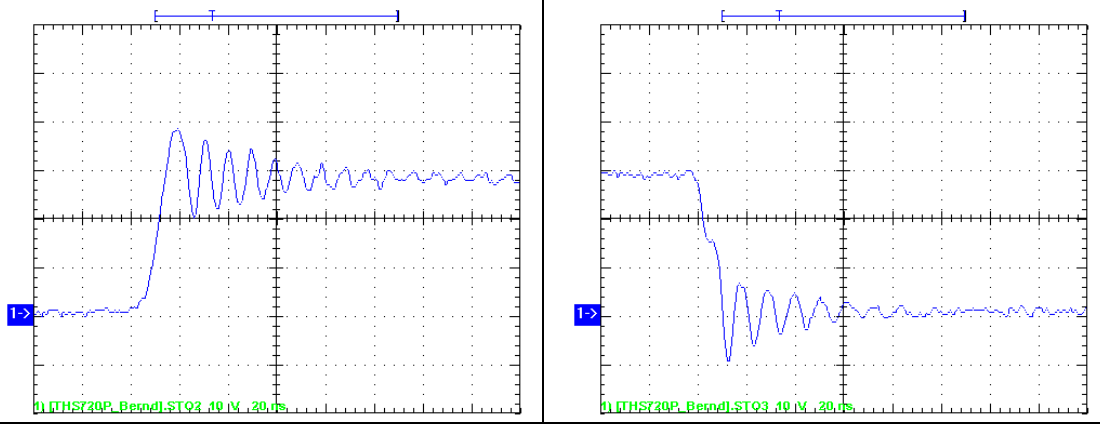
7 Switch Node Waveform

With a load of 1A results in the waveforms shown in Figure 7 and Figure 8. 14.4V were applied to the input. The output were adjusted to about 14.4V.



Ch3 => SW
10V/div
500ns/div
full bandwidth

Figure 7



Ch1/2 => 10V/div
20ns/div
full bandwidth

Figure 8

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