1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 12V, with no load on the output.

Channel C1: **input voltage**
2V/div, 2ms/div

Channel C2: **output voltage**
2V/div, 2ms/div

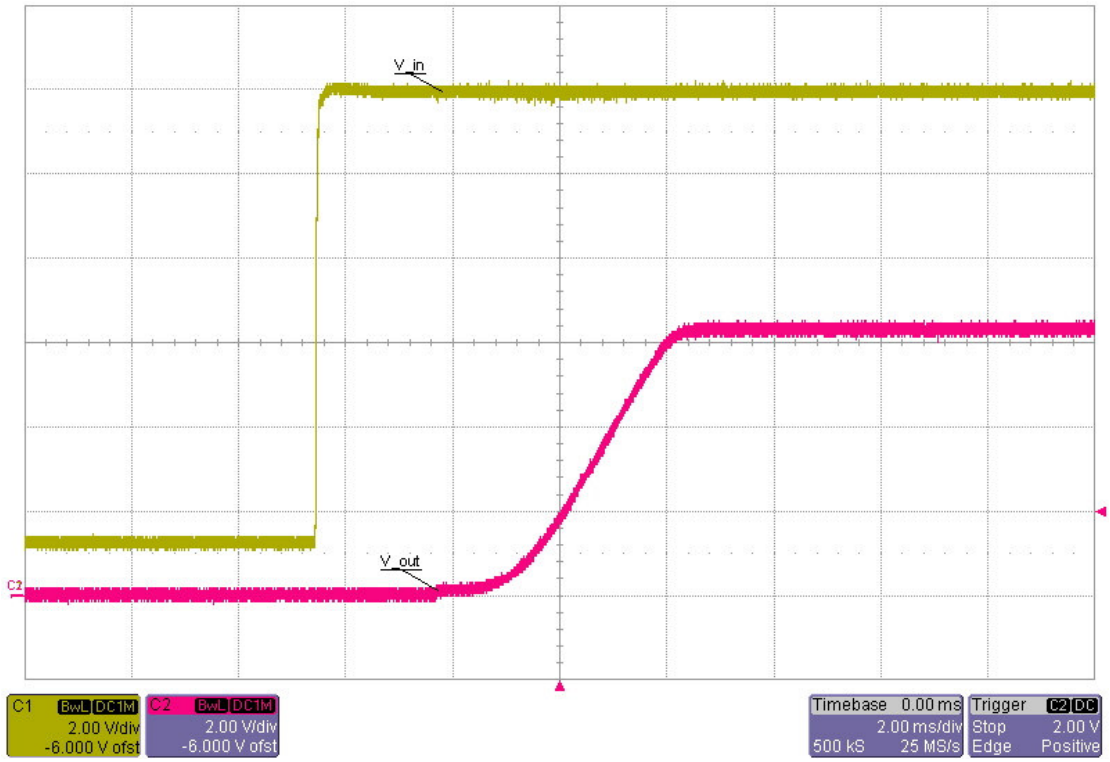

Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 12V with a 4.0A load on the output.

Channel C1: **input voltage**
2V/div, 500us/div

Channel C2: **output voltage**
2V/div, 500us/div

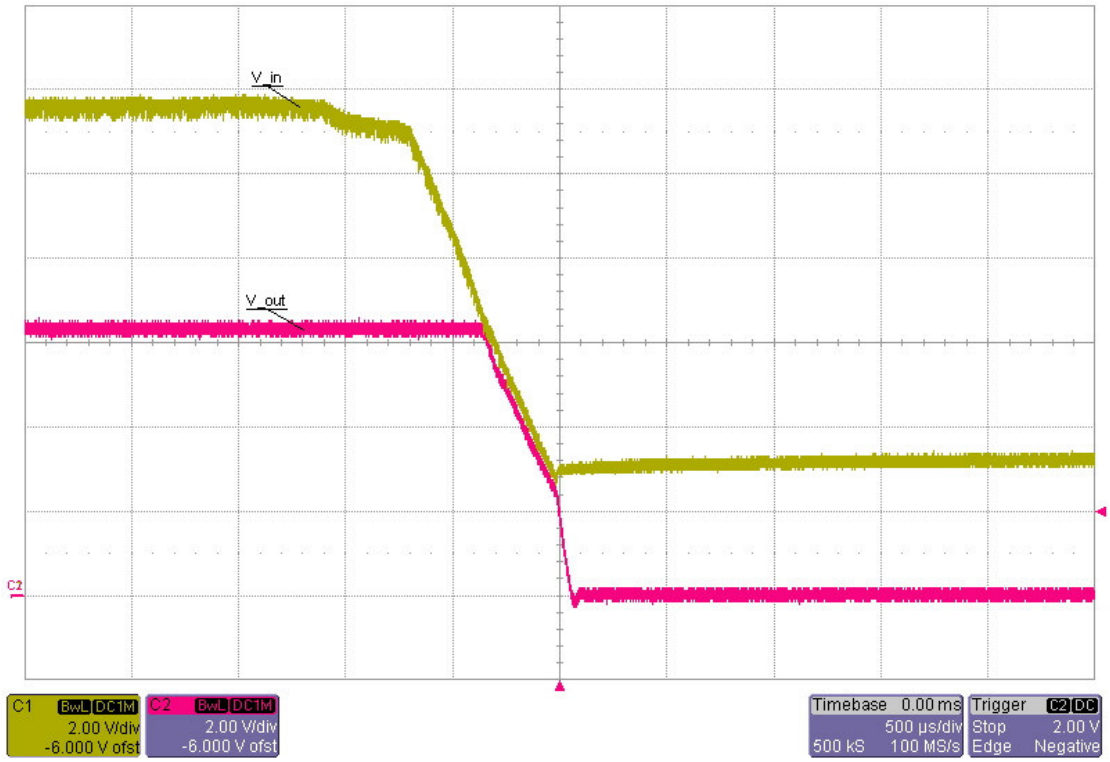

Figure 2

3 Efficiency

The efficiency is shown in Figure 3.

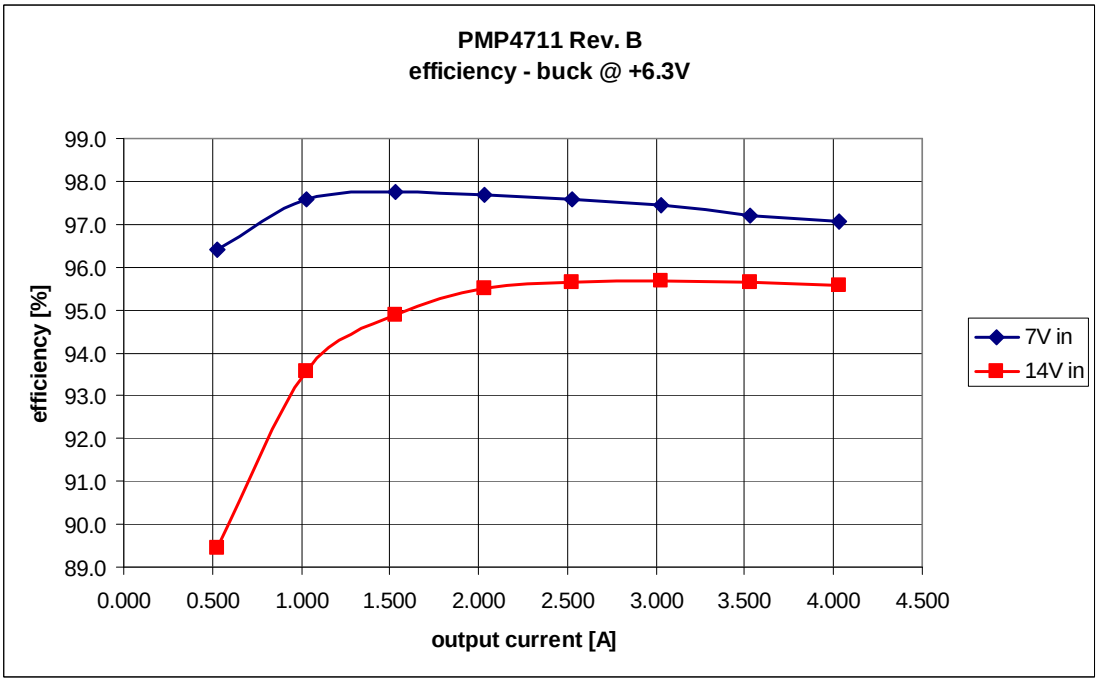

Figure 3

4 Load regulation

The load regulation of the 6.3V output is shown in Figure 4.

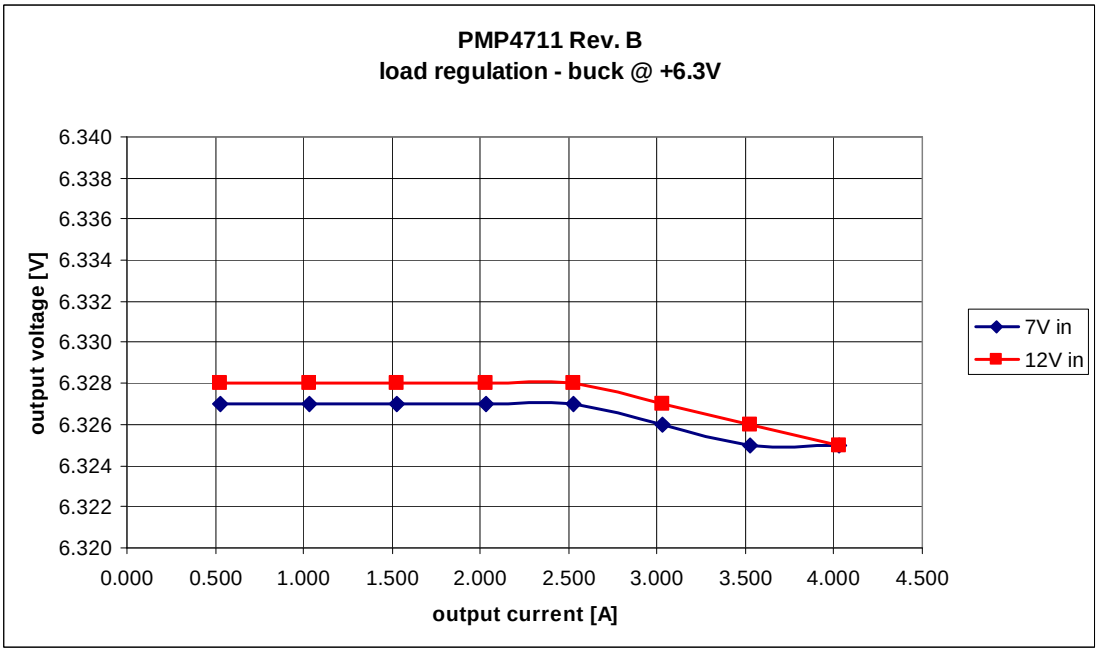

Figure 4

5 Output ripple voltage

The output ripple voltage at 4.0A load and 7.0V, 12.0V and 14.0V input voltage is shown in Figure 5.

Channel M1: **output voltage**, 13mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M1: **output voltage**, 11mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M3: **output voltage**, 10mV peak-peak
20mV/div, 5us/div, AC coupled

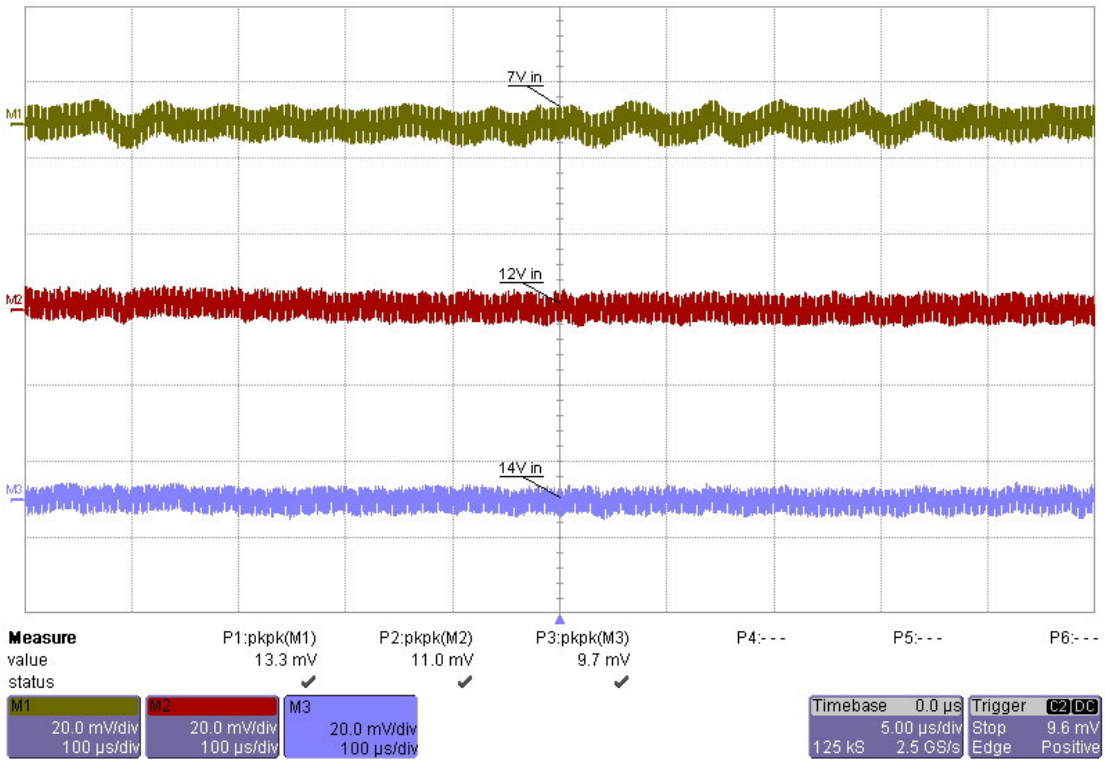

Figure 5

Due to the very low ESR of the ceramic output capacitors it is almost impossible to measure any ripple.
What you can see on the plot is mainly the noise picked up by the probe.

6 Load transients

The response to a load step and a load dump at an input voltage of 12.0V is shown in Figure 6 and Figure 7.

Channel C2: **output voltage**, -30mV undershoot, 20mV overshoot
50mV/div, 20us/div, AC coupled

Channel C1: **load current**, load step 2.0A to 4.0A
2A/div, 20us/div

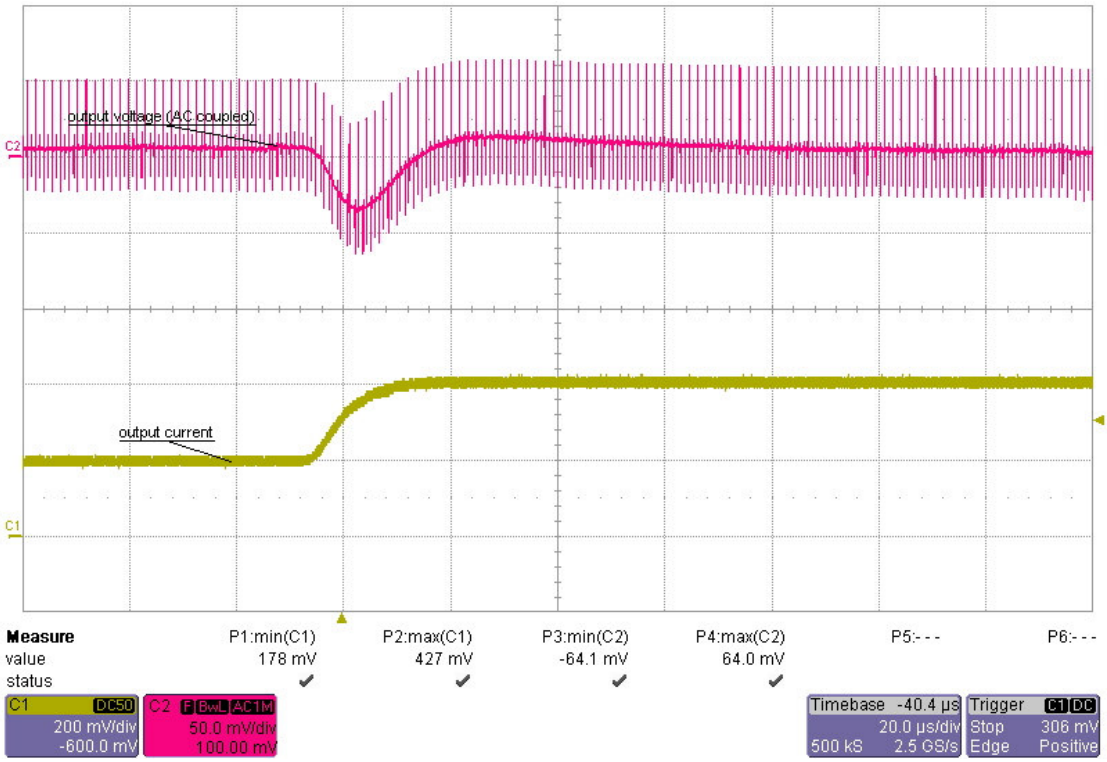

Figure 6

Channel C2: **output voltage**, 40mV overshoot, -10mV undershoot
50mV/div, 20us/div, AC coupled

Channel C1: **load current**, load dump 4.0A to 2.0A
2A/div, 20us/div

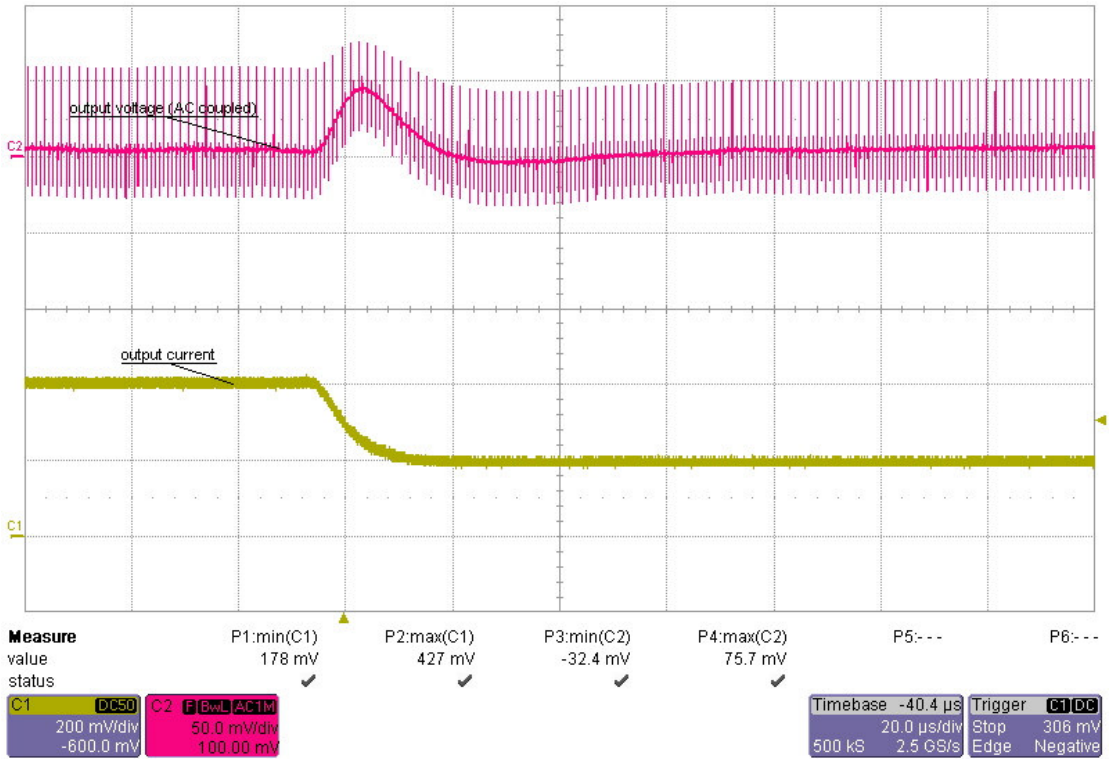

Figure 7

7 Frequency response

Figure 8 shows the loop response of the 6.3V output with 12.0V input and a 4.0A load.

59 deg phase margin @ crossover frequency 86.5 kHz

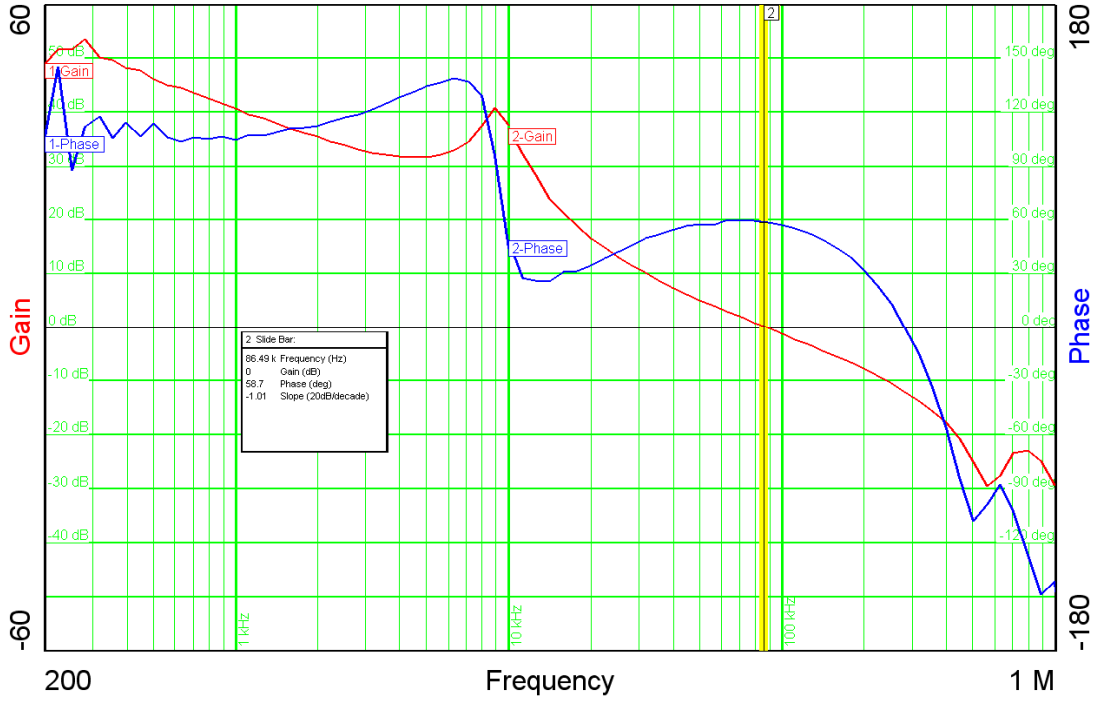

Figure 8

8 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 9. The image was captured with a 14V input and a 4.0A load.

Channel C2: **drain-source voltage**, -1.5V minimum voltage, 19.3V maximum voltage
5V/div, 500ns/div

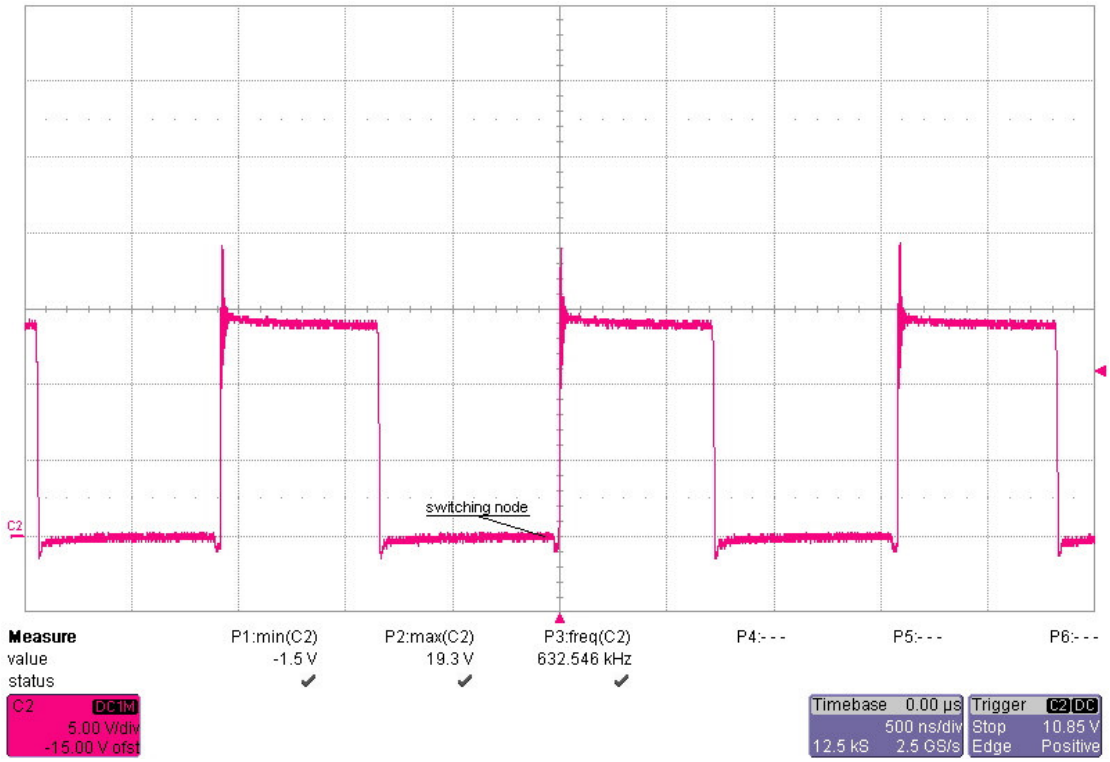

Figure 9

9 Thermal measurement

The thermal image (Figure 10) shows the circuit at an ambient temperature of 21 °C with an input voltage of 14.0V and a load of 4.0A (worst case).

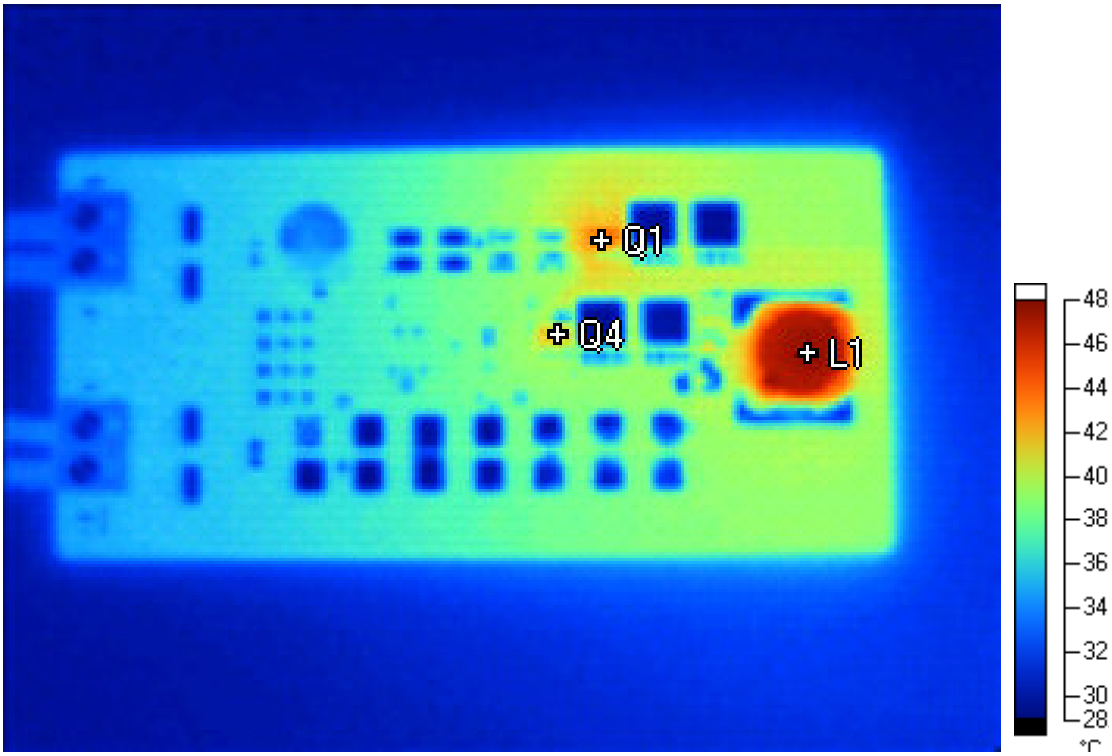

Figure 10

device	max. temperature	measured temp. @ 25 °C
Q1 – CSD16409Q3	150 °C	43.6 °C
Q4 – CSD16409Q3	150 °C	41.7 °C
L1 – MSS1260-682MLD	85 °C	47.7 °C

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