1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 15.0V, with no load on the two outputs.

Channel C1: **input voltage**
5V/div, 5ms/div

Channel C2: **output voltage, +23.0V**
10V/div, 5ms/div

Channel C3: **output voltage, -23.0V**
10V/div, 5ms/div

Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 15.0V with a 0.1A load on each output.

Channel C1: **input voltage**
5V/div, 20ms/div

Channel C2: **output voltage, +23.0V**
10V/div, 20ms/div

Channel C3: **output voltage, -23.0V**
10V/div, 20ms/div

Figure 2

3 Efficiency

The efficiency is shown in Figure 3.

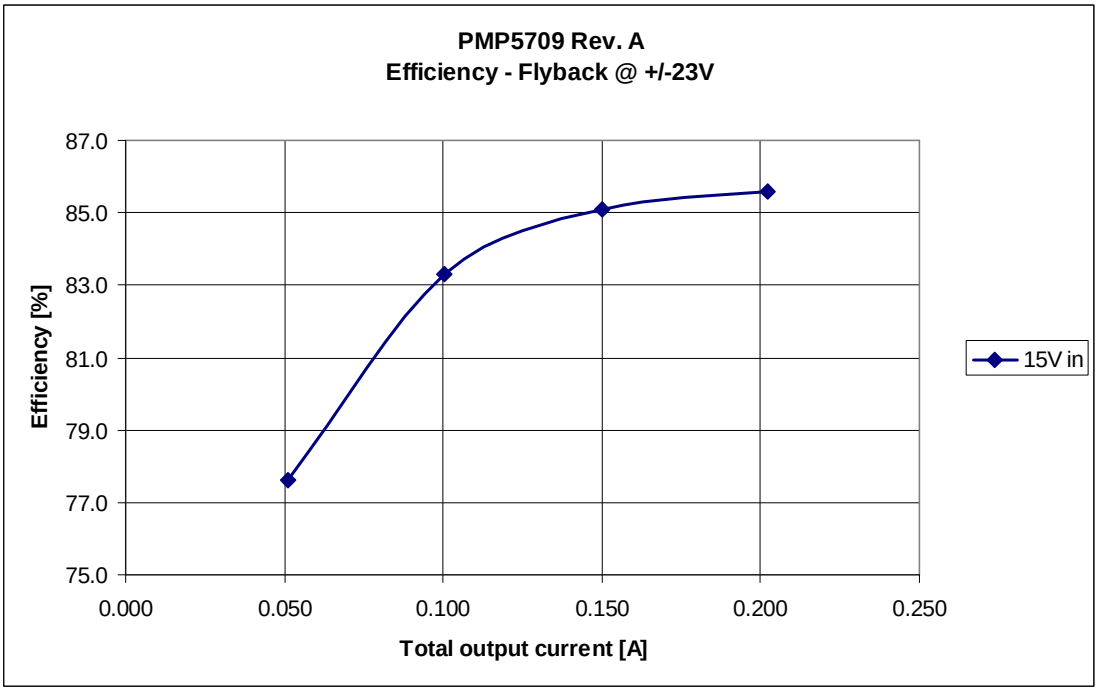

Figure 3

4 Load regulation

The load regulation of the two outputs is shown in Figure 4.
The negative output is shown as a positive voltage (multiplied by -1).

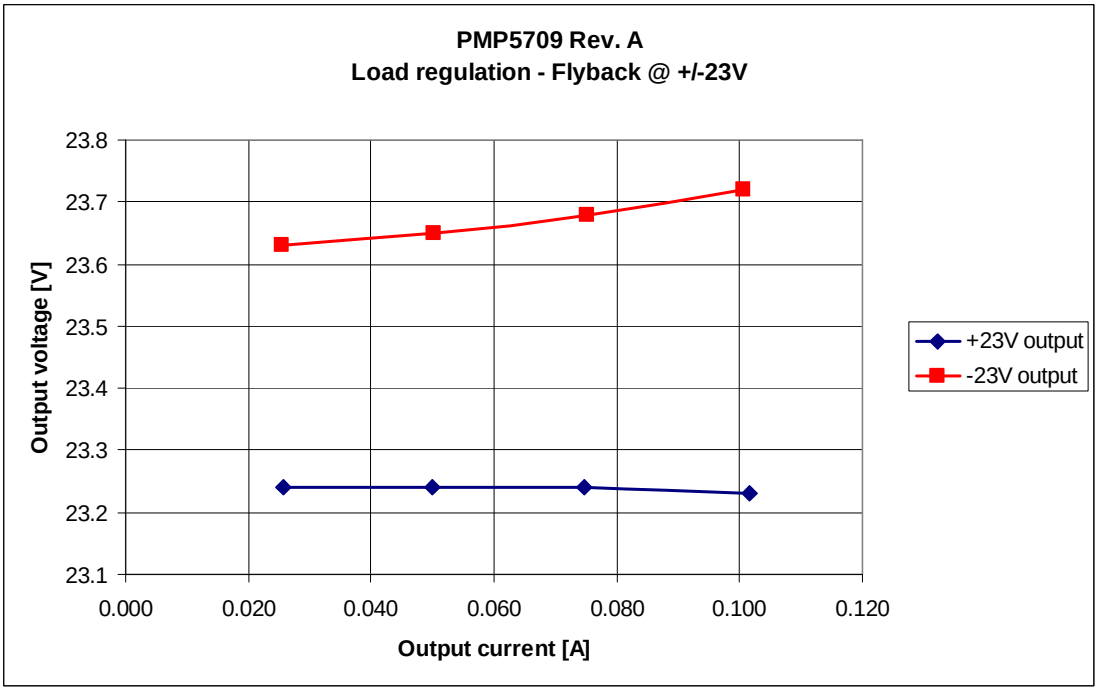

Figure 4

5 Output ripple voltage

The output ripple voltage at 0.1A load on each output is shown in Figure 5.

Channel M1: **output voltage of +23V rail, 130mV peak-peak**
50mV/div, 5us/div, AC coupled

Channel M2: **output voltage of -23V rail, 365mV peak-peak**
100mV/div, 5us/div, AC coupled

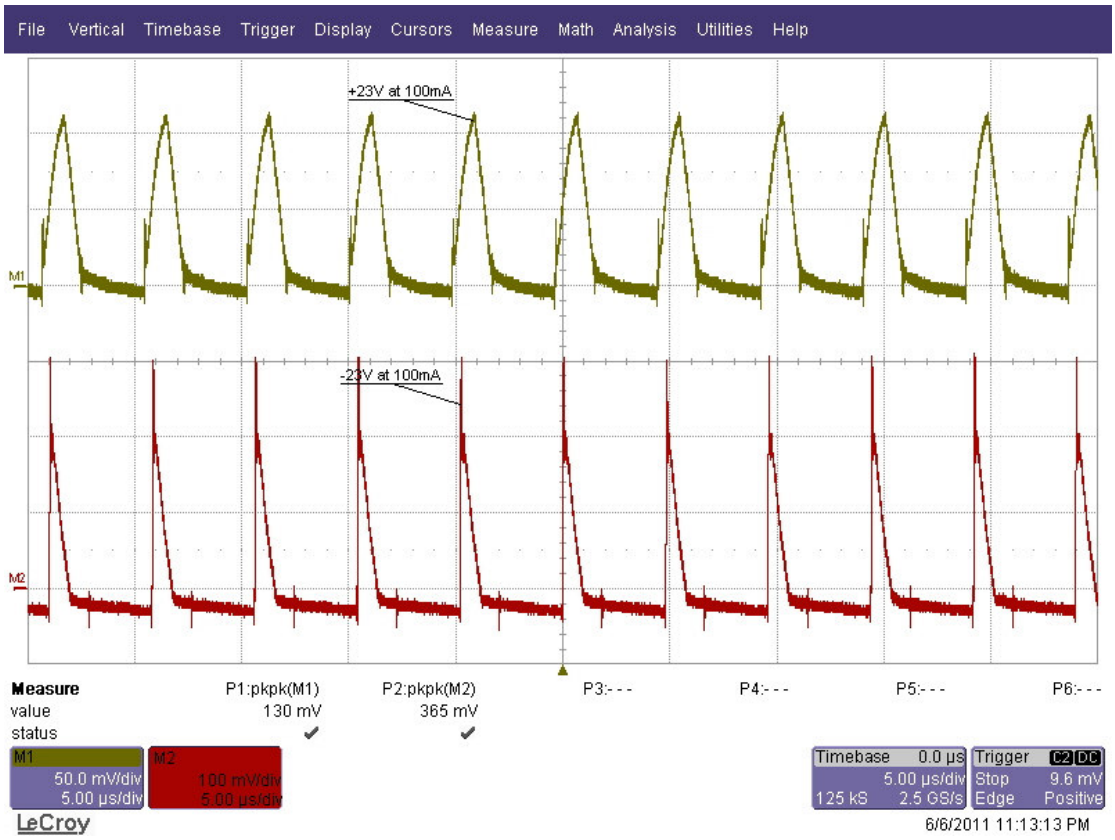

Figure 5

6 Load transients

The response to a load step and a load dump at an input voltage of 15.0V is shown in Figure 6.

Channel C2: **output voltage**, -146mV undershoot, 136mV overshoot
100mV/div, 10ms/div, AC coupled

Channel C1: **load current**, load step 0.0A to 0.1A
100mA/div, 10ms/div

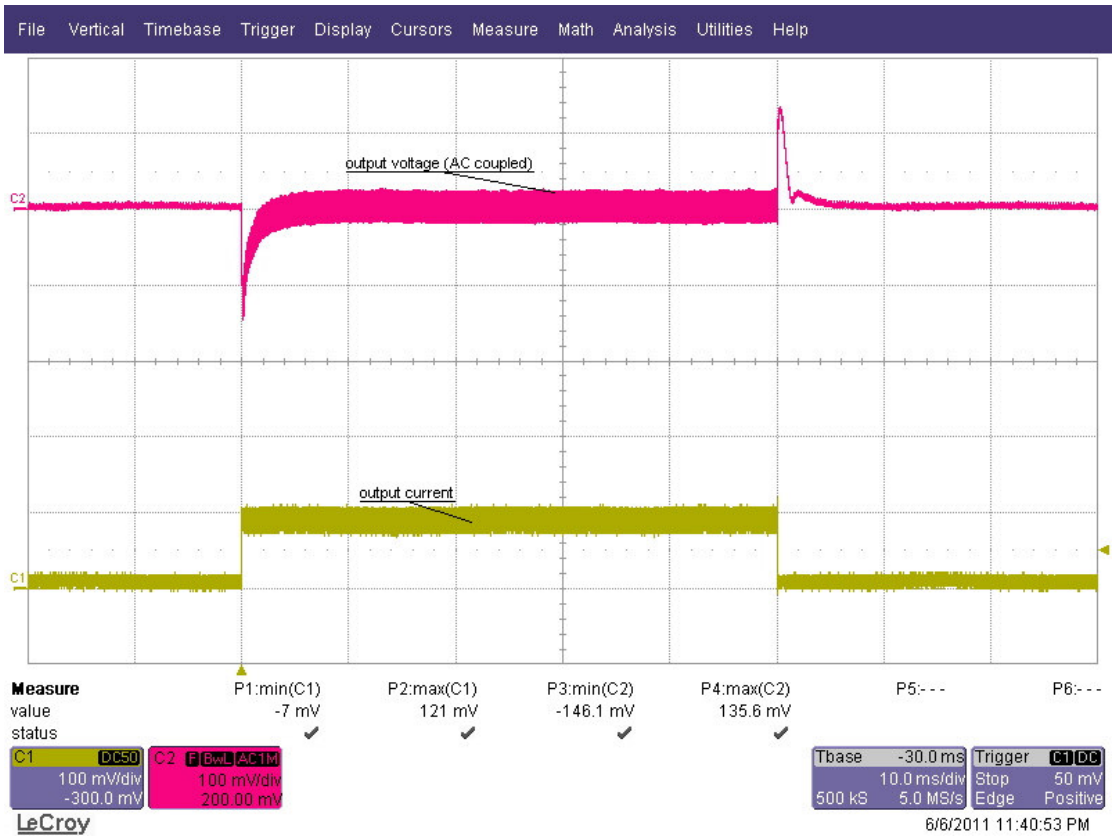

Figure 6

Frequency response

Figure 7 shows the loop response with a 100mA load on each output.

92 deg phase margin @ crossover frequency 2.6 kHz

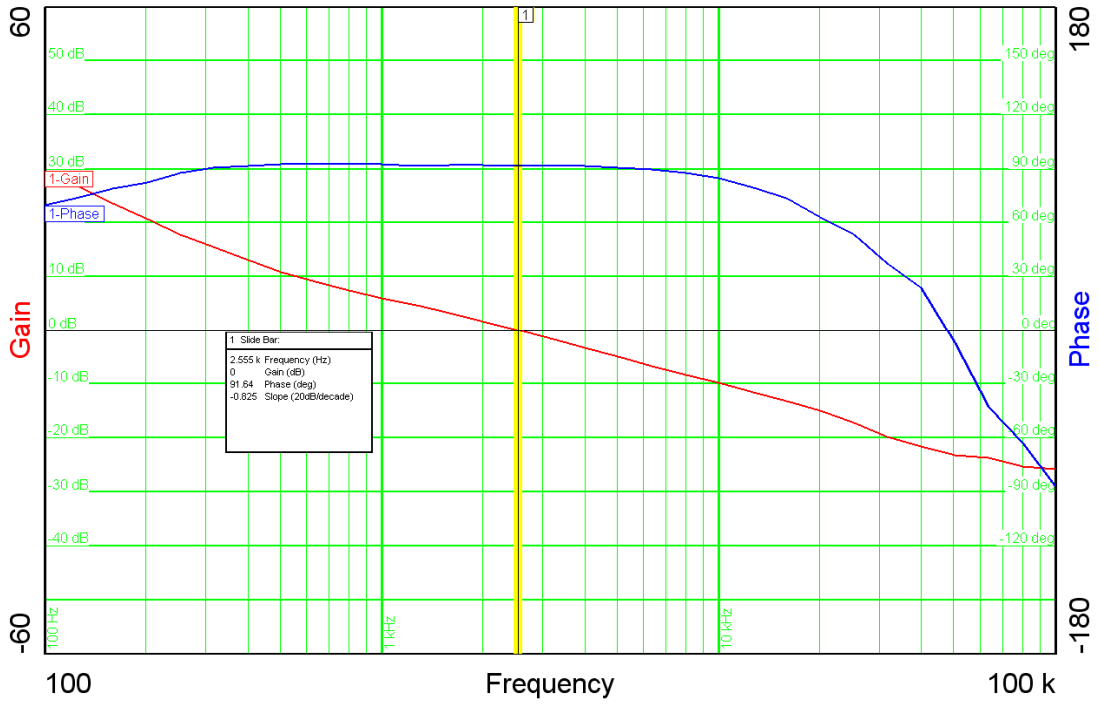

Figure 7

7 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 8. The image was captured with a 15.0V input and 0.1A load on each output.

Channel C2: **drain-source voltage**, -2.0V minimum voltage, 61.0V maximum voltage 10V/div, 2us/div

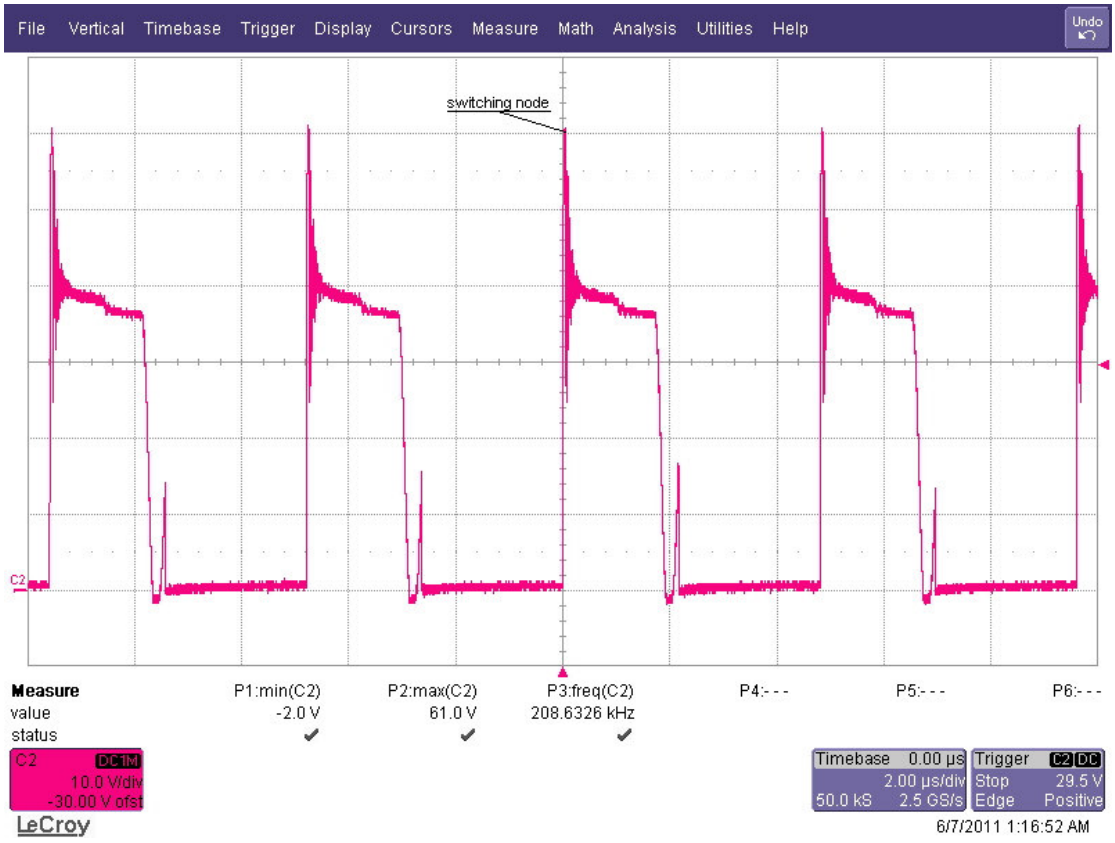

Figure 8

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