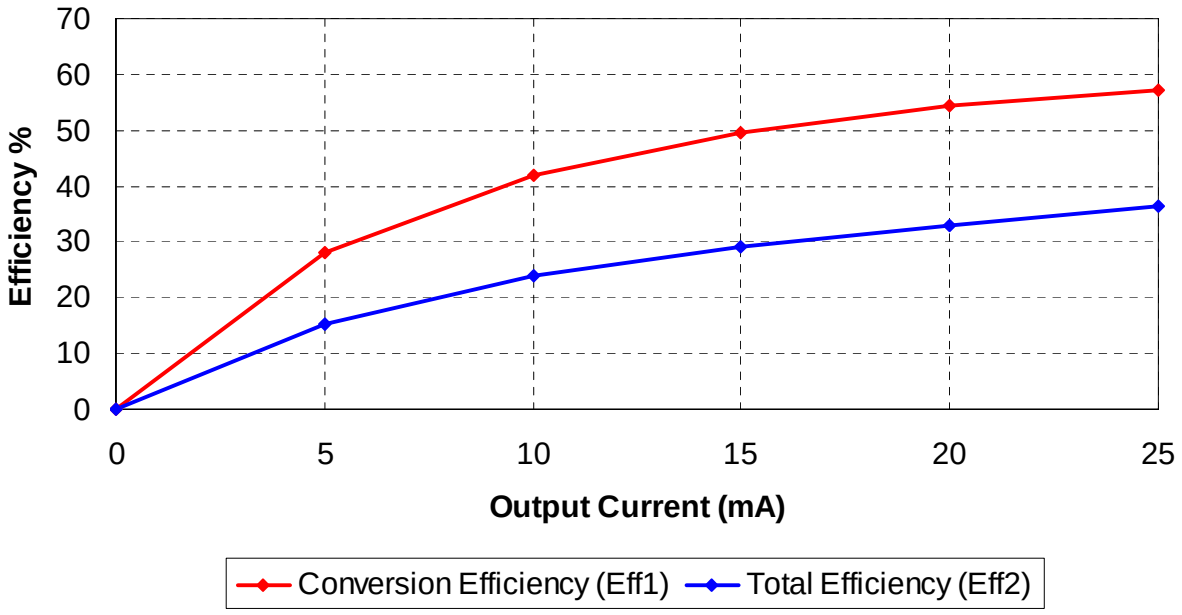
1 Conversion and Total Efficiency

The efficiency comprises two values:
Eff1 is the Conversion Efficiency: Input power in U3 (pin1) divided by USB output power
Eff2 is the Total Efficiency: Output power divided by USB output power

Two measurements were taken:
The first measurement was performed with no distance between the two PCBs.
In the second measurement a 0.5mm spacer was inserted between the two PCBs.

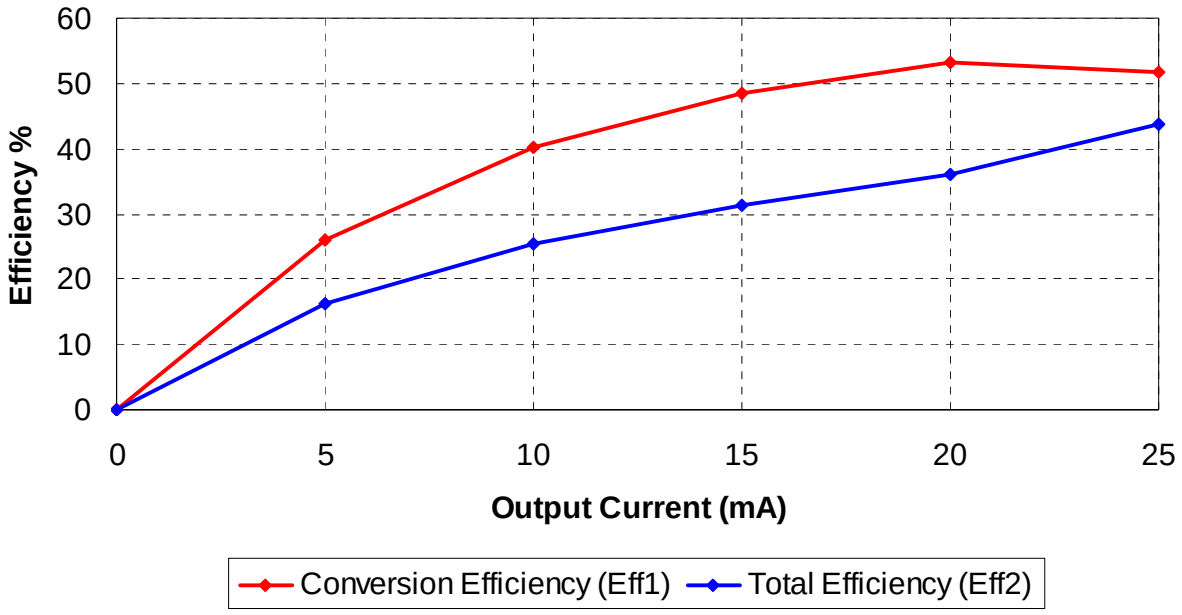
Efficiency table and graph without any spacer inserted between the two PCBs.

Iusb	Pin	Iout	VinU3	VoutU3	Pout1	Pout2	Eff1	Eff2
mA	mW	mA	Volt	Volt	mW	mW	%	%
26.0	130	0	10.40	5.519	0.0	0.0	0.0	0.0
36.1	180.5	5	10.14	5.519	50.7	27.6	28.1	15.3
46.4	232	10	9.73	5.518	97.3	55.2	41.9	23.8
56.8	284	15	9.41	5.516	141.2	82.7	49.7	29.1
66.7	333.5	20	9.07	5.515	181.5	110.3	54.4	33.1
75.6	378	25	8.67	5.513	216.8	137.8	57.3	36.5



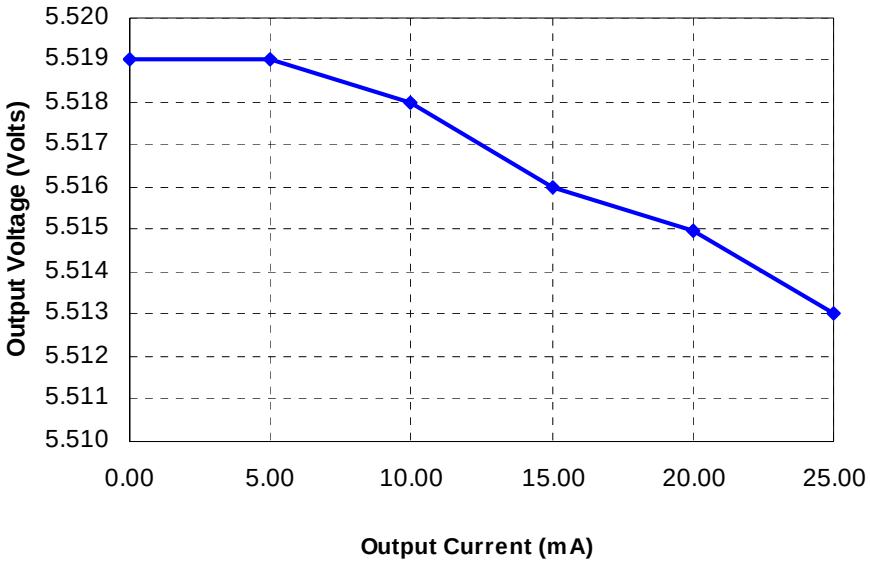
Efficiency table and graph with a 0.5mm spacer inserted between the two PCBs.

Iusb	Pin	Iout	VinU3	VoutU3	Pout1	Pout2	Eff1	Eff2
mA	mW	mA	Volt	Volt	mW	mW	%	%
25.2	126	0	10.47	5.519	0.0	0.0	0.0	0.0
34.1	170.5	5	8.89	5.519	44.5	27.6	26.1	16.2
43.4	217	10	8.72	5.517	87.2	55.2	40.2	25.4
52.7	263.5	15	8.51	5.516	127.7	82.7	48.4	31.4
61.3	306.5	20	8.14	5.514	162.8	110.3	53.1	36.0
63.2	316	25	6.53	5.513	163.3	137.8	51.7	43.6



2 Output Voltage Load Regulation

The output voltage variation with load is plotted below.



3 Output Ripple Voltage

The U3 input voltage ripple is shown in the plot below.
Load was set to 25mA
Channel 2: VinU3 (ac coupled) 50mV/div
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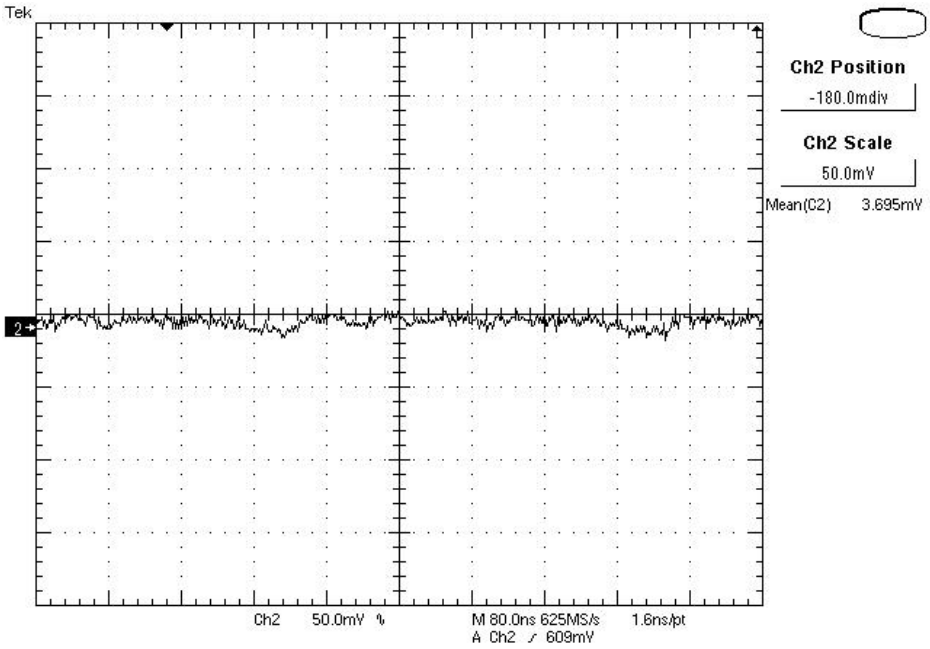
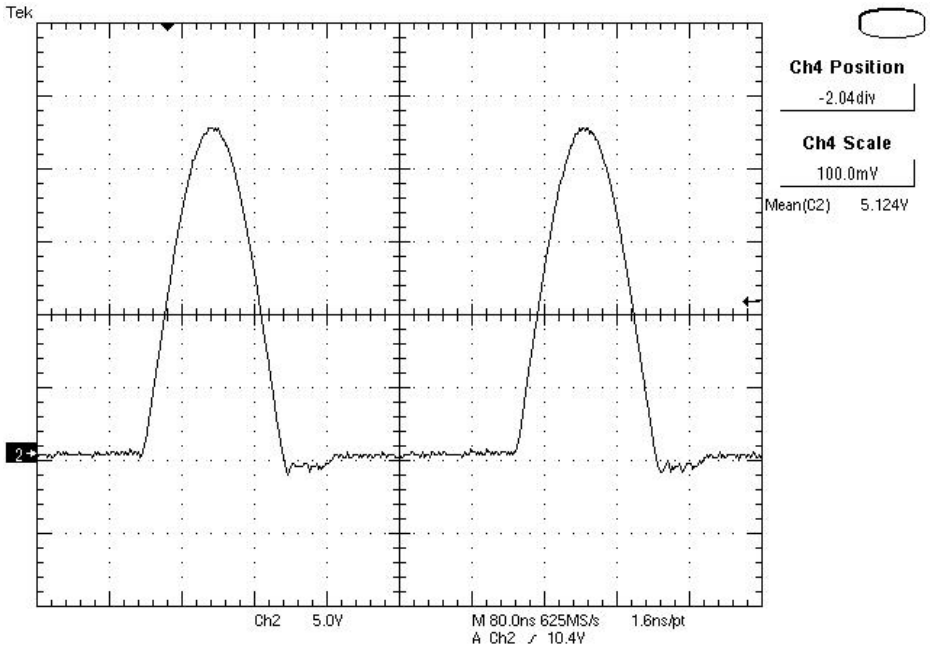
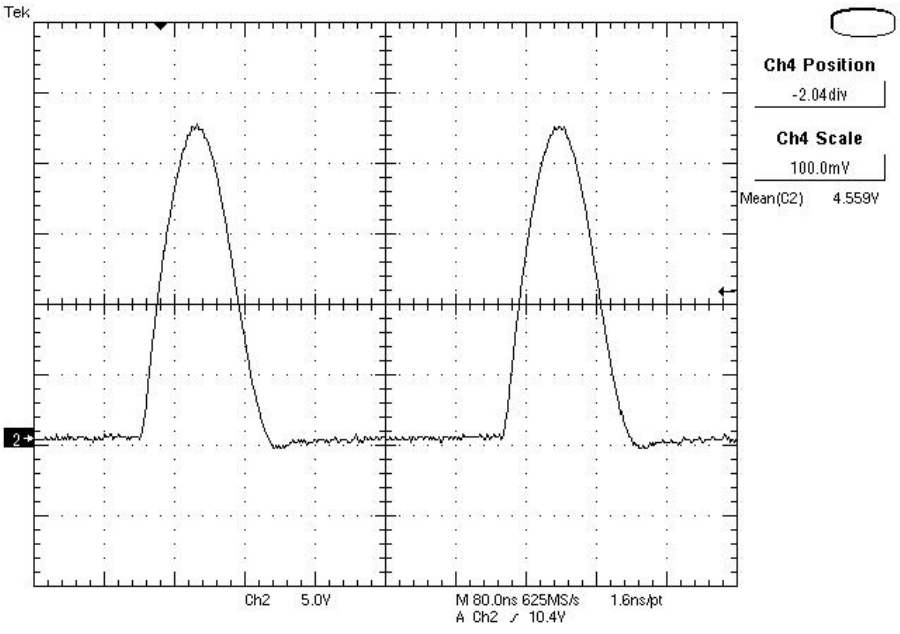


4 Q1 Drain Switching Waveform with No Load



5 Q1 Drain Switching Waveform with Full Load



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