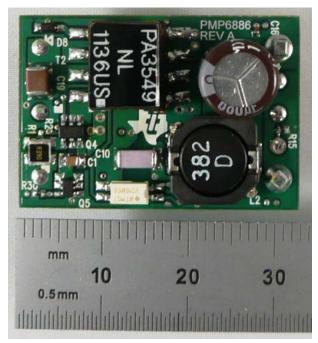


1 Photo

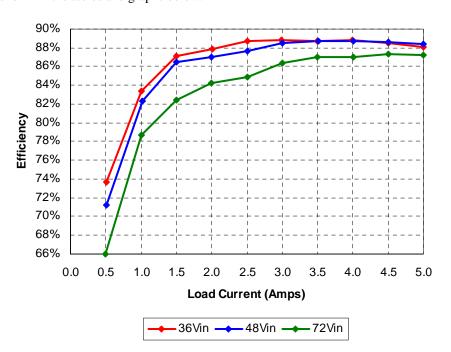
The photographs below show the top and bottom views of the PMP6886 Rev B demo board. The circuit is built on a PMP6886 Rev A PWB.





2 Efficiency

The efficiency data is shown in the tables and graphs below.





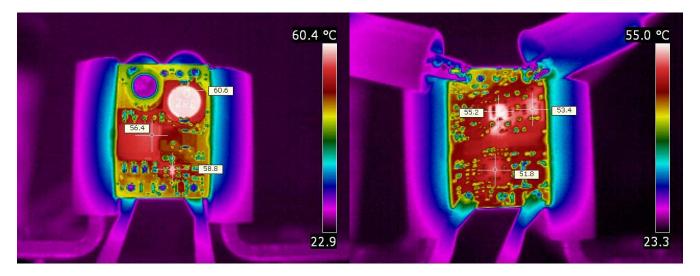
lout	Vout	Vin	lin	Pout	Losses	Efficiency
0.000	2.490	36.0	0.012	0.00	0.432	0.0%
0.511	2.490	36.0	0.048	1.27	0.456	73.6%
1.001	2.489	36.0	0.083	2.49	0.497	83.4%
1.499	2.489	36.0	0.119	3.73	0.553	87.1%
2.007	2.489	36.0	0.158	5.00	0.693	87.8%
2.502	2.488	36.0	0.195	6.22	0.795	88.7%
2.995	2.488	36.0	0.233	7.45	0.936	88.8%
3.504	2.488	36.0	0.273	8.72	1.110	88.7%
3.998	2.488	36.0	0.311	9.95	1.249	88.8%
4.498	2.487	36.0	0.351	11.19	1.449	88.5%
4.997	2.487	36.0	0.392	12.43	1.684	88.1%

lout	Vout	Vin	lin	Pout	Losses	Efficiency
0.000	2.490	48.0	0.011	0.00	0.528	0.0%
0.508	2.490	48.0	0.037	1.26	0.511	71.2%
1.016	2.489	48.0	0.064	2.53	0.543	82.3%
1.501	2.489	48.0	0.090	3.74	0.584	86.5%
1.998	2.489	48.0	0.119	4.97	0.739	87.1%
2.503	2.488	48.0	0.148	6.23	0.877	87.7%
3.004	2.488	48.0	0.176	7.47	0.974	88.5%
3.510	2.488	48.0	0.205	8.73	1.107	88.7%
4.005	2.488	48.0	0.234	9.96	1.268	88.7%
4.500	2.487	48.0	0.263	11.19	1.433	88.7%
5.002	2.487	48.0	0.293	12.44	1.624	88.5%

lout	Vout	Vin	lin	Pout	Losses	Efficiency
0.000	2.491	72.0	0.009	0.00	0.648	0.0%
0.496	2.490	72.0	0.026	1.24	0.637	66.0%
1.001	2.490	72.0	0.044	2.49	0.676	78.7%
1.501	2.490	72.0	0.063	3.74	0.799	82.4%
1.999	2.489	72.0	0.082	4.98	0.928	84.3%
2.505	2.489	72.0	0.102	6.23	1.109	84.9%
2.998	2.488	72.0	0.120	7.46	1.181	86.3%
3.502	2.488	72.0	0.139	8.71	1.295	87.1%
4.005	2.488	72.0	0.159	9.96	1.484	87.0%
4.502	2.487	72.0	0.178	11.20	1.620	87.4%
4.999	2.487	72.0	0.198	12.43	1.823	87.2%

3 Thermal Images

The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 25C with no forced air flow. The input was 48VDC, and the output was loaded with 5A.



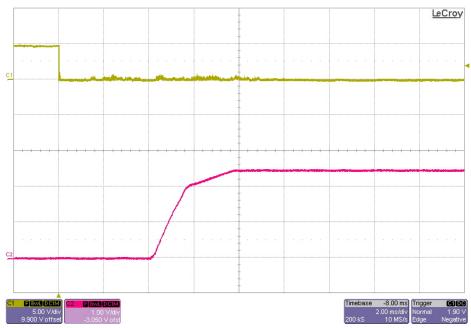


4 Startup

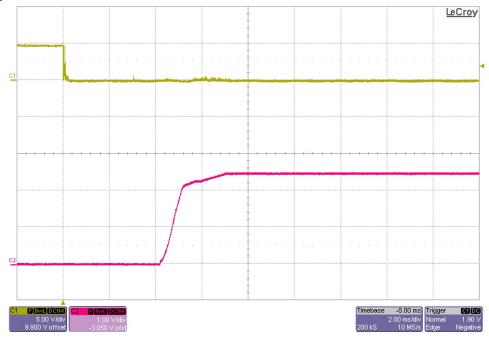
The output voltage at startup is shown in the images below. Channel 1 shows the Enable signal voltage. Channel 2 shows the output voltage.

4.1 No External Capacitance

4.1.1 36V Input - No Load

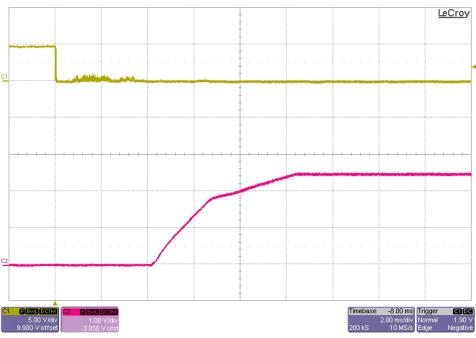


4.1.2 72V Input - No Load

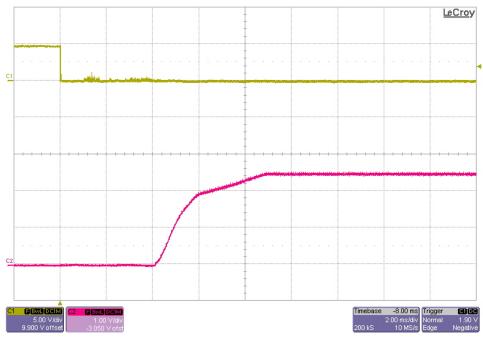




4.1.3 36V Input – 5A Load



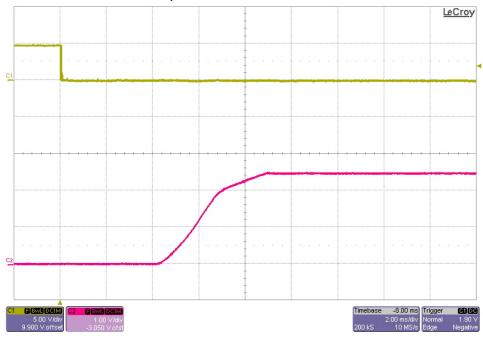
4.1.4 72V Input - 5A Load



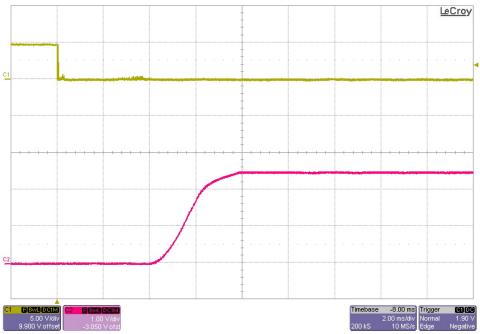


4.2 2700uF External Capacitance

4.2.1 36V Input – 270uF External Capacitance – No Load

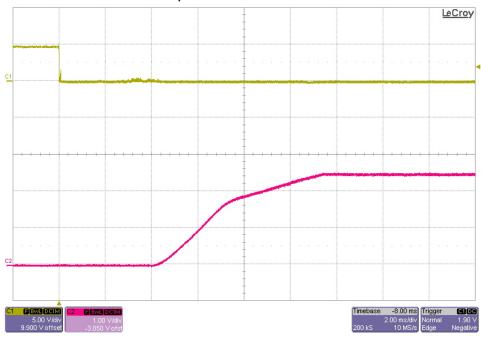


4.2.2 72V Input – 270uF External Capacitance – No Load

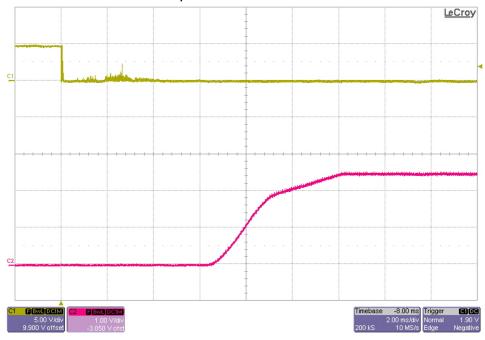




4.2.3 36V Input – 2700uF External Capacitance – 5A Load



4.2.4 72V Input – 2700uF External Capacitance – 5A Load

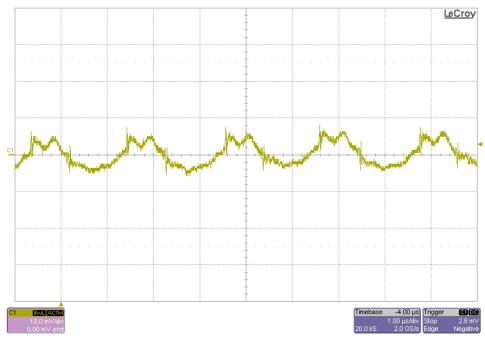




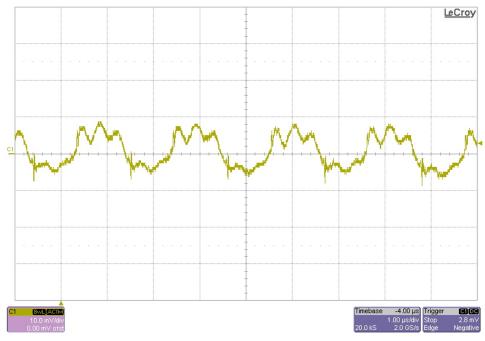
5 Output Ripple Voltage

The output ripple voltage is shown in the plots below. The output was loaded with 5.

5.1 36V Input

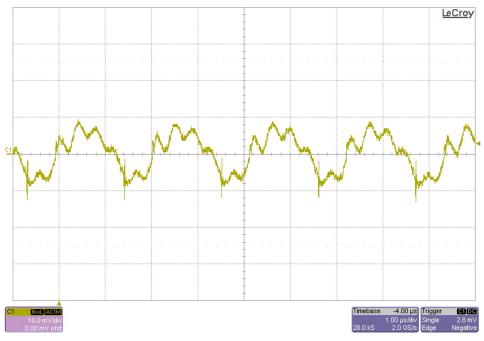


5.2 48V Input





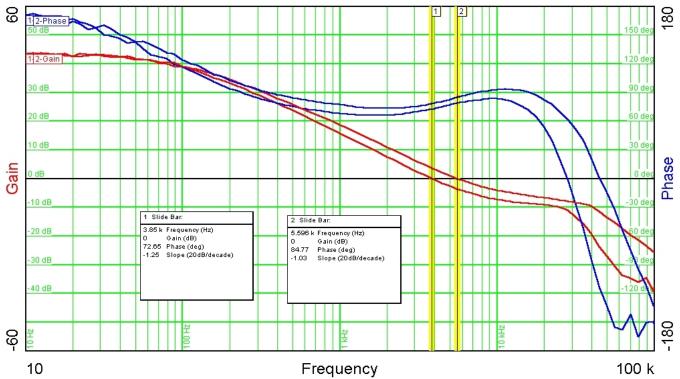
5.3 72V Input



6 Frequency Response

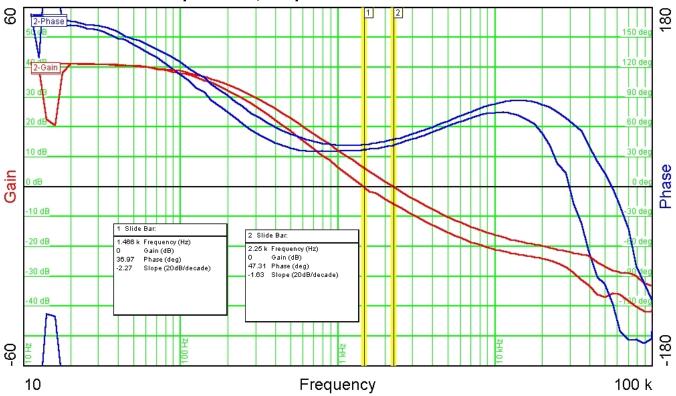
The frequency response of the feedback loop is shown below. For the upper gain and phase plot, the input was set to 72V. For the lower gain and phase plot, the input was set to 36V. The output was loaded with 5A.

6.1 No External Capacitance, Loop Broken At R14

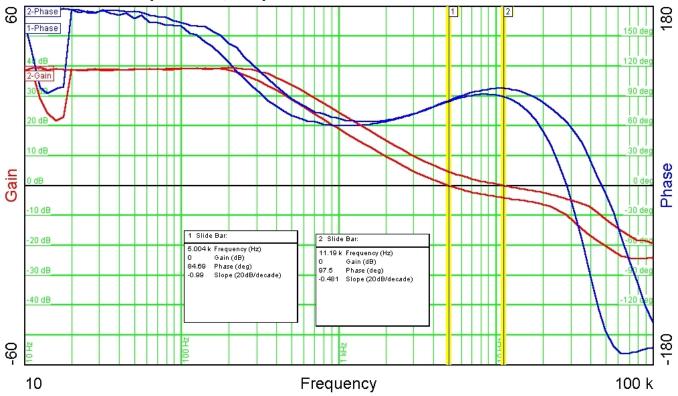




6.2 2700uF External Capacitance, Loop Broken At R14

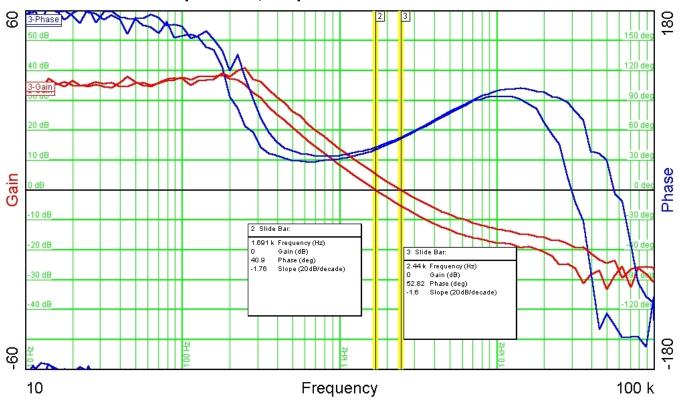


6.3 No External Capacitance, Loop Broken At R26





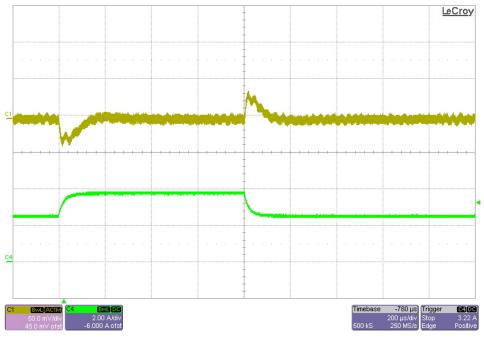
6.4 2700uF External Capacitance, Loop Broken At R26



7 Load Transients

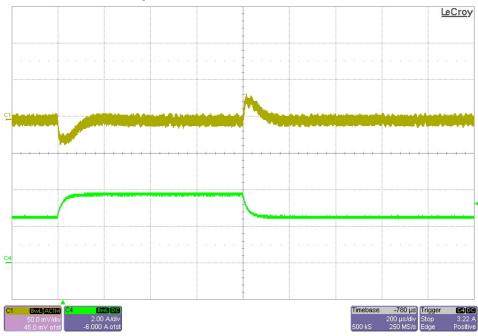
The response to a load step from 2.5A to 3.8A is shown in the images below. Channel 1: Vout 50mV/div (ac coupled); Channel 4: Iout 2A/div

7.1 36V Input – No External Capacitance

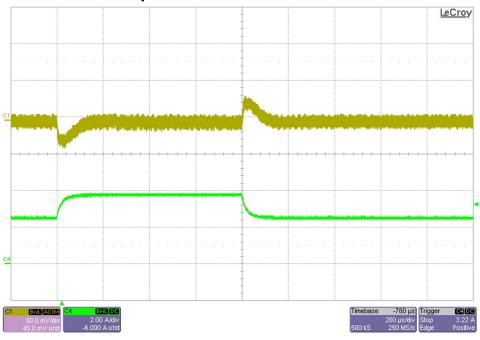




7.2 48V Input – No External Capacitance

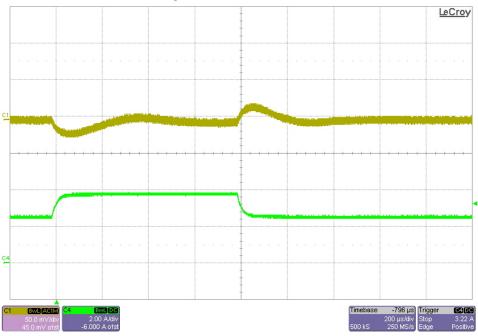


7.3 72V Input – No External Capacitance

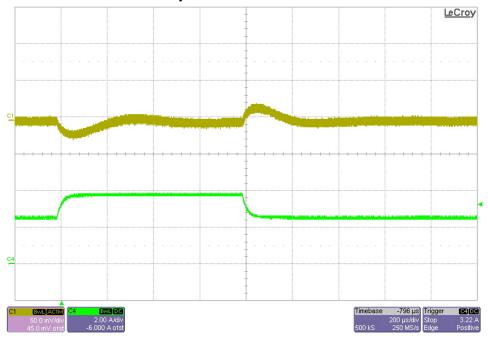




7.4 36V Input – 2700uF External Capacitance

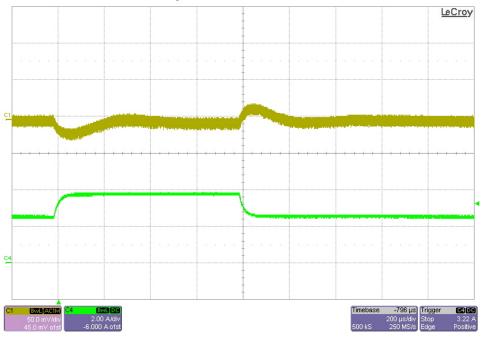


7.5 48V Input – 2700uF External Capacitance





7.6 72V Input – 2700uF External Capacitance



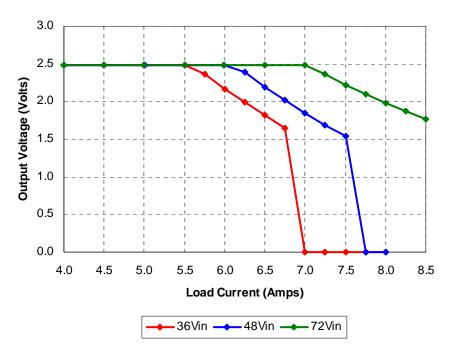
8 Input Under-Voltage Lock-Out

The turn-on and turn-off input voltages were measured and recorded below.

Turn-On	35.0 V
Turn-Off	33.4 V

9 Current Limit

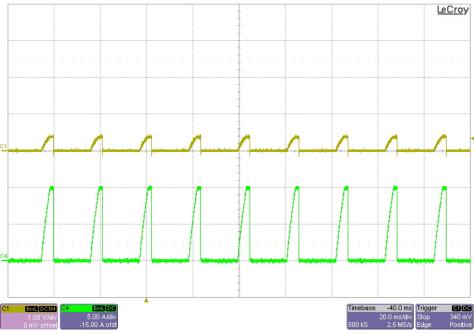
The output voltage versus load current in overload conditions is shown below.





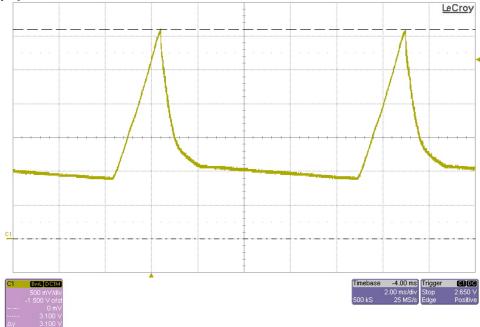
10 Output Short-Circuit

A short was applied to the output of the converter and the output voltage and input current waveforms were captured and displayed below.



11 Output Over-Voltage

An output over-voltage was induced by shorting the +Remote Sense pin (J4) to ground. The output voltage waveform was captured and is displayed below.

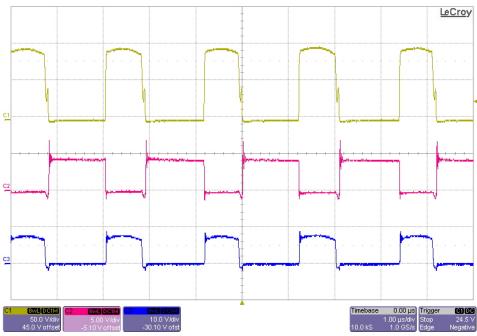




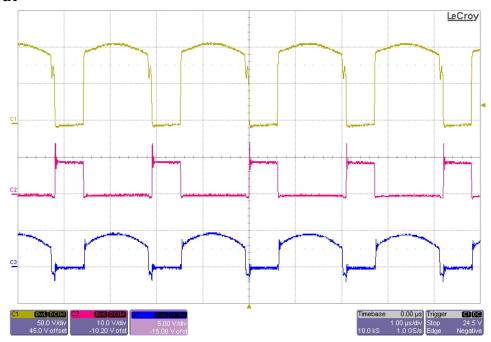
12 Switching Waveforms

The images below show the drain-to-source voltage waveforms on the switching MOSFETs. The output was loaded with 5A. Channel 1: Q4 Vds; Channel 2: Q7 Vds; Channel 3: Q3 Vds.

12.1 36V Input



12.2 72V Input



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