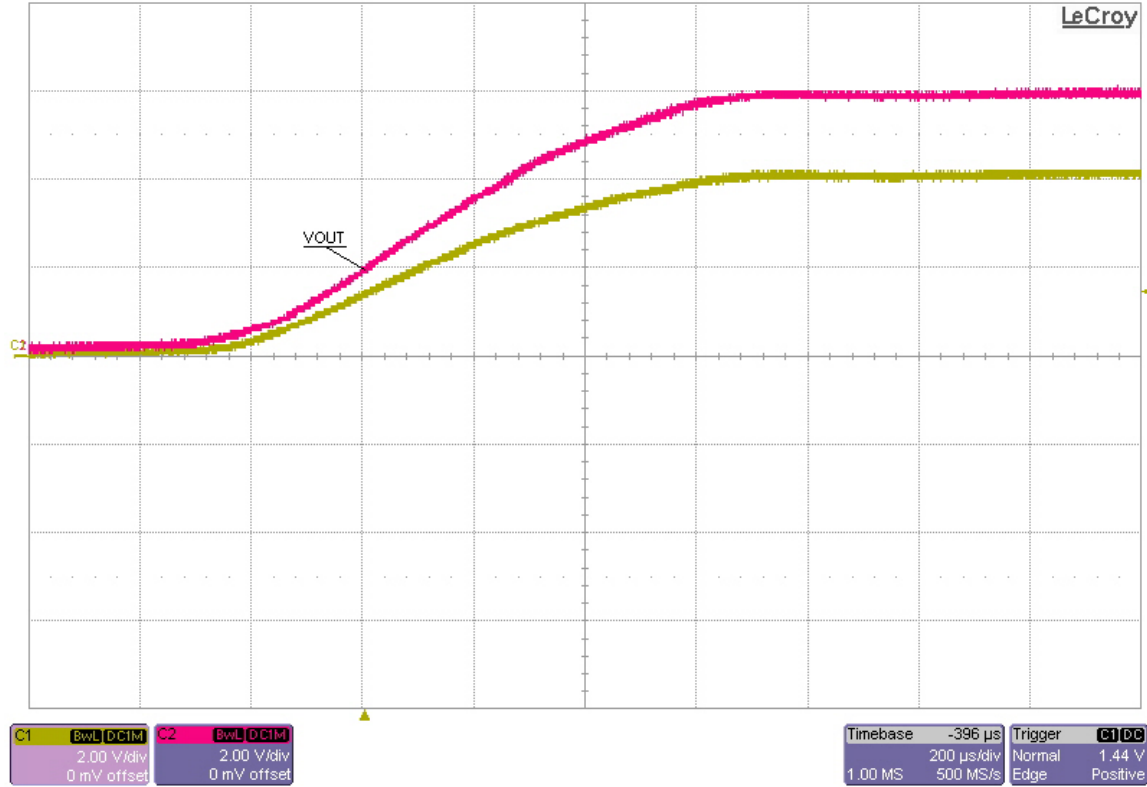




1 Startup

The startup waveform is shown in the figure below. The input voltage was set at 48V, with maximum loads on the outputs.



2 Efficiency and Cross Regulation

The efficiency and cross regulation are shown in the table below.

Vin	lin	6V	6I	4V	4I	Eff
-----	-----	----	----	----	----	-----

PMP6633 Test Results

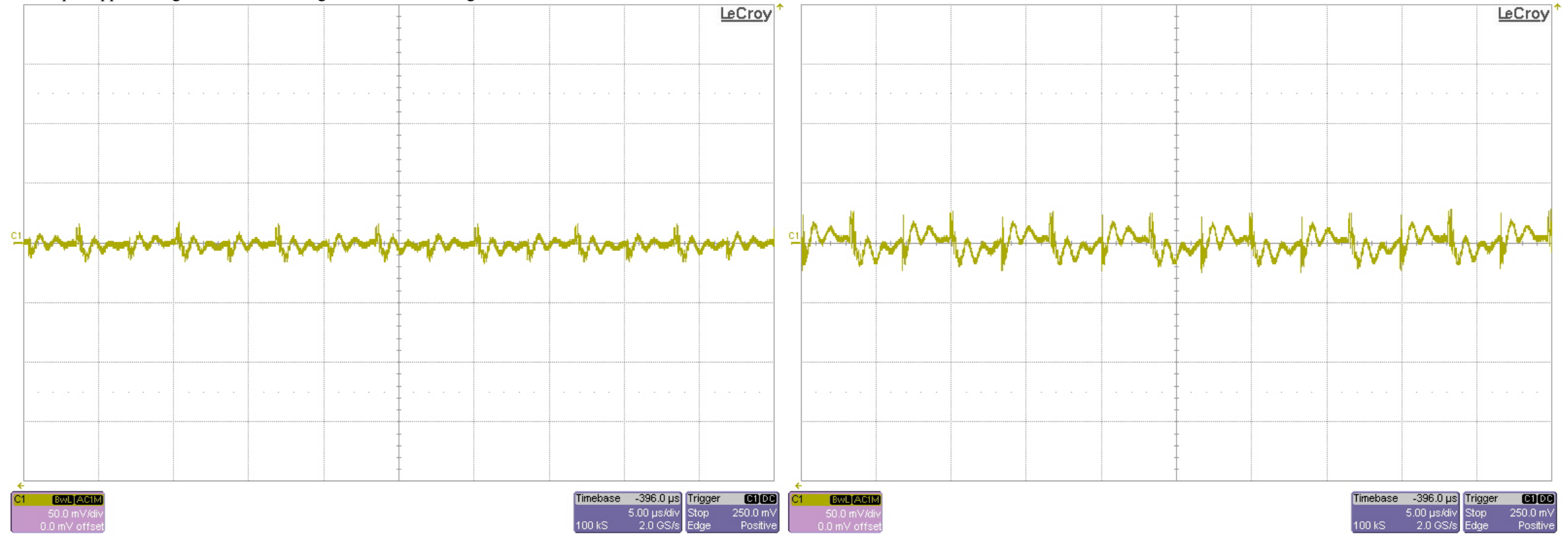


48.83	985	5.949	4.978	4.145	2393	82.2%
48.95	299	6.198	0	4.015	2500	68.6%
48.99	76	6.066	0	4.097	0	
48.99	719	5.825	4.92	5.4226	0	81.4%

PMP6633 Test Results

3 Output Ripple Voltage

The output ripple voltage is shown in the figure below. The image was taken at Full Load. 50 mV/div Vertical and 5 uS/div Horizontal. 4 volts first.

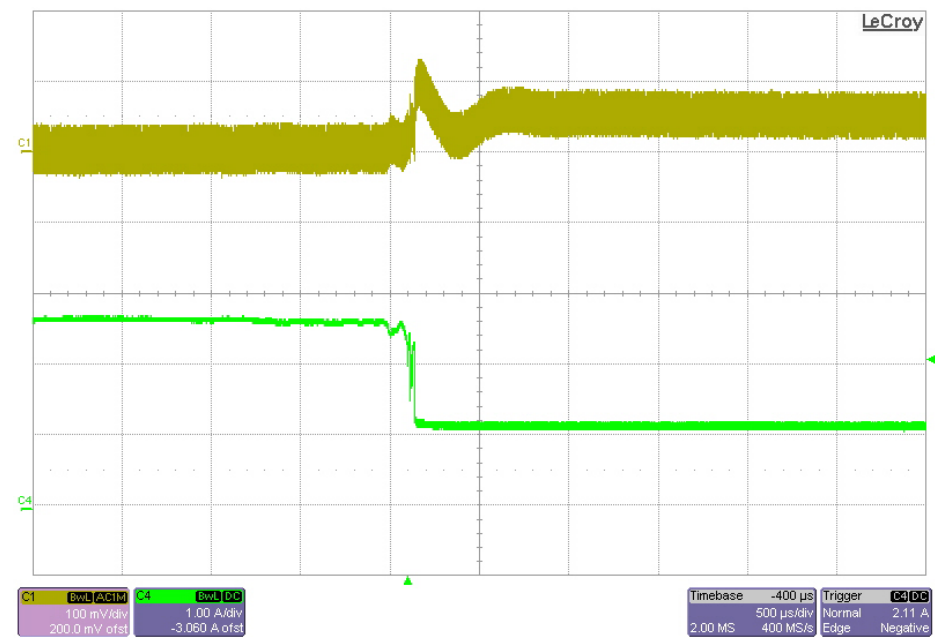


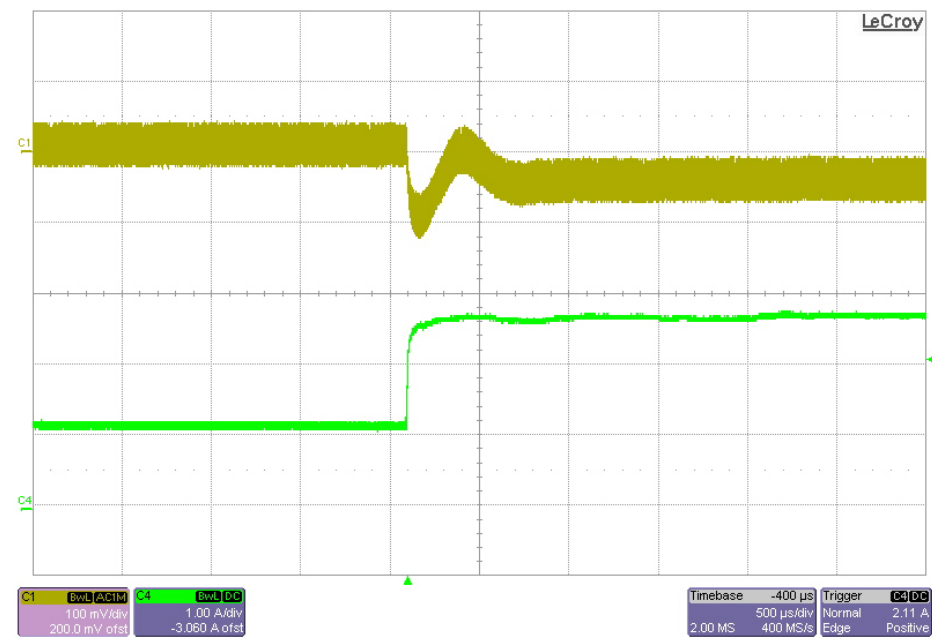
4 Load Transients

The figures below show the 4 volt output response to load transients. The input voltage was set to 48V.

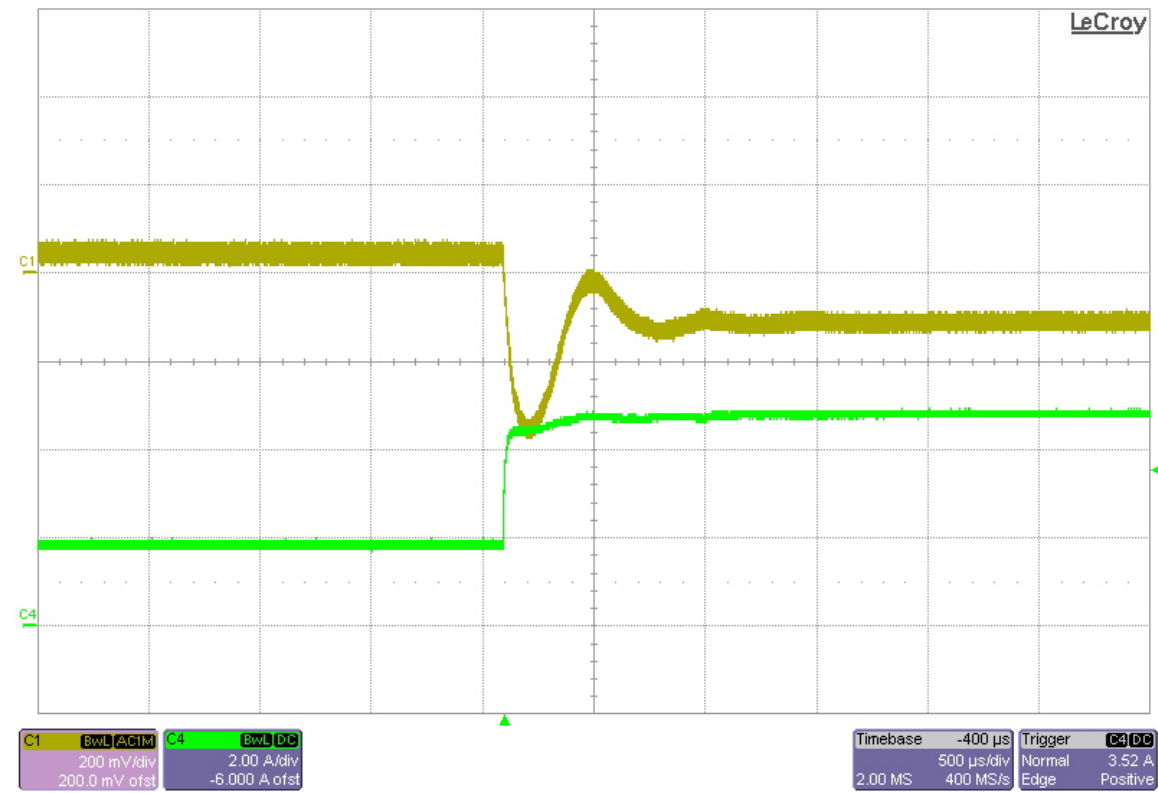
Channel 1 : Vout (AC coupled)

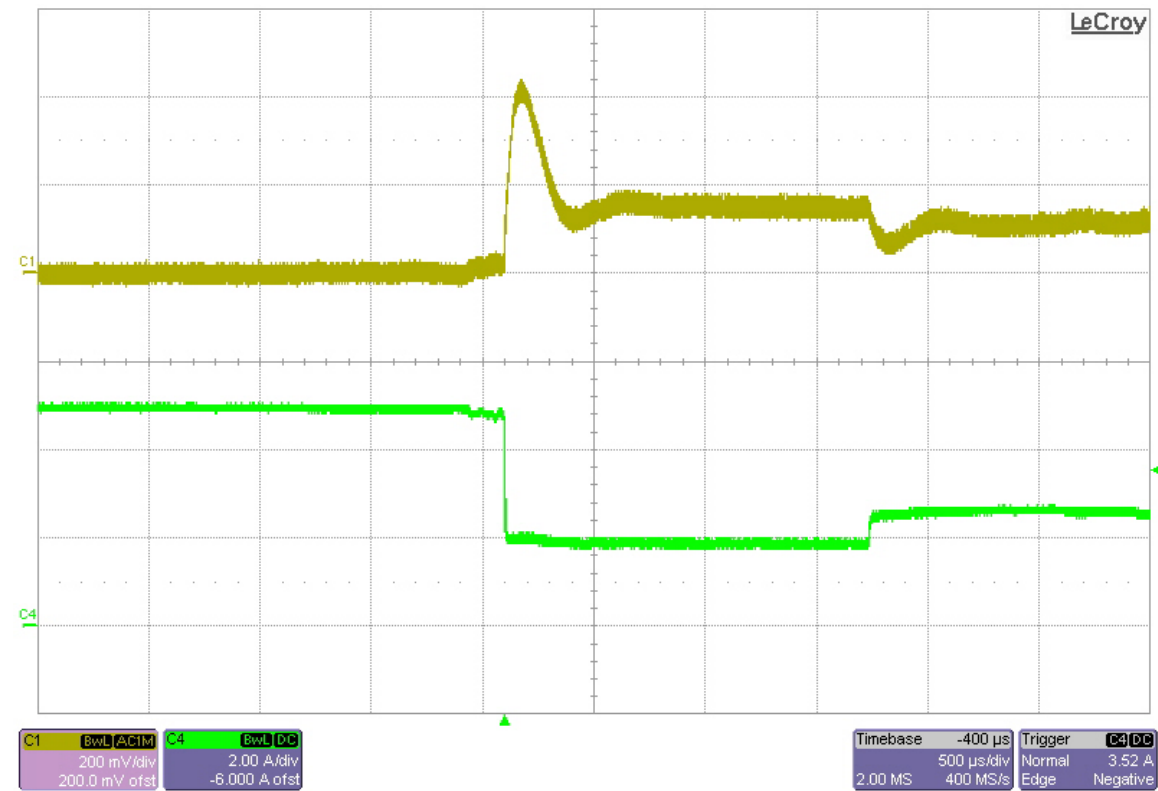
Channel 4 : Load current





The figures below show the 6 volt output response to load transients. The input voltage was set to 48V.

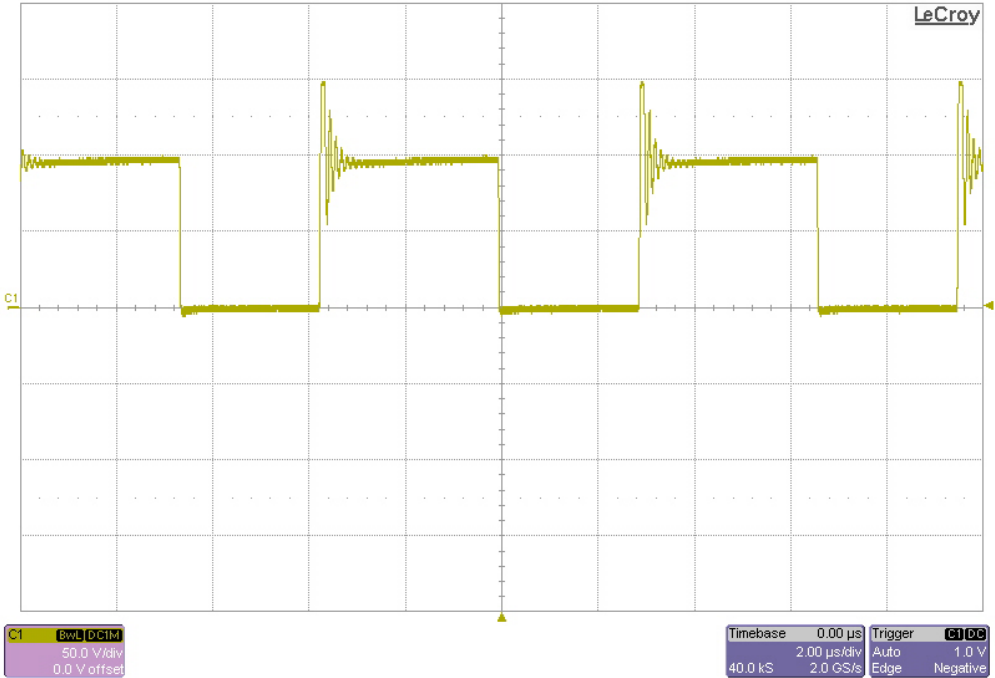




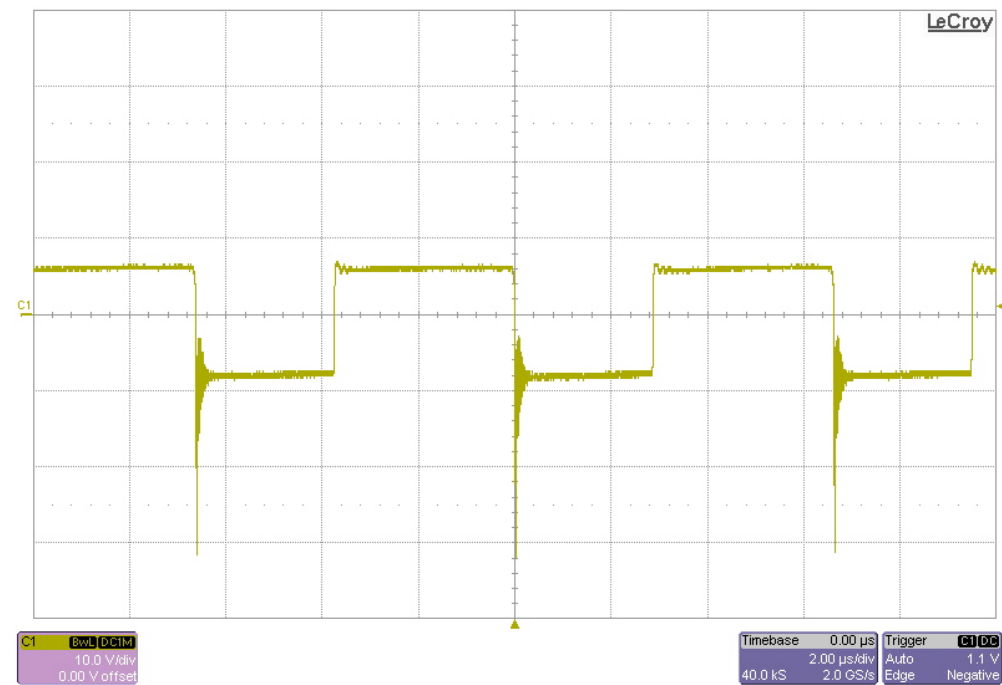
5 Switch Node Waveforms

The following figures show the switch node waveform at high line and maximum load.

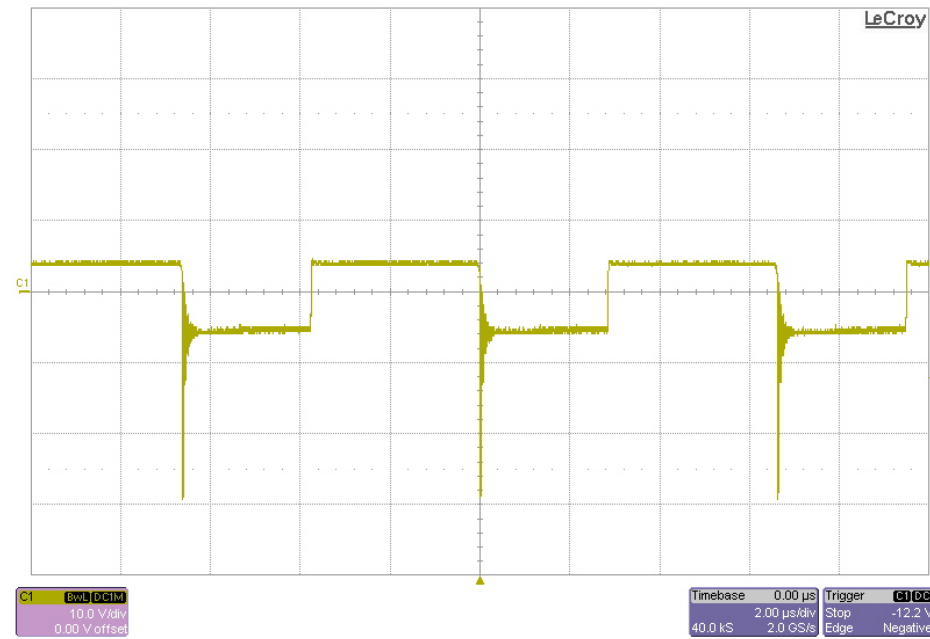
FET Drain



6 Volt Synchronous Rectifier

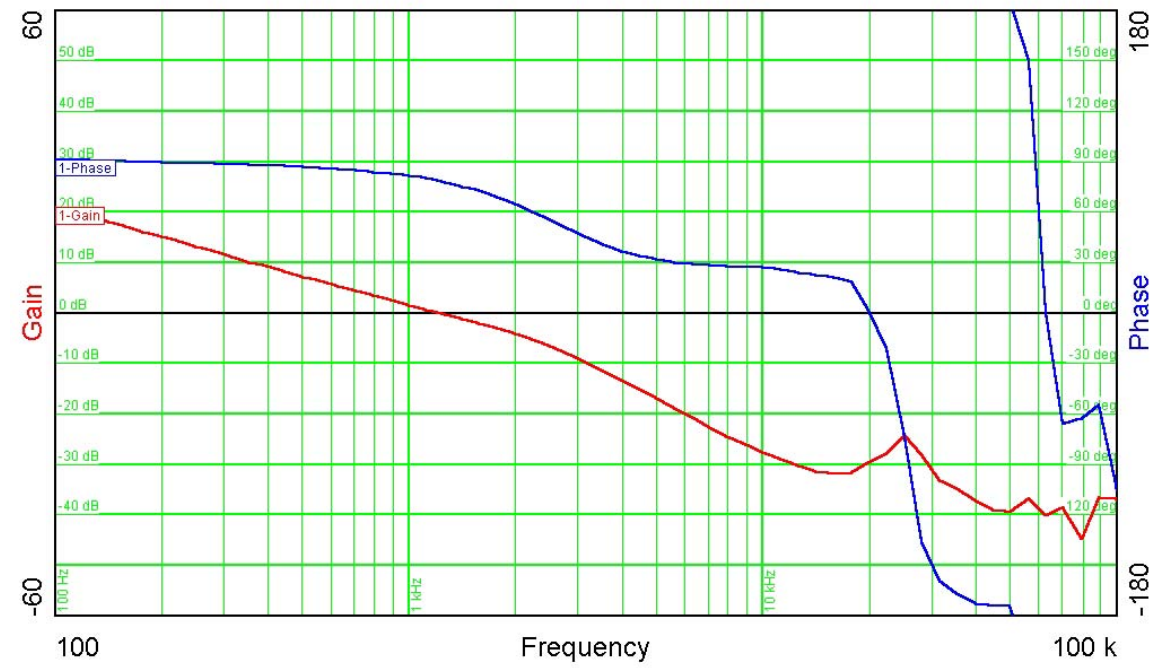


6 Volt Synchronous Rectifier



6 Control Loop

The following figure shows the control loop characteristics. 80 degrees phase margin, 26 dB gain margin.



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