

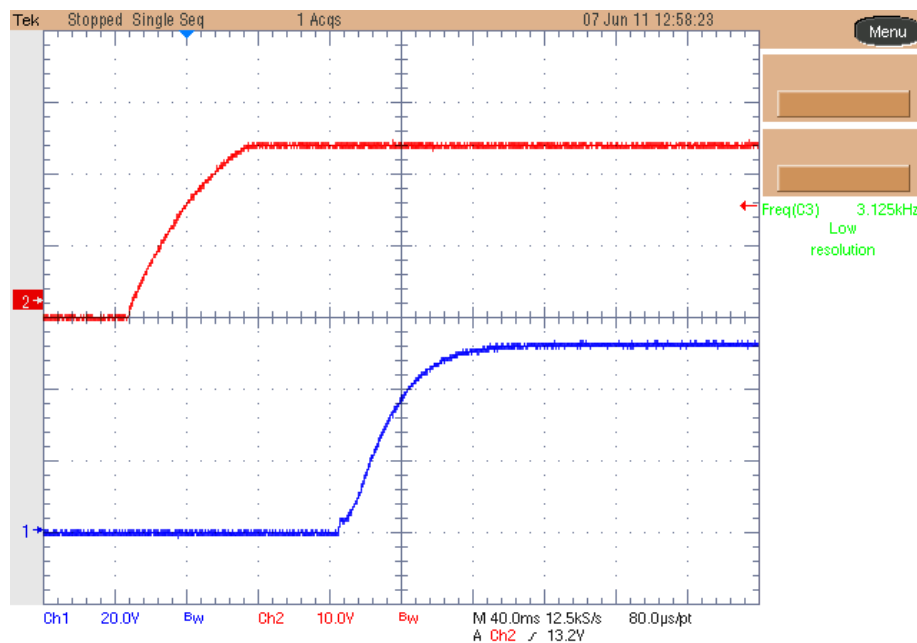
1 Startup

The output voltage behavior at startup is shown in the pictures below. The input voltage has been set to 25V. Upper picture: no load, lower: full load.

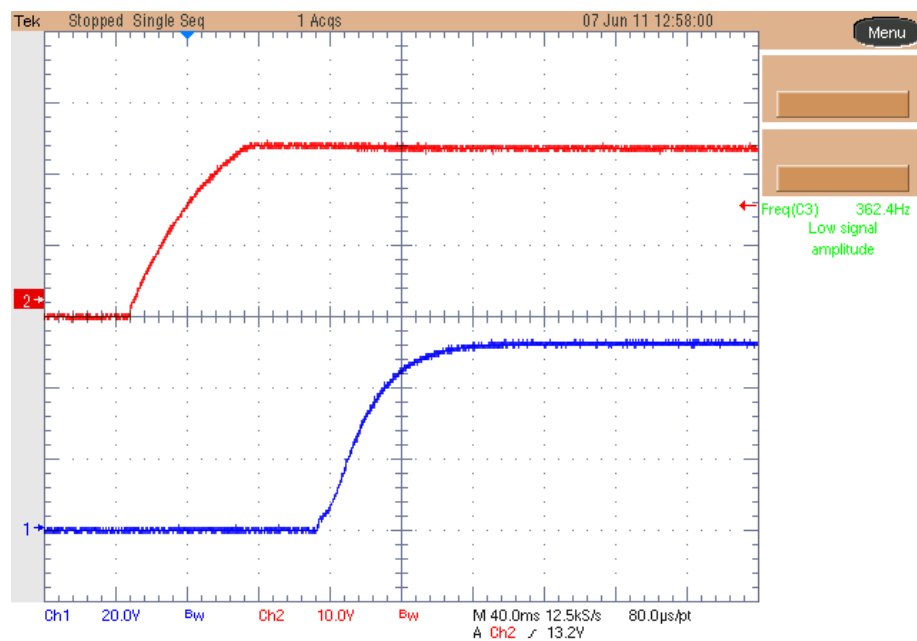
Channel 2: Input Voltage (10V/div, 40ms/div, 20MHz BWL)

Channel 1: Output Voltage (20V/div, 20MHz BWL)

No load:



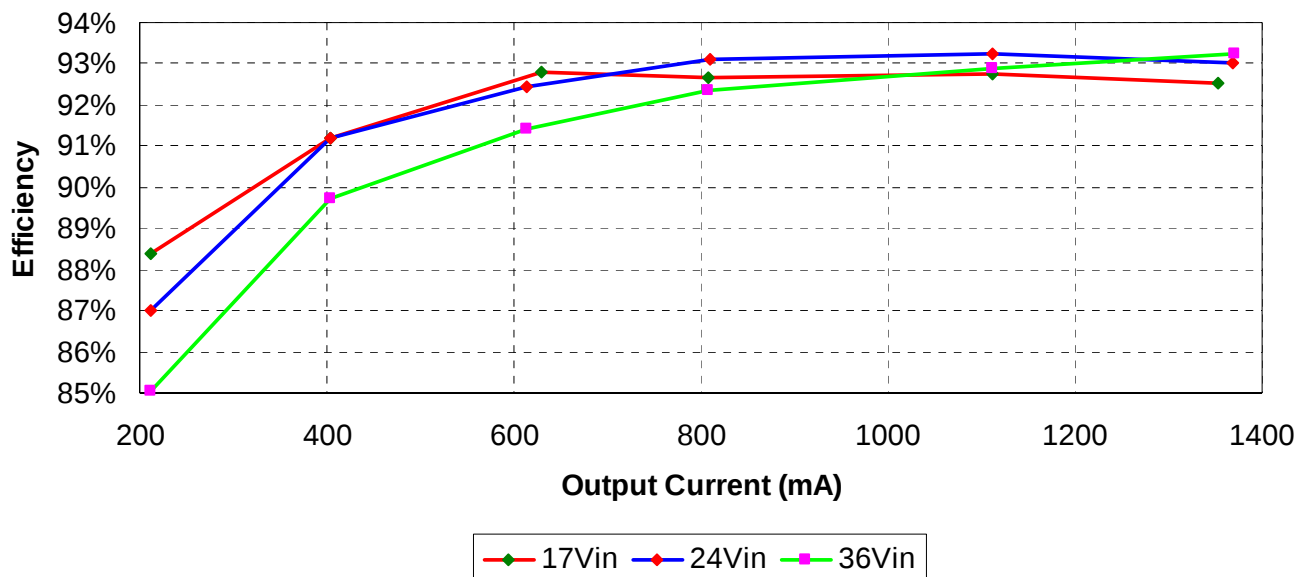
Full load:



2 Efficiency

The efficiency data is shown in the tables and graph below. The input voltage was set to 17V, 24V and 36V, while the load has been varied between 0 and full load (1.35A).

Note also that the output voltage changes only slightly from 52.45V to 52.44V. The graph has been therefore not shown.



I _{out} (mA)	V _{out} (V)	P _{out} (W)	I _{in} (mA)	V _{in} (V)	P _{in} (W)	P _{loss} (W)	Eff
0.0	52.45	0.00	54.6	17.02	0.929	0.93	0.00%
211.5	52.45	11.09	737.8	17.01	12.550	1.46	88.39%
403.6	52.45	21.17	1358	17.09	23.208	2.04	91.21%
630.1	52.45	33.05	2090	17.04	35.614	2.56	92.80%
808.3	52.45	42.40	2690	17.01	45.757	3.36	92.65%
1111.6	52.45	58.30	3683	17.07	62.869	4.57	92.74%
1353	52.45	70.96	4494	17.07	76.713	5.75	92.51%

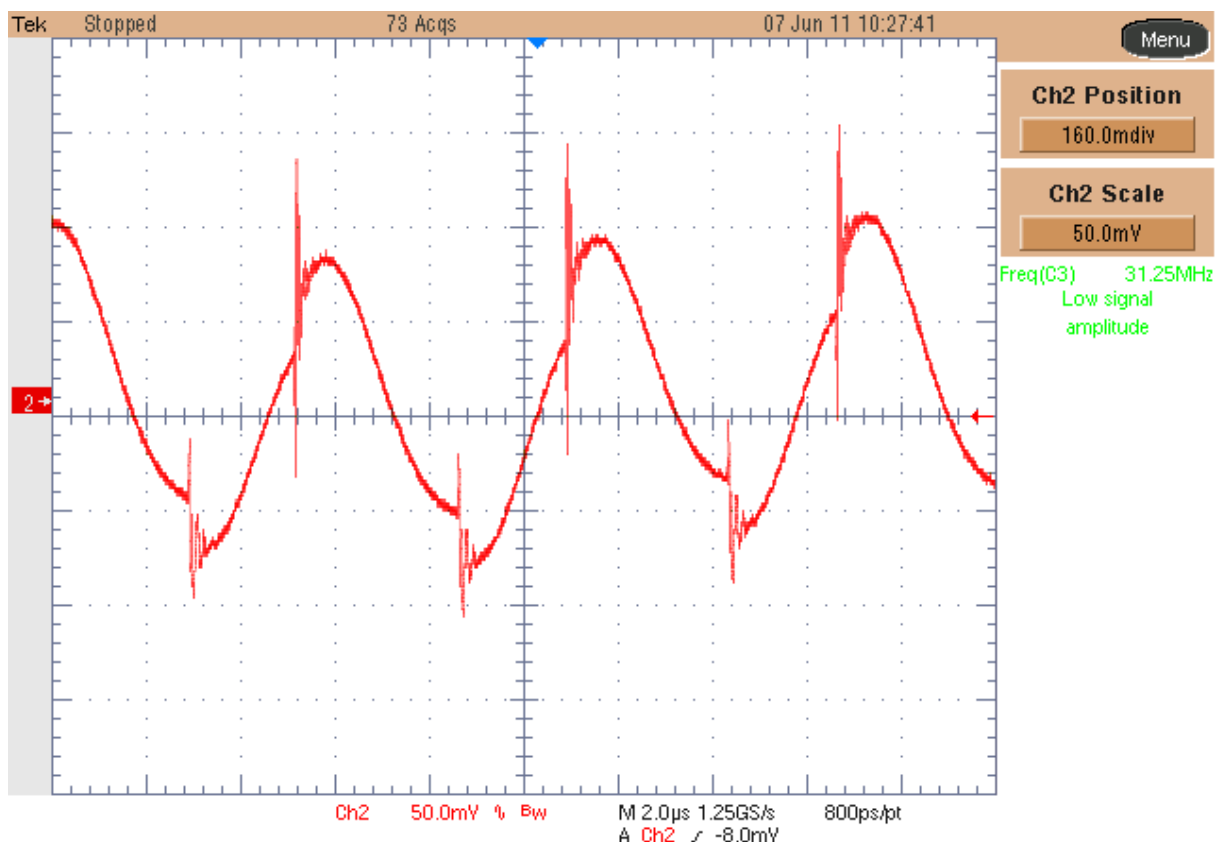
I _{out} (mA)	V _{out} (V)	P _{out} (W)	I _{in} (mA)	V _{in} (V)	P _{in} (W)	P _{loss} (W)	Eff
0.0	52.45	0.00	44.3	24.00	1.063	1.06	0.00%
211.7	52.45	11.10	531.8	24.00	12.763	1.66	87.00%
403.9	52.45	21.18	966.8	24.03	23.232	2.05	91.19%
614.6	52.45	32.24	1449	24.07	34.877	2.64	92.43%
808.9	52.45	42.43	1899	24.00	45.576	3.15	93.09%
1112.3	52.45	58.34	2605	24.02	62.572	4.23	93.24%
1369	52.45	71.80	3217	24.00	77.208	5.40	93.00%

I _{out} (mA)	V _{out} (V)	P _{out} (W)	I _{in} (mA)	V _{in} (V)	P _{in} (W)	P _{loss} (W)	Eff
0.0	52.45	0.00	35.7	36.07	1.288	1.29	0.00%
211.3	52.45	11.08	361.6	36.03	13.028	1.95	85.07%
403.7	52.45	21.17	654.5	36.06	23.601	2.43	89.72%
614.2	52.44	32.21	978.1	36.02	35.231	3.02	91.42%
808.5	52.44	42.40	1272	36.10	45.919	3.52	92.33%
1112.3	52.44	58.33	1742	36.05	62.799	4.47	92.88%
1370	52.44	71.84	2140	36.00	77.040	5.20	93.25%

3 Output ripple voltage

The output ripple voltage, measured at full load and at 24V input, is shown in the plot below.

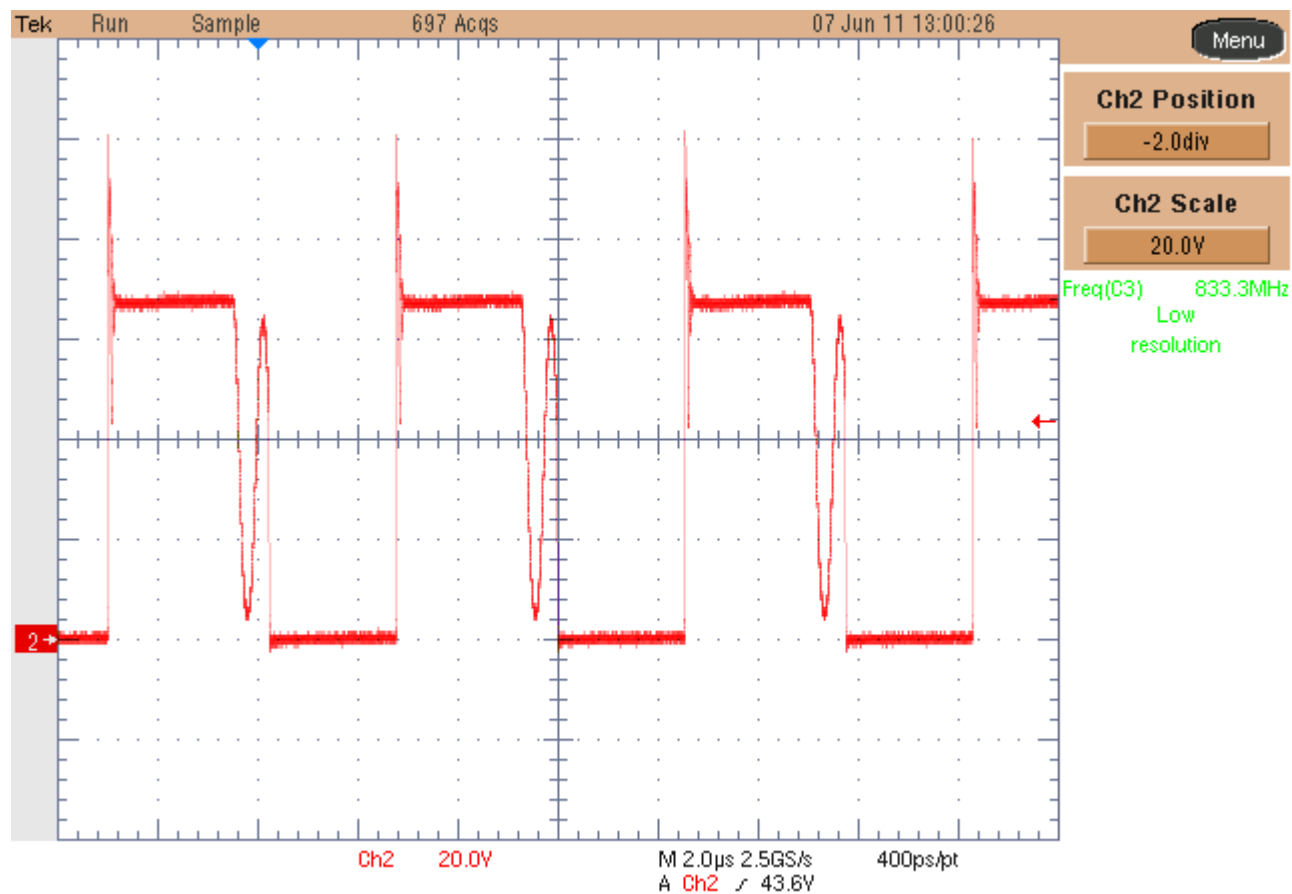
Channel 2: Output Voltage (50 mV/div, 2 μ s/div, AC coupling, 20MHz BWL)



4 Switch-node

The image below shows the switch-node waveform (drain of Q1, Q2). The input voltage was set to 36V and the output fully loaded.

Channel 2: Q1, Q2 Vds Voltage (20 V/div, 2us/div, No BWL).

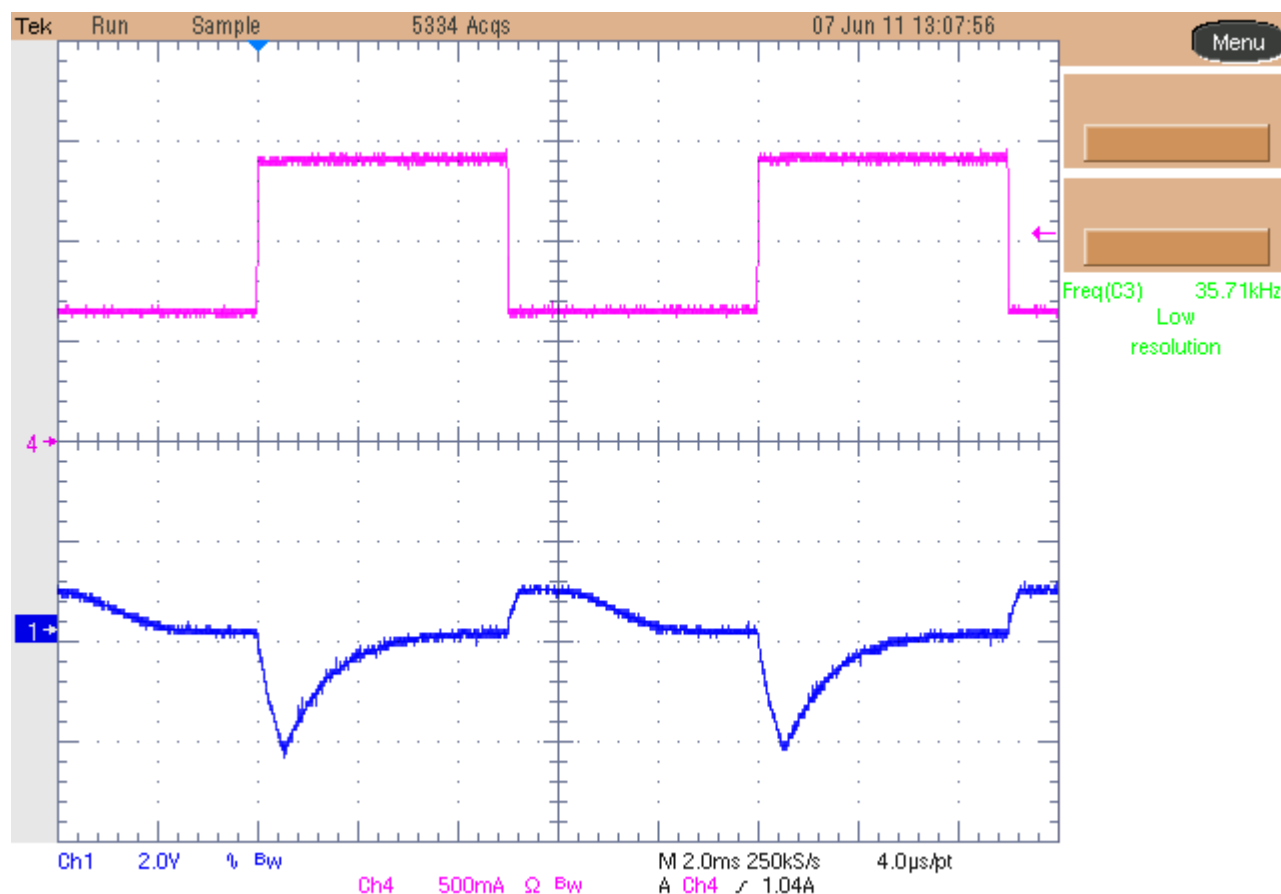


5 Transient response

The image below shows the transient response of the output voltage when the load was switched between 650mA and 1.35A. The input voltage was set to 24V.

Channel 1: Output Voltage (2V/div, 2ms/div, AC coupling, 20 MHz BWL).

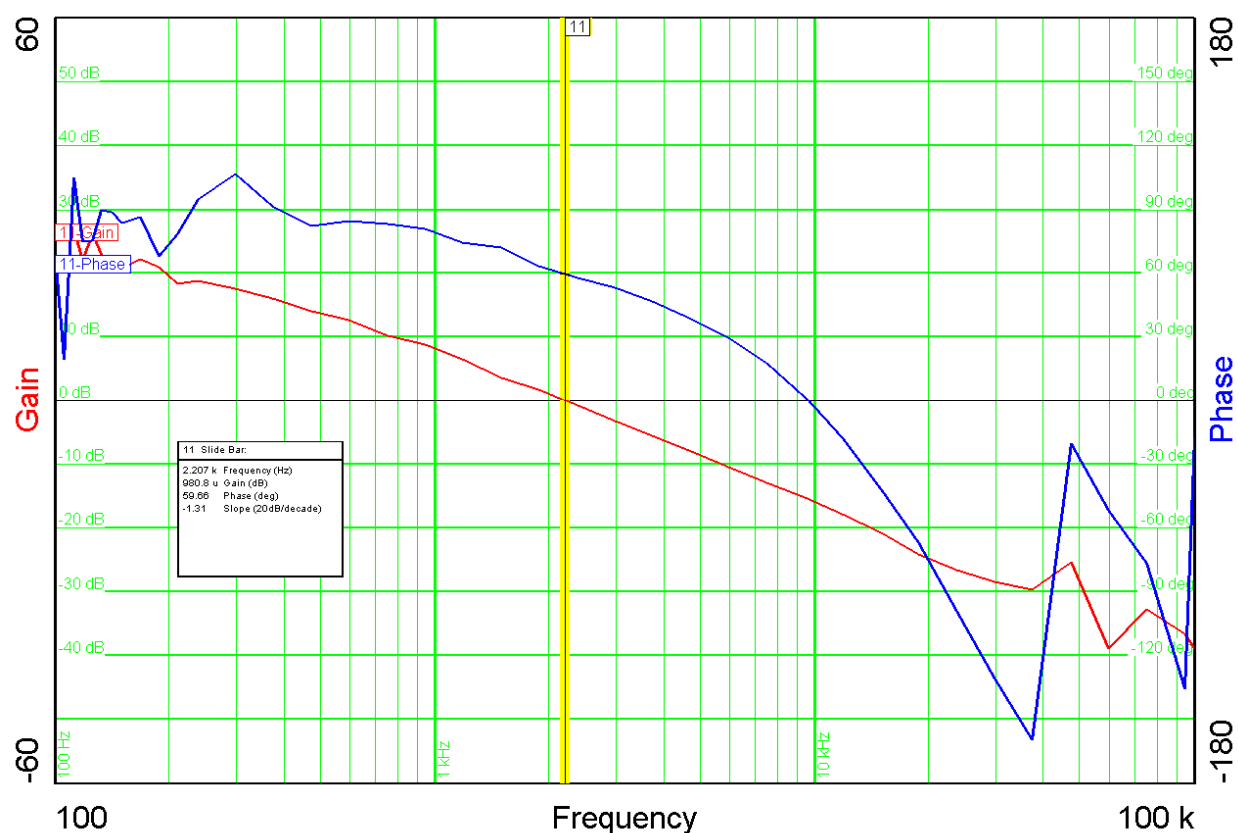
Channel 2: Output current (500 mA/div, DC coupling, 20 MHz BWL).



6 Loop Response

The image below shows the loop response of the converter measured at worst case input voltage, which is 17V, and full load. This is the worst case since the converter works, at this input voltage, in continuous conduction mode, thus generating a right half plane zero; this is the reason why we must keep low the crossover frequency.

The phase margin was 59.66 deg., the gain margin 15.22dB, and the crossover frequency was 2.207KHz.



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