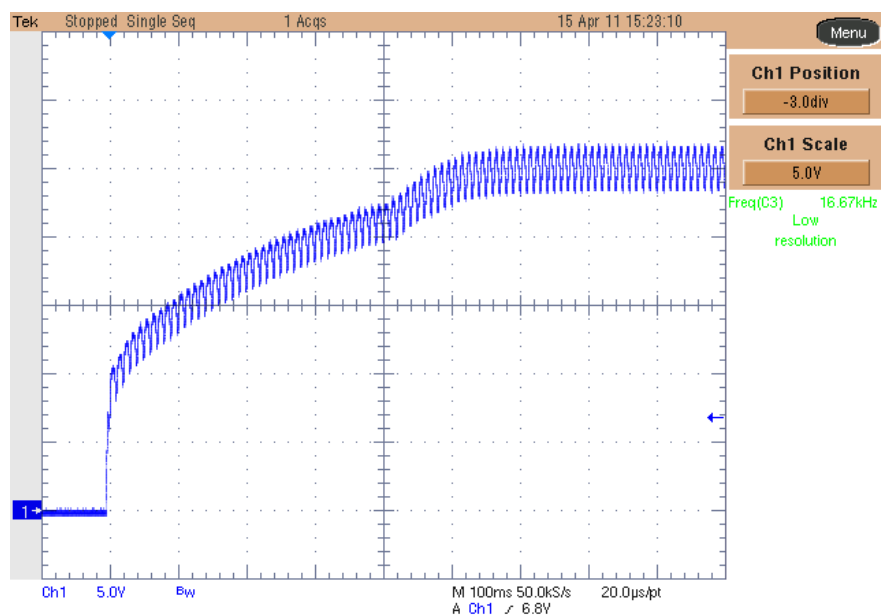


1 Startup

The output voltage at startup is shown in the image below. Input voltage was set to 230Vac and both outputs fully loaded.

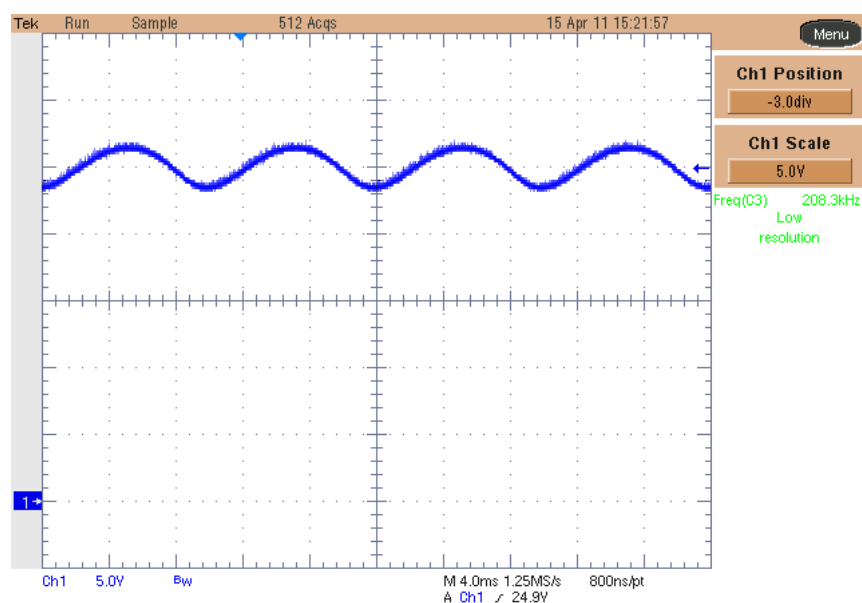
Channel 1: Output voltage (5V/div, 100ms/div, 20MHz BWL).



2 Output Ripple Voltage

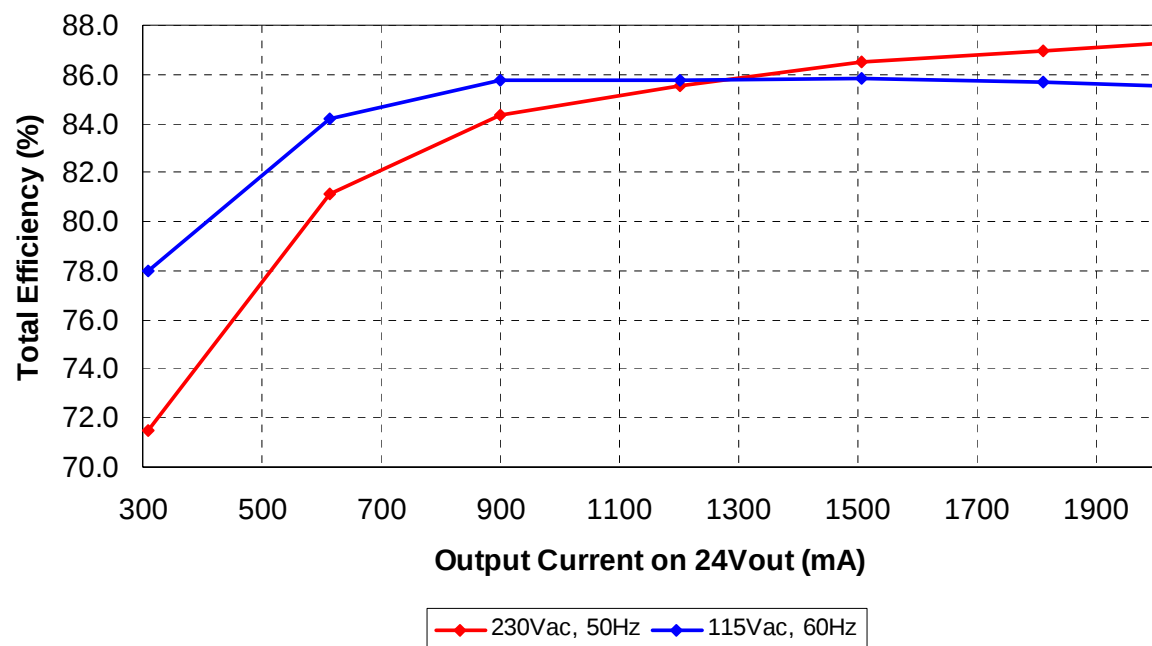
The output ripple voltage is shown in the plot below. The source and load setup was the same as above.

Channel 1: Output voltage (5 V/div, 4ms/div, dc coupling, 20MHz BWL).



3 Efficiency

The efficiency data are shown in the tables and graph below.

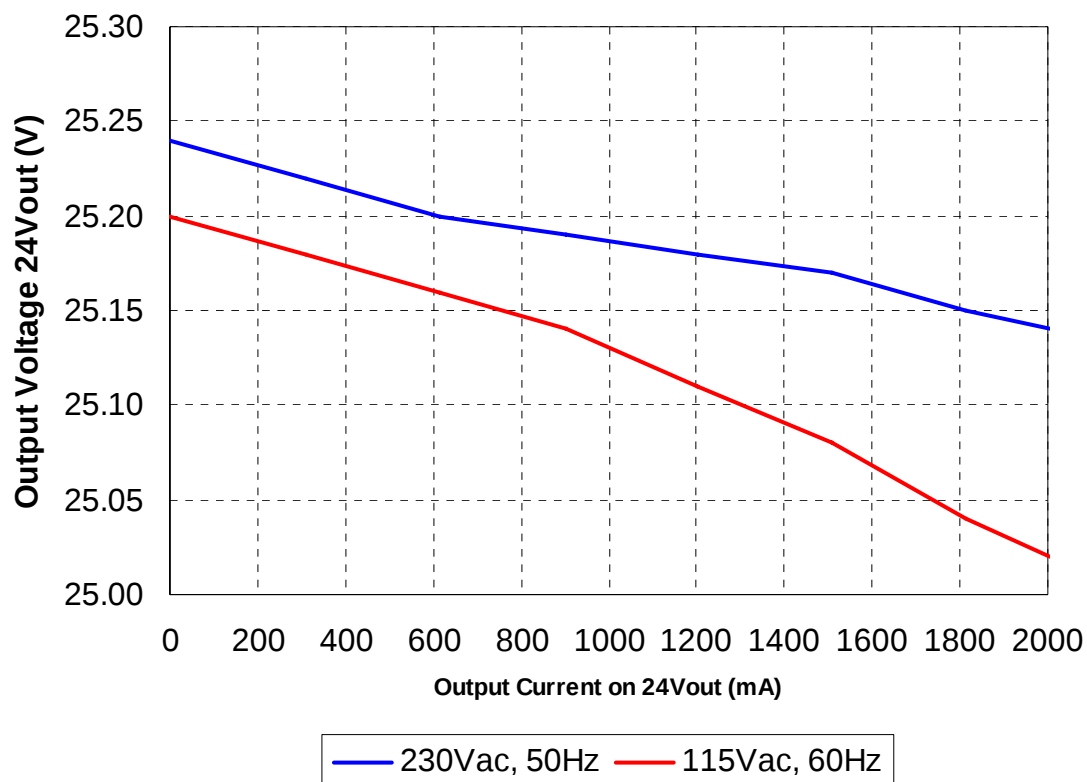


Iout 24V (mA)	Vout 24V (Vdc)	Iout 5V (mA)	Vout 5V (Vdc)	Pout (W)	Vin (Vac)	Pin (W)	Ploss (W)	Eff (%)	PF (%)
0.0	25.24	0.0	5.01	0.00	230	1.04	1.04	0.00	16.7
308.3	25.22	100.6	5.01	8.28	230	11.58	3.30	71.50	63.35
613.5	25.20	200.7	5.00	16.46	230	20.30	3.84	81.10	79.45
901.6	25.19	300.2	4.99	24.21	230	28.70	4.49	84.35	85.21
1202	25.18	401.4	4.99	32.27	230	37.74	5.47	85.50	88.77
1507	25.17	500.0	4.99	40.43	230	46.75	6.32	86.47	90.89
1811	25.15	600.5	4.99	48.54	230	55.81	7.27	86.98	92.36
2004	25.14	600.4	4.99	53.38	230	61.18	7.80	87.25	92.95

Iout 24V (mA)	Vout 24V (Vdc)	Iout 5V (mA)	Vout 5V (Vdc)	Pout (W)	Vin (Vac)	Pin (W)	Ploss (W)	Eff (%)	PF (%)
0.0	25.20	0.0	5.01	0.00	115	0.66	0.66	0.00	28.2
308.6	25.18	101.6	5.01	8.28	115	10.62	2.34	77.96	92.88
613.7	25.16	200.9	5.00	16.45	115	19.53	3.08	84.20	96.56
901.4	25.14	300.2	5.00	24.16	115	28.18	4.02	85.74	97.42
1201	25.11	400.6	4.99	32.16	115	37.50	5.34	85.75	97.7
1506	25.08	501.3	4.99	40.27	115	46.91	6.64	85.85	97.91
1811	25.04	600.9	4.99	48.35	115	56.44	8.09	85.66	97.97
2004	25.02	600.9	4.99	53.14	115	62.11	8.97	85.56	97.98

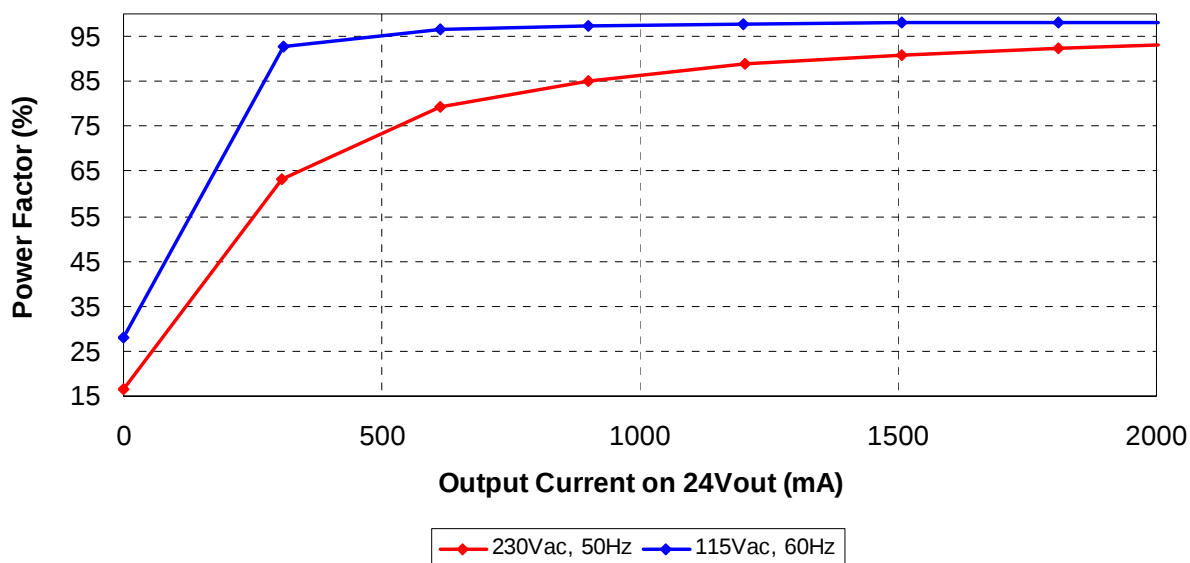
4 Output Voltage Regulation

The output voltage (24Vout) versus output current graph is plotted below.



5 Power Factor

The Power Factor graph for the two nominal input voltages (230Vac, 50Hz and 115Vac 60Hz) is shown below:

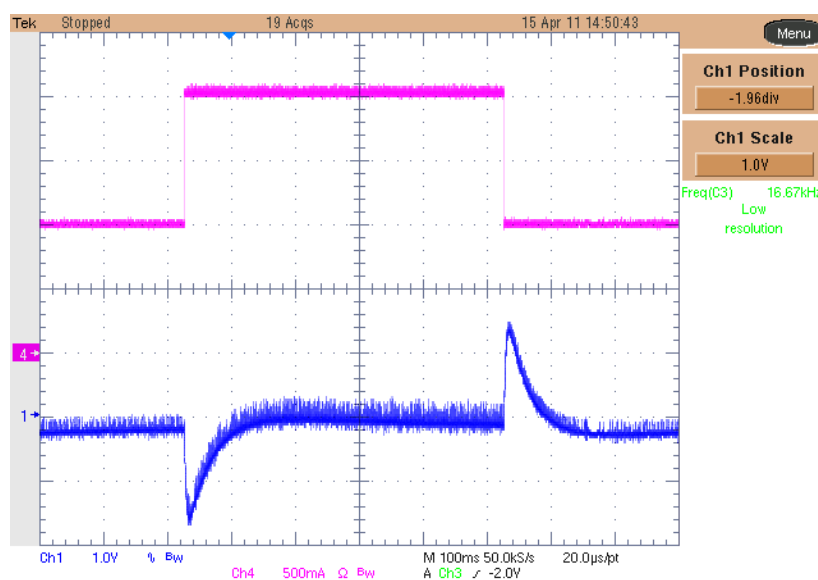


6 Transient Response

The output voltage (24V_{out}) transient response is shown in the plot below. The input was set to 270V_{dc} and the load switched between 1A and 2A.

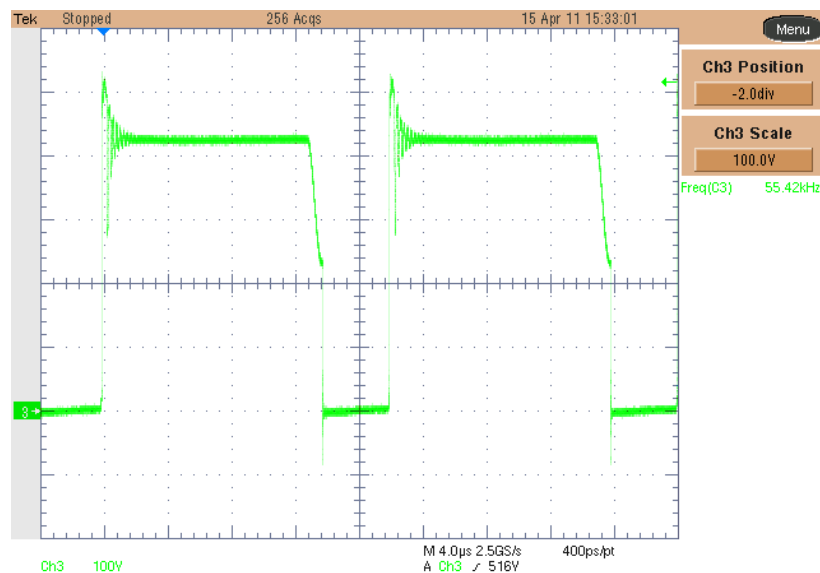
Channel 1: Output voltage on 24Vout (1 V/div, ac coupled, 100ms/div, 20MHz BWL)

Channel 4: Output current (500mA/div, dc coup.)



7 Switching Node Waveform

The image below shows the voltage on the drain of Q1, with a 230Vac input, and full load on both outputs. Channel 3 shows the drain voltage (100V/div, 4 μ s/div, no BWL).

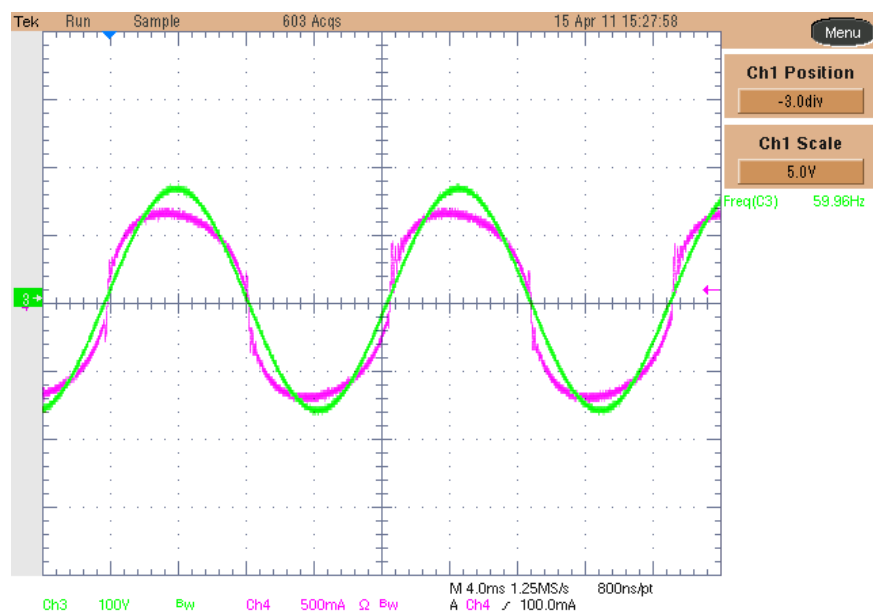


8 Input Voltage and Current Waveforms

The images below show the input voltage and current while the source was set to the two different input voltages and the converter was fully loaded on both outputs.

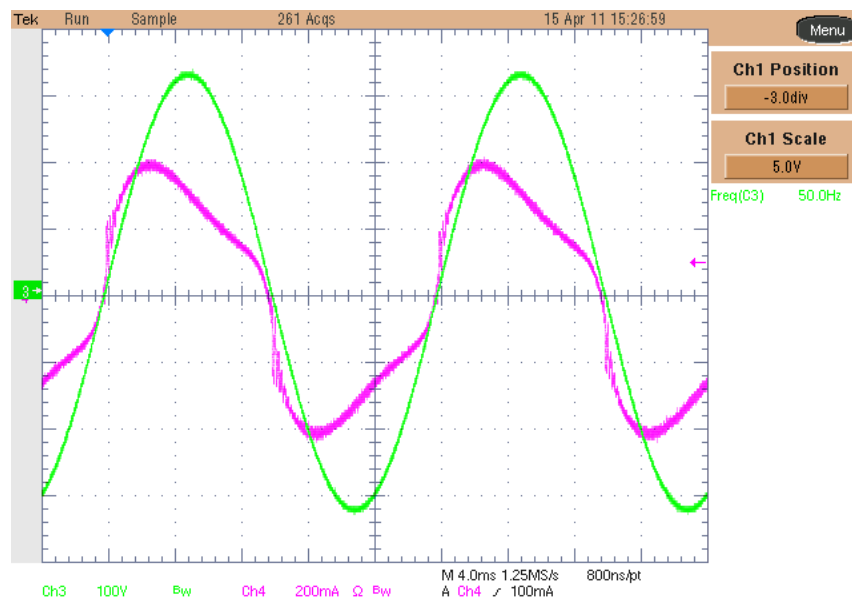
V_{in} = 115Vac, 60Hz

Channel 3: Input voltage (100V/div, 4ms/div); Channel 4: Input current (500mA/div)



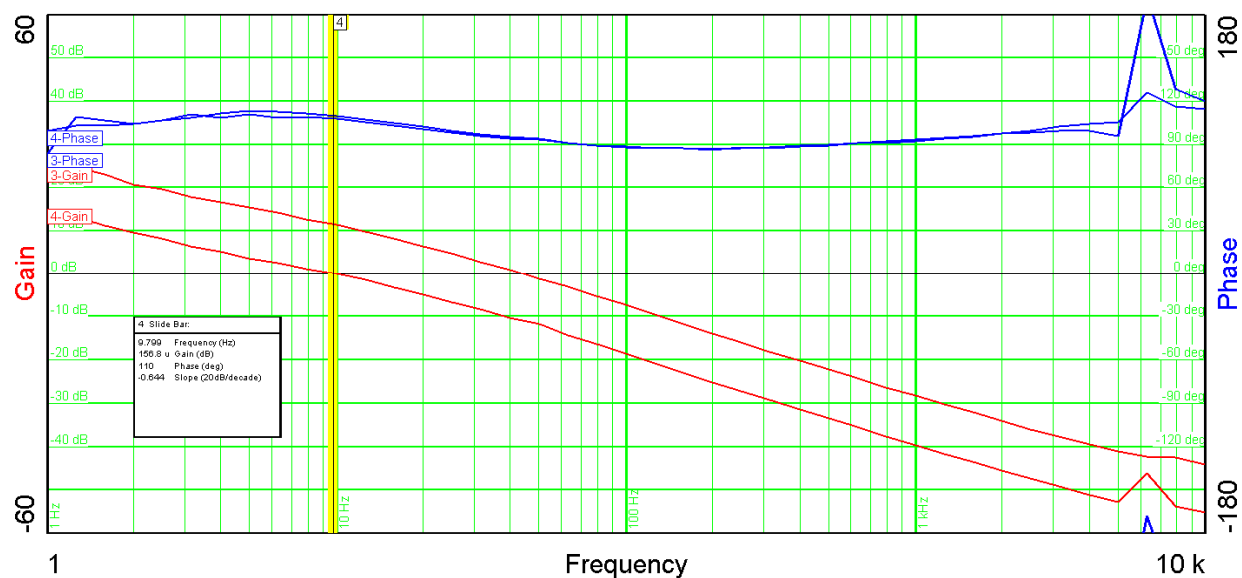
V_{in} = 230Vac, 50Hz

Channel 3: Input voltage (100V/div, 4ms/div); Channel 4: Input current (200mA/div)



9 Loop Response

The image below shows the loop response of the converter (on the 24Vout) measured with a 120Vdc input and 266Vdc @ 2A load. Worst case phase margin is 93.6 deg. and crossover frequency is 43.93 Hz.



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