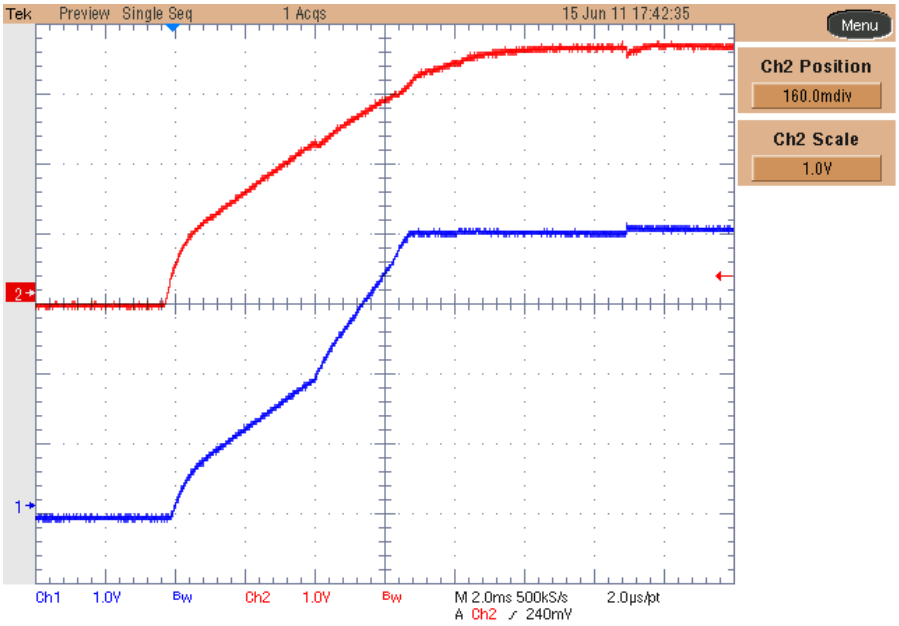
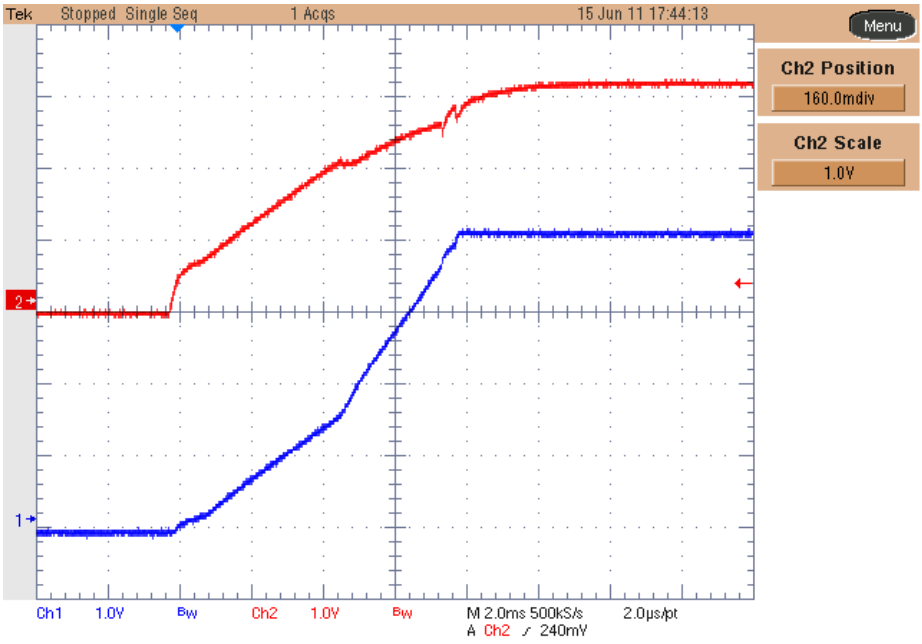
1 Startup

The output voltage behavior at startup is shown in the pictures below. The input voltage has been set to 3.6V. Upper picture: no load, lower: full load.
Channel 2: Input Voltage (1V/div, 2ms/div, 20MHz BWL)
Channel 1: Output Voltage (1V/div, 20MHz BWL)

No load:

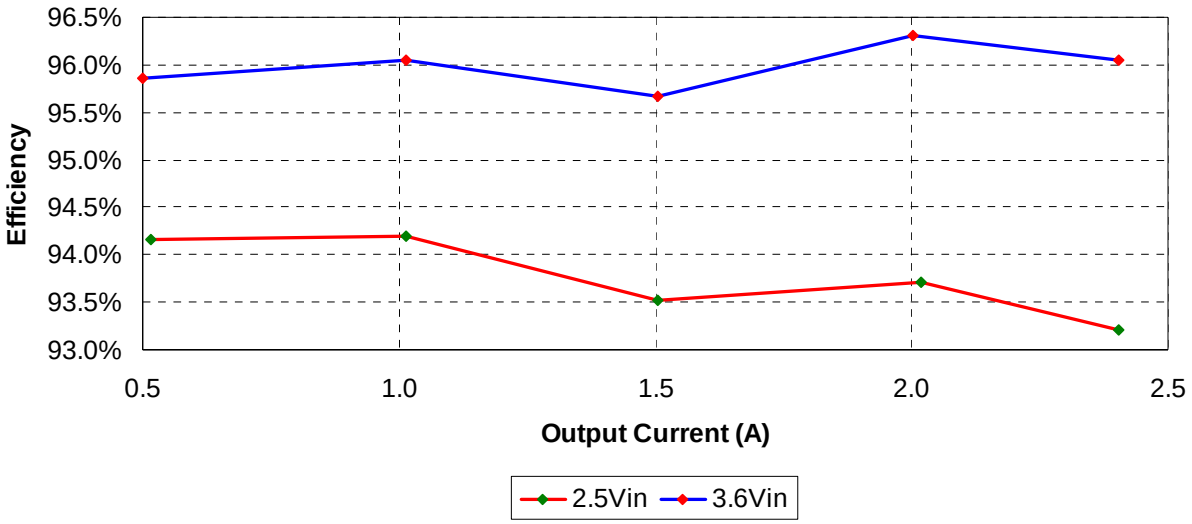


Full load:



2 Efficiency

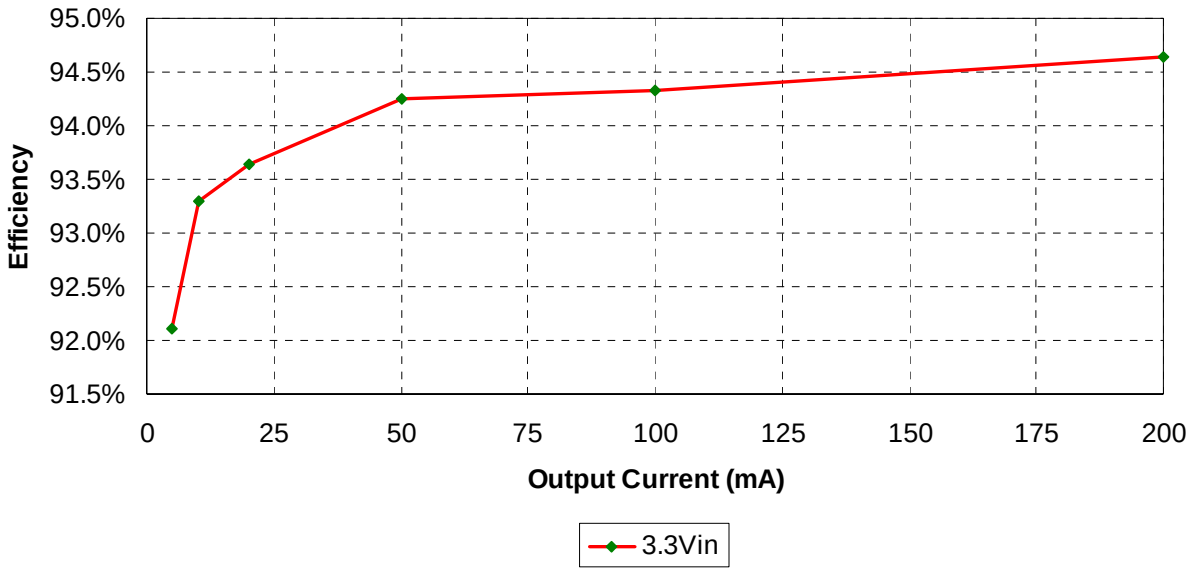
The efficiency data is shown in the tables and graphs below. The input voltage was set to 2.5V and 3.6V while the load has been varied from 500mA to 2.4A. The lower picture shows the behavior at light loads, starting from 5mA up to 200mA, while the input voltage was set to 3.3V.



Iout (A)	Vout (V)	Pout (W)	Iin (A)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.5149	4.128	2.13	0.9026	2.501	2.257	0.13	94.16%
1.0136	4.139	4.20	1.778	2.505	4.454	0.26	94.19%
1.504	4.143	6.23	2.659	2.506	6.663	0.43	93.51%
2.019	4.148	8.37	3.575	2.500	8.938	0.56	93.70%
2.404	4.147	9.97	4.270	2.505	10.696	0.73	93.20%

Iout (A)	Vout (V)	Pout (W)	Iin (A)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.5000	4.130	2.07	0.5984	3.600	2.154	0.09	95.86%
1.0139	4.140	4.20	1.213	3.603	4.370	0.17	96.04%
1.505	4.142	6.23	1.810	3.600	6.516	0.28	95.67%
2.002	4.148	8.30	2.393	3.603	8.622	0.32	96.32%
2.404	4.146	9.97	2.880	3.603	10.377	0.41	96.05%

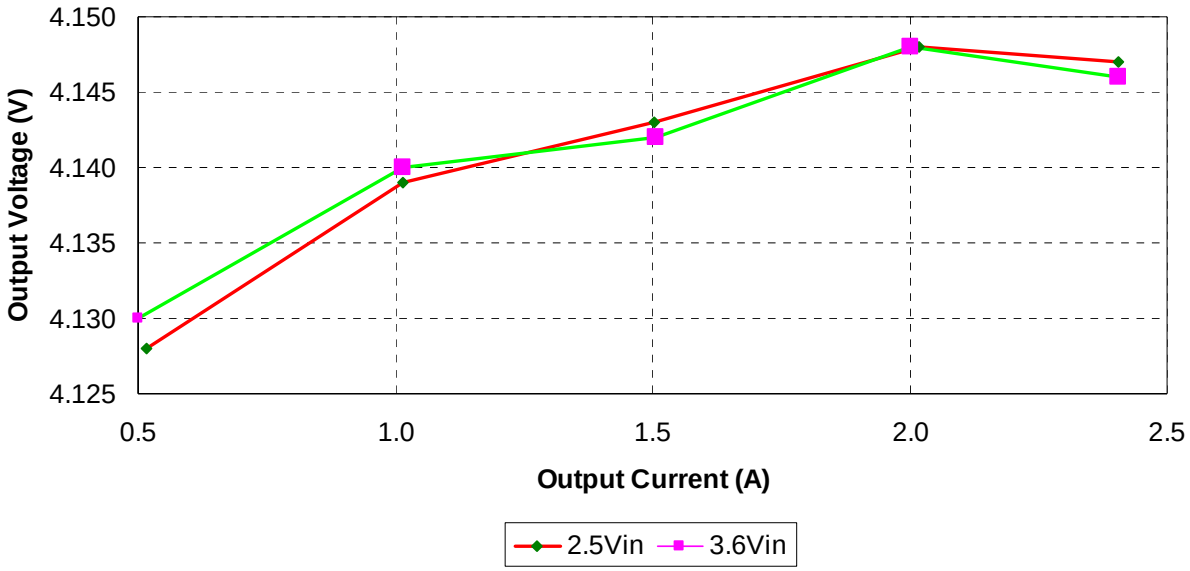
Efficiency at light load, 5mA…200mA; Vin = 3.3V

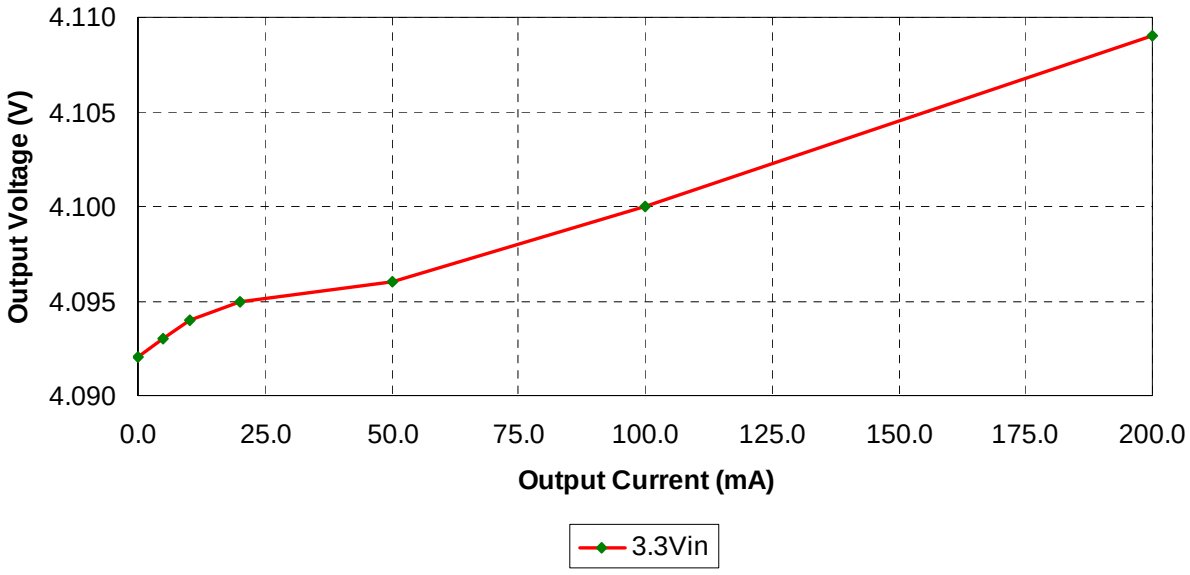


Iout (mA)	Vout (V)	Pout (mW)	Iin (mA)	Vin (V)	Pin (mW)	Ploss (mW)	Eff
0.00	4.092	0.0	0.1380	3.030	0.418	0.42	0.00%
5.05	4.093	20.7	6.80	3.300	22.440	1.77	92.11%
10.14	4.094	41.5	13.46	3.306	44.499	2.99	93.29%
20.03	4.095	82.0	26.51	3.304	87.589	5.57	93.65%
50.10	4.096	205.2	65.80	3.309	217.732	12.52	94.25%
100.00	4.100	410.0	131.4	3.308	434.671	24.67	94.32%
200.00	4.109	821.8	262.9	3.303	868.359	46.56	94.64%

3 Output voltage regulation

The two graphs below show how the converter regulates the output voltage, again for loads of 500mA to 2.4A and for light loads (below).

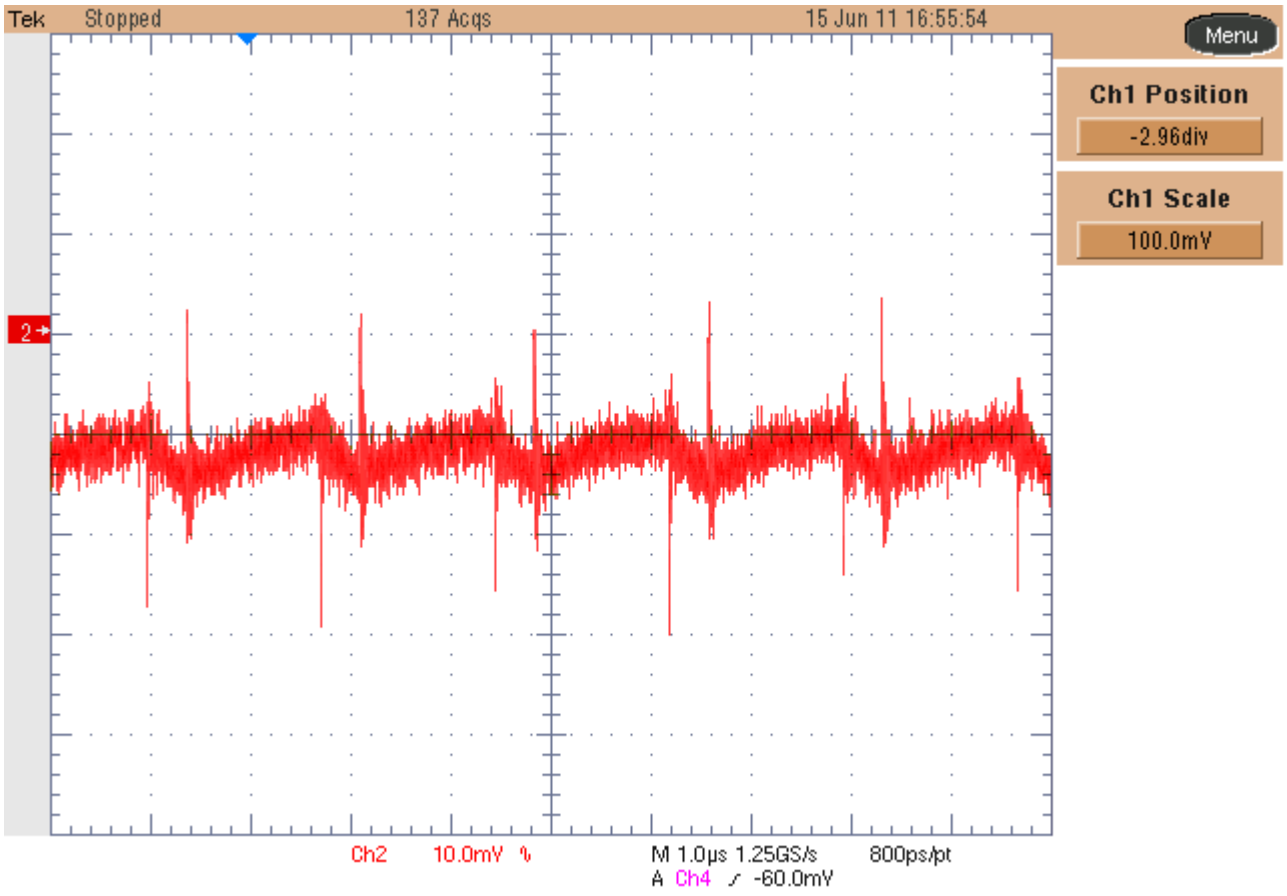




Output ripple voltage

The output ripple voltage, measured at full load (Iout=2.4A) and at 3.3V input, is shown in the plot below.

Channel 2: Output Voltage (10 mV/div, 1us/div, AC coupling, 20MHz BWL)

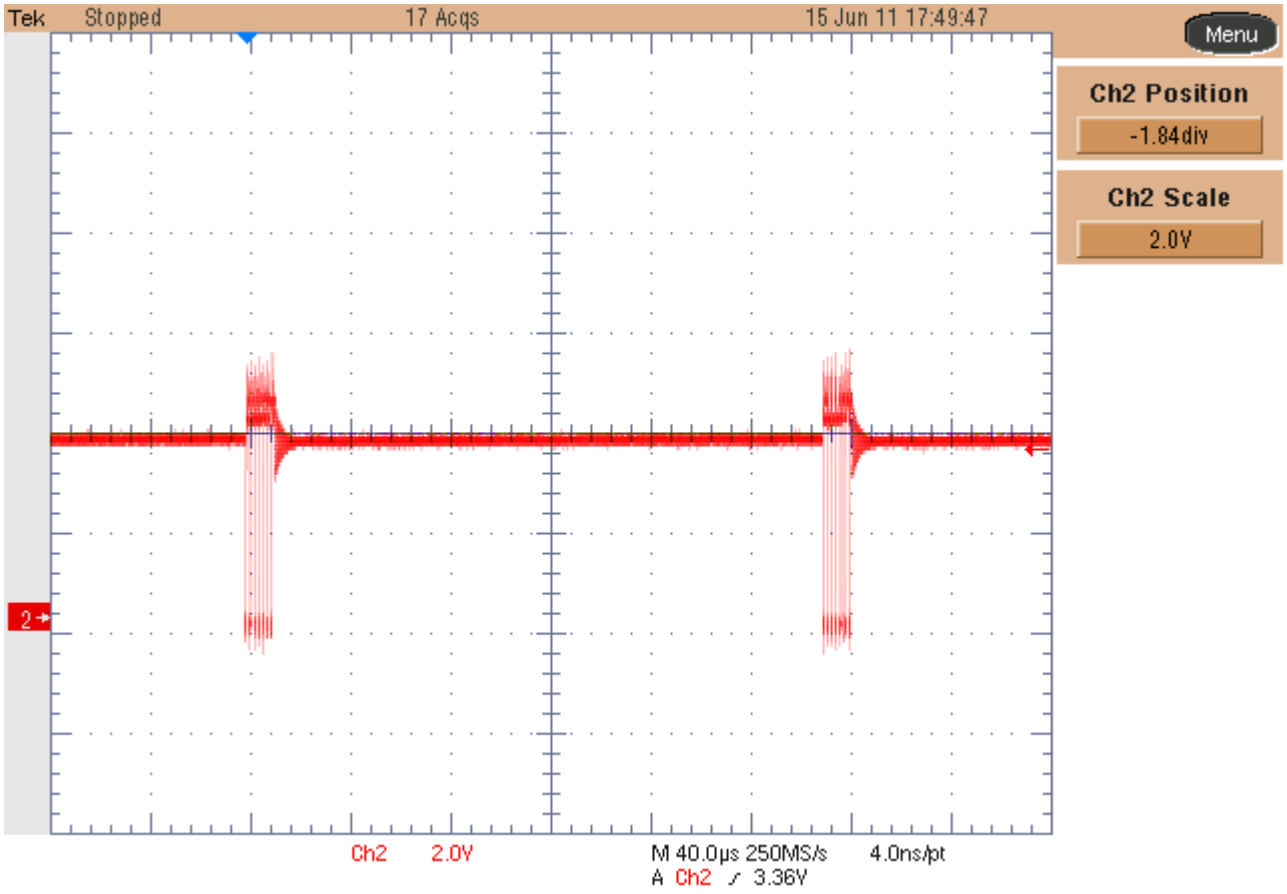


4 Switch-node

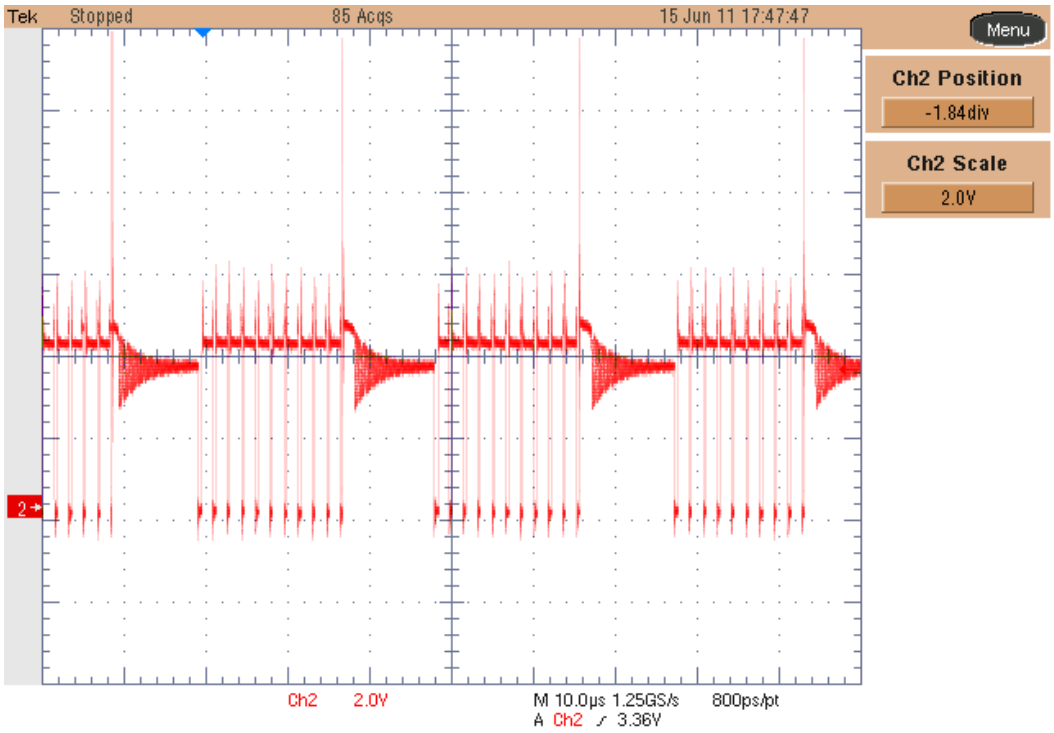
The images below show the switch-node waveform (drain of Q2). The input voltage was set to 3.3V and the output current respectively 30mA, 1A and 2.4A.

Channel 2: Q2, Drain Voltage (2 V/div, 40us/div, No BWL).

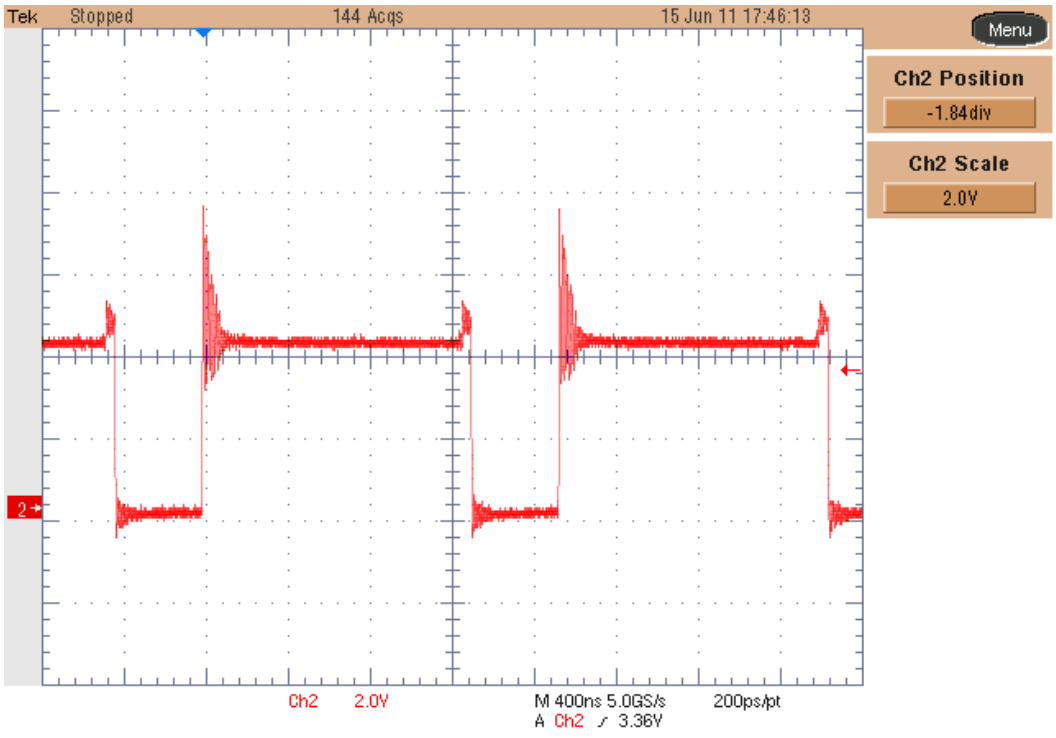
Output current = 30mA



Output current = 1A, Ch2: Q2 drain voltage (2 V/div, 10us/div, No BWL)



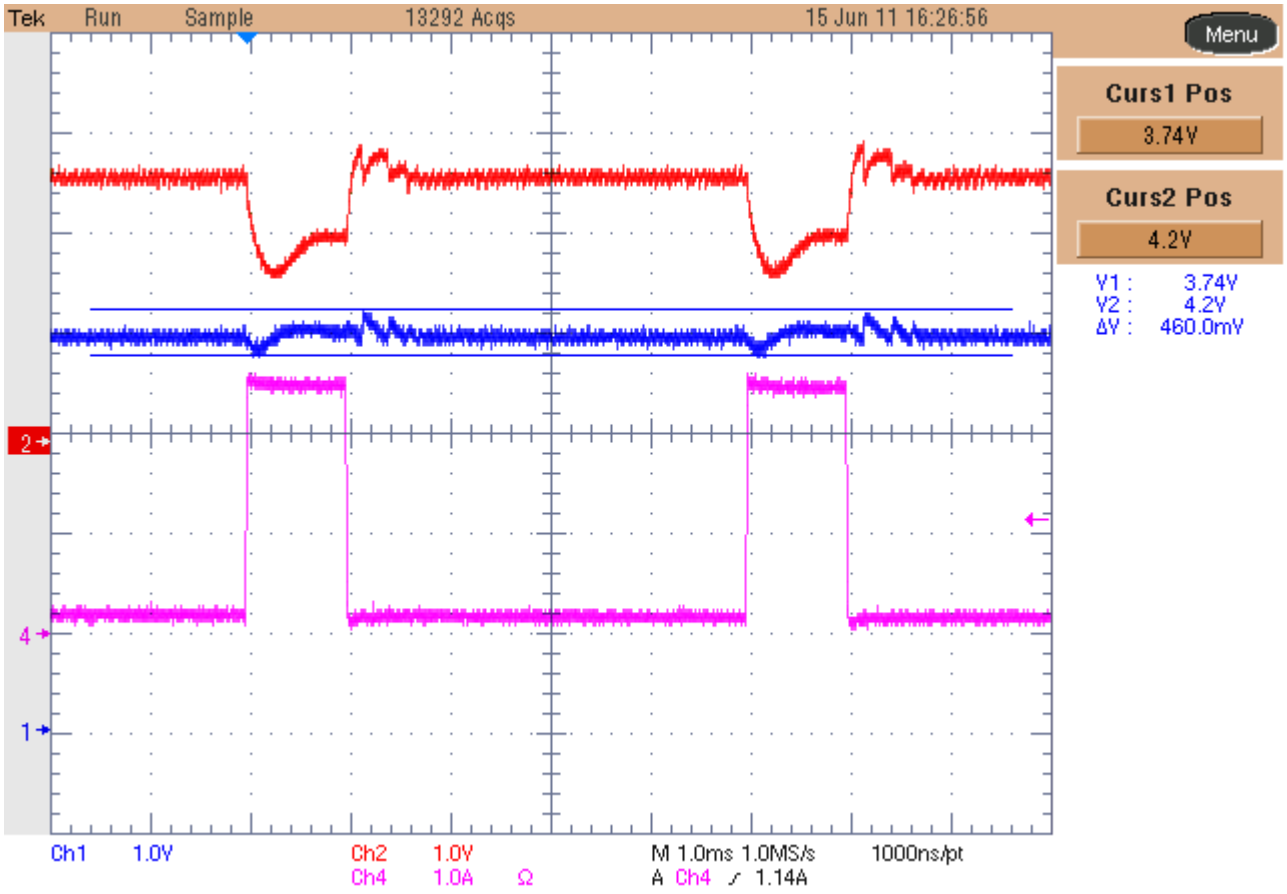
Output current = 2.4A, Ch2: Q2 drain voltage (2 V/div, 400ns/div, No BWL)



5 Transient response

The image below shows the transient response of the output voltage when the load was switched between 20mA and 2.4A. The input voltage was set to 2.6V.
Due to the drops on the cabling, the channel 2 shows the voltage measured directly on input capacitors (C1…C4), reaching a minimum value of 1.6V.

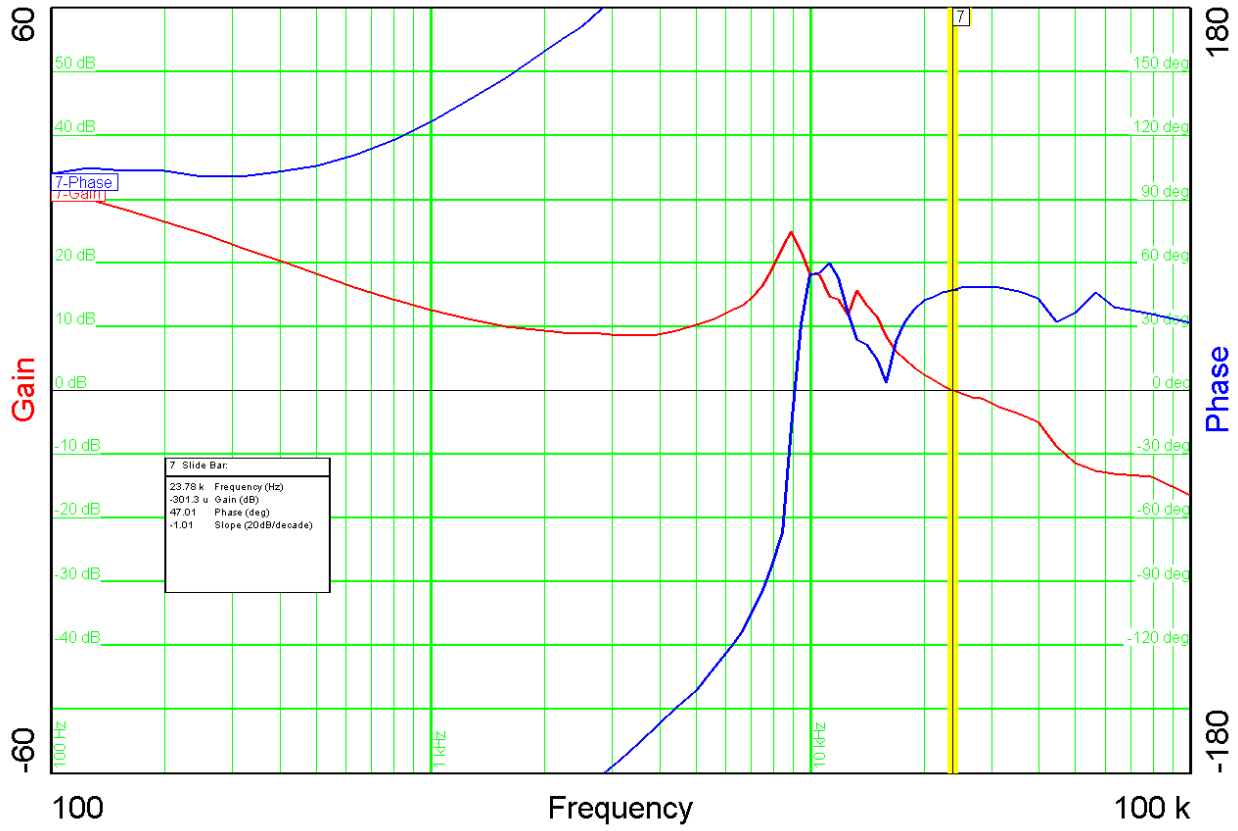
Channel 1: Output Voltage (1V/div, 1ms/div, DC coupling, No BWL).
Channel 2: Input Voltage (1V/div, 1ms/div, DC coupling, No BWL).
Channel 4: Output current (1A/div, DC coupling, No BWL).



6 Loop Response

The image below shows the loop response of the converter measured at 3V input voltage and 1A load. The converter works in CCM, thus generating a right half plane zero; the position of this zero is @ 168KHz worst case.

The measured phase margin was 47.01 deg., the crossover frequency was 23.78KHz and the slope -1.



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